A 0.13 μm CMOS UWB RF Transmitter with an On-Chip T/R Switch

Chang-Wan Kim, Quoc-Hoang Duong, Seung-Sik Lee, and Sang-Gug Lee

This paper presents a fully integrated 0.13 μm CMOS MB-OFDM UWB transmitter chain (mode 1). The proposed transmitter consists of a low-pass filter, a variable gain amplifier, a voltage-to-current converter, an I/Q up-mixer, a differential-to-single-ended converter, a driver amplifier, and a transmit/receive (T/R) switch. The proposed T/R switch shows an insertion loss of less than 1.5 dB and a Tx/Rx port isolation of more than 27 dB over a 3 GHz to 5 GHz frequency range. All RF/analog circuits have been designed to achieve high linearity and wide bandwidth. The proposed transmitter is implemented using IBM 0.13 μm CMOS technology. The fabricated transmitter shows a -3 dB bandwidth of 550 MHz at each sub-band center frequency with gain flatness less than 1.5 dB. It also shows a power gain of 0.5 dB, a maximum output power level of 0 dBm, and output IP3 of +9.3 dBm. It consumes a total of 54 mA from a 1.5 V supply.

Keywords: Transmitter, T/R switch, UWB, ultra-wideband, mixer, LPF, VGA, MB-OFDM, CMOS, RFIC.

I. Introduction

The ultra-wideband (UWB) system has emerged as a major technology for high data rate services in short-range wireless communication systems, including the wireless universal serial bus (USB), the wireless IEEE 1394, and the wireless link between HDTVs and laptop computers. The unlicensed UWB band between 3.1 GHz and 10.6 GHz has been reserved, and the transmitted spectrum shape of its modulated output power and maximum power level are limited to -41.3 dBm/MHz by the FCC [1].

In multi-band orthogonal frequency-division multiplexing (MB-OFDM) UWB systems, the UWB band of 3.1 GHz to 10.6 GHz is divided into 14 sub-bands with a bandwidth of 528 MHz, as shown in Fig. 1. Moreover, each sub-band is hopped within 9.5 ns for time-hopping. The MB-OFDM UWB devices, using the first 3 sub-bands (3,432 MHz, 3,960 MHz, and 4,488 MHz), are called mode 1 devices. The UWB transmitters for mode 1 are required to provide a total output power of -14.1 dBm for each sub-band of 528 MHz (or -9.3 dBm for hopping 3 sub-bands).

However, practically, the output average peak power level of the UWB transmitter should be about -1 dBm to 0 dBm for hopping 3 bands, considering the transmit/receive (T/R) switch loss (about 2 dB), the pre-band-pass filter (BPF) loss

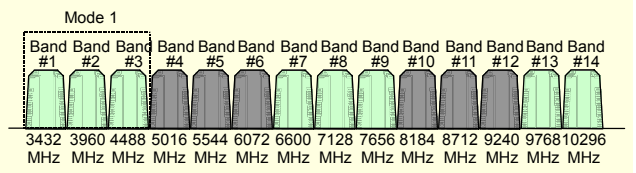

Fig. 1. MB-OFDM UWB frequency plan.

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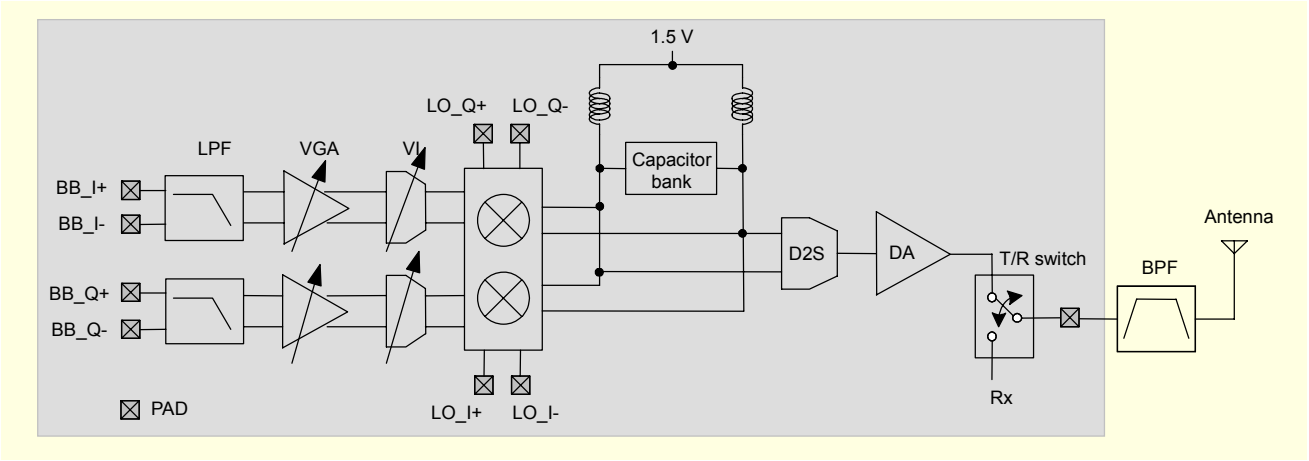


Fig. 2. Proposed CMOS direct-conversion UWB transmitter with an on-chip T/R switch.

(about 3 dB), the cable loss (about 2 dB), and back-off (about 6 dB). Finally, the UWB transmitters must be designed to have high linearity and broad bandwidth characteristics. Recently, several CMOS UWB transmitters (mode 1) have been reported [2]-[5].

This paper presents a highly linear 3-band MB-OFDM UWB transmitter chain with an on-chip T/R switch, which is implemented in 0.13 μm CMOS technology. To our knowledge, this is the first report to describe a CMOS UWB transmitter in which an on-chip T/R switch is integrated.

II. Architecture

Figure 2 shows a block diagram of the proposed 3-band CMOS MB-OFDM UWB direct-conversion transmitter, which consists of a low-pass filter (LPF), a variable gain amplifier (VGA), a voltage-to-current (VI) converter, an I/Q up-mixer, a differential-to-single-ended (D2S) converter, a driver amplifier (DA), and a T/R switch. As seen in Fig. 2, the fast hopping frequency synthesizer has been excluded from this work; therefore, three I/Q LO signals of 3,432 MHz, 3,960 MHz, and 4,488 MHz are provided by an external multi-LO generation module [6].

The baseband differential voltage signal of 600 $mV_{p\text{-}p}$ generated by an off-chip digital-to-analog converter (DAC) is applied to the input of the baseband LPF. To accommodate this high input voltage swing, an active resistor-capacitor (RC) LPF is used in this work. The active RC LPF has been implemented as a sixth-order Thomas biquad structure with attenuation of 40 dB from 285 MHz to 528 MHz. The overall transmitter gain variation range is 50 dB with 10 steps by the VGA (from -20 dB to +10 dB) and VI converter (-15 dB to +5 dB). The output voltage signal from the VGA is converted to current form by a high linear VI converter to achieve high linearity, and then its frequency is up-converted into RF frequency by the up-mixer. The output load of the mixer is an inductor-capacitor (LC) resonant circuit with a metal-insulator-metal (MIM) capacitor bank. The LC load resonates at the center frequency of each sub-band. The 3-bit MIM capacitor bank, which is controlled by a 3-bit digital control signal, changes the resonant frequency of the load. The differential output signal of the mixer is converted to the single-ended form by the D2S for connection with the single-ended driver amplifier. The T/R switch is implemented as a series configuration [7], which provides an input 1 dB compression point of 10 dBm. The proposed transmitter chain can provide output power in a range up to 0 dBm at the output of the T/R switch.

III. Circuit Design

Implementation of the wideband active UWB LPF with high linearity and high attenuation is a difficult challenge. In this work, the wideband UWB Tx LPF must accommodate a baseband differential input voltage signal of 600 $mV_{p\text{-}p}$ and have a high attenuation of 40 dB from 285 MHz to 528 MHz to suppress image signals created by the DAC. For high linearity, the sixth-order active RC LPF shown in Fig. 3 is proposed [8], [9]. The active RC LPF shows higher linearity characteristics than the G_m-C LPF, but its wideband characteristics are not sufficient. To achieve a wide bandwidth up to 264 MHz, we suggest the solution of using the Thomas biquad structure to implement the active RC filter. In Fig. 3, the three biquads show different bandwidths and quality (Q) factors respectively. The three different bandwidths and Q factors compensate each other so that the overall LPF can achieve a wider bandwidth of 264 MHz with a high rejection ratio of 40 dB. For process variation immunity, as shown in Fig. 4, the upper -3 dB cut-off frequency of the overall LPF can be changed from 222 MHz to 292 MHz with a resistor tuning of

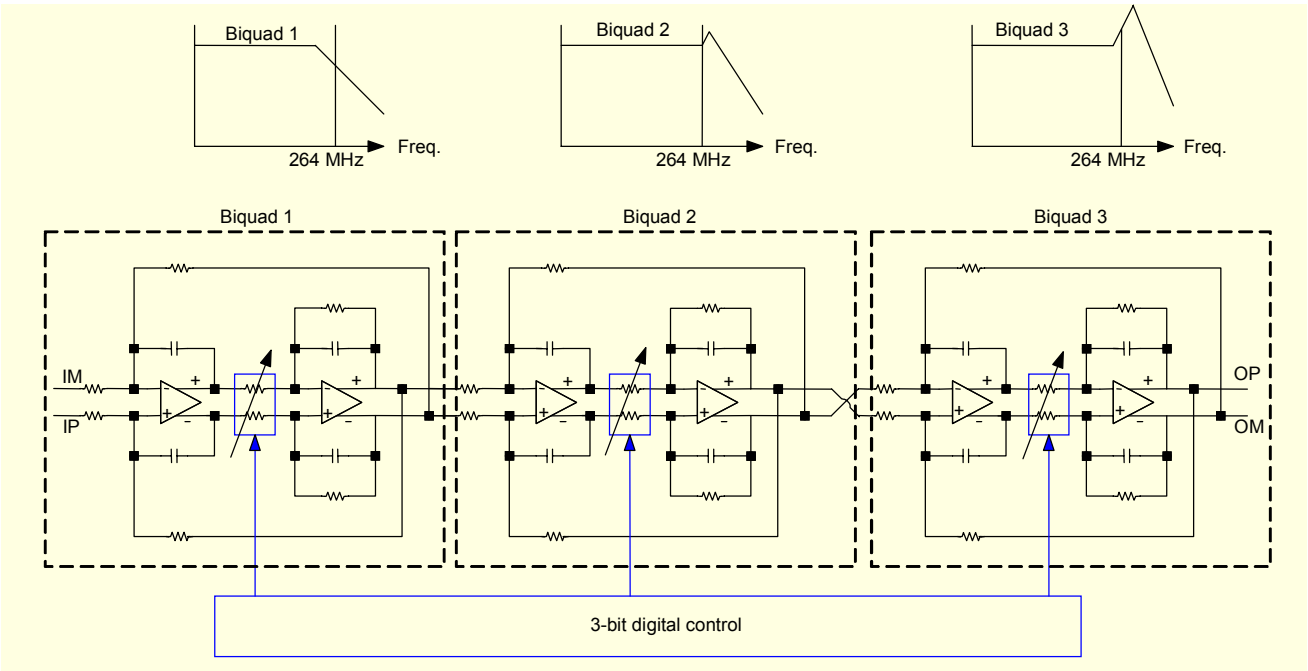
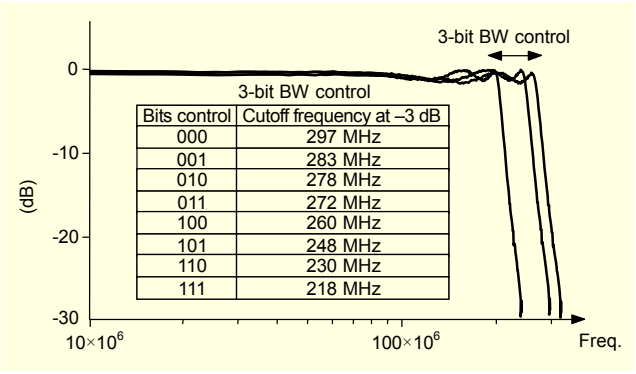


Fig. 3. Proposed sixth-order active RC LPF.



3-bit BW control

Bits control	Cutoff frequency at –3 dB
000	297 MHz
001	283 MHz
010	278 MHz
011	272 MHz
100	260 MHz
101	248 MHz
110	230 MHz
111	218 MHz

Fig. 4. Bandwidth tuning by 3 digital control bits.

3 digital control bits. The simulated maximum group delay of the LPF in the pass-band is less than 1.6 ns. The proposed LPF draws 7.2 mA from a 1.5 V supply.

Figure 5 shows the schematic of the VGA used in the transmitter chain [10]. The VGA consists of an input differential pair, M_1 and M_2; diode-connected NMOS transistors, M_3 and M_4; and active loads, where M_1=M_2 and M_3=M_4. The output node of the VGA is connected to a common-mode feedback (CMFB) circuit to stabilize the dc voltage at the output. Therefore, the differential voltage gain of the VGA shown in Fig. 5 can be briefly expressed as

$$A_v \cong \frac{g_{m1,2}}{g_{m3,4}} = \sqrt{\frac{(W/L)_{1,2}\, I_{C1}}{(W/L)_{3,4}\, I_{C2}}}. \quad (1)$$

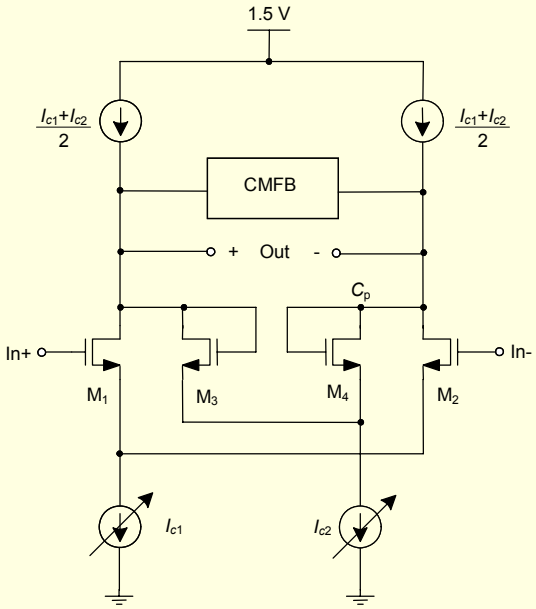


Fig. 5. Proposed analog variable gain amplifier (VGA).

Note that the differential voltage gain of the VGA is controlled by $(I_{C1}/I_{C2})^{1/2}$, where I_{C1} and I_{C2} are provided by a control circuit block (not shown in Fig. 5) generating dB-linear characteristics of $(I_{C1}/I_{C2})^{1/2}$ as a function of the control voltage [11]. The VGA shows a gain variation range of 30 dB (-20 to +10 dB) with 10 steps and an upper -3 dB bandwidth of 290 MHz with 6.5 mA. The VI converter is a constant transconductance (G_m) amplifier using an OP amplifier with

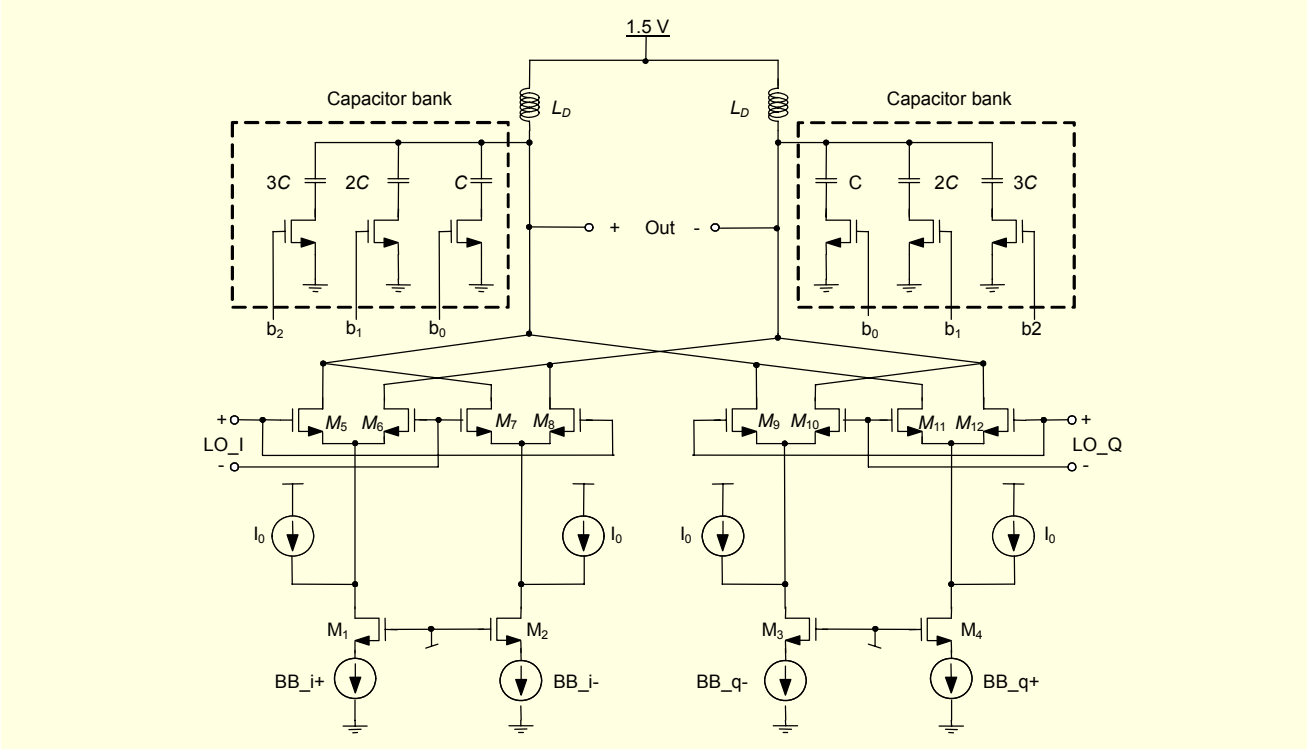


Fig. 6. Proposed I/Q up-mixer.

20 dB gain variation. The overall G_m of the VI converter remains almost constant until the large input voltage swing of 1 $V_{p\text{-}p}$.

The proposed UWB I/Q up-mixer, as shown in Fig. 6, is a single side-band (SSB) Gilbert mixer, which senses baseband input current signals from the VI converter. The major challenges in the design of the up-mixer are its broad bandwidth, spurious leakage into the adjacent bands, LO leakage at the output, and high linearity. To suppress unwanted spurious leakage and to achieve high voltage swing under the limited supply voltage of 1.5 V, the LC resonant circuit is adopted as the mixer output load. The LC load resonates at the center frequency of each sub-band, respectively, by the 3-bit MIM capacitor bank. The band-pass filtering characteristic of the LC load can provide high impedance for interested sub-bands but low impedance for other adjacent sub-bands. When the baseband signals enter the mixer, they are simultaneously multiplied with both a wanted LO tone and unwanted leakages of LO tones for other adjacent bands. Due to the band-pass filtering characteristic of the LC load, the baseband signals which have been multiplied with a wanted LO tone are accordingly up-converted into RF and achieve a high gain. However, those multiplied with leakages of other LO tones have a low gain. The frequency selectivity issues are very important for both the transmitter and receiver chain in MB-OFDM UWB applications. The LC load can provide more

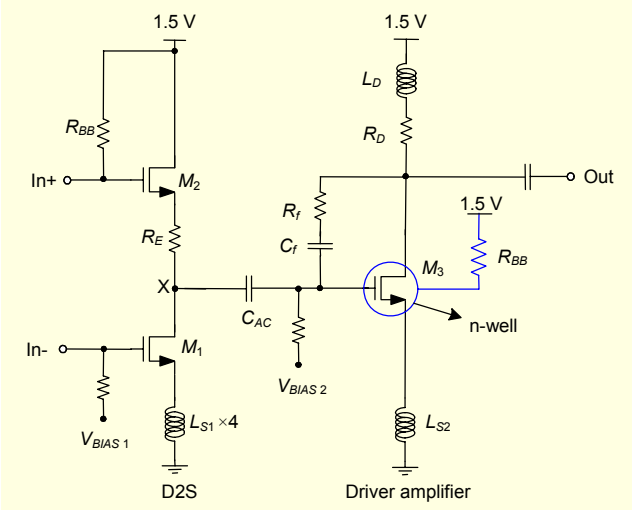


Fig. 7. Proposed D2S and driver amplifier.

gain and high linearity given the dc power consumption compared to shunt-peaking load [12]. For gain flatness in each sub-band, two on-chip spiral inductors (L_{d1} and L_{d2}) in the mixer have a low Q of about 4 at 4 GHz. The current sources I_0 permit high current in the transconductance stage and low current in the switching pairs, improving linearity and conversion gain in the Gilbert mixer. The proposed IQ mixer consumes 13 mA.

Figure 7 shows the proposed D2S converter and the driver

amplifier. The proposed driver amplifier is constructed in a single-ended configuration in consideration of the DC power consumption. To connect the differential output of the up-mixer into the single ended input of the driver amplifier, differential output signals from the up-mixer are converted to single-ended forms in the D2S. As shown in Fig. 7, to improve summation of input differential signals and rejection of input common-mode noises, the conventional D2S is modified in this work. At node X shown in Fig. 7, the source node of M_2 is degenerated by a resistor, R_E, to reduce the voltage gain of common-drain amplifier M_2 and increase the load impedance $1/g_{m2}+R_E$ of the common-source amplifier, M_1. In addition, four down-bonding wires for grounding are connected in parallel with the source node of M_1 to increase its voltage gain. L_{S1} is the bonding wire parasitic inductance. As shown in Fig. 7, the proposed driver amplifier adopts the common-source configuration to supply sufficient voltage margins for the maximum output power level of 2 dBm. The input transistor M_3 is a deep n-well MOSFET device, where the n-well terminal is connected to the supply voltage via a 10,000 ohm resistor, R_B, to mitigate a parasitic capacitance effect between the p-well and the n-well [13], improving the high frequency characteristics of the device. The shunt-peaking load (L_D and R_D) and feedback path (R_f and C_f) provide both broad bandwidth and lower output impedance. In Fig. 7, L_D is the on-chip spiral inductor and L_{S2} is the bonding wire parasitic inductance. The D2S and driver amplifier draw 5 mA and 8.5 mA, respectively.

From previously reported T/R switches [14]-[17], the series-shunt T/R switch configurations show better isolation characteristics with shunt transistors than the series configurations provide. However, the measurement results in these works are based on on-wafer tests and do not include parasitic bonding wire inductances. When parasitic inductances from ground bonding wires cannot be ignored, they can resonate with the parasitic capacitance of the shunt transistors. If peaking by this series resonance occurs in the interested UWB band, major characteristics of the series-shunt T/R switches can be considerably degraded. In this work, the proposed T/R switch is implemented as the series configuration shown in Fig. 8 to avoid the possibility of these series resonance problems. The device sizes of M_1 and M_2 are carefully chosen as W/L=75-μm/0.13-μm considering the trade-off between insertion loss and isolation [15]. In Fig. 8, switch transistors M_1 and M_2 are deep n-well MOS transistors, which can provide better substrate isolation between other RF building blocks. As shown in Fig. 8, however, each local body terminal (B) of M_1 and M_2 is independently connected to the ground for better isolation between the Tx and Rx ports. Figure 9(a) shows the conventional deep n-well NMOSFET cross structure and major parasitic capacitances. Other parasitic

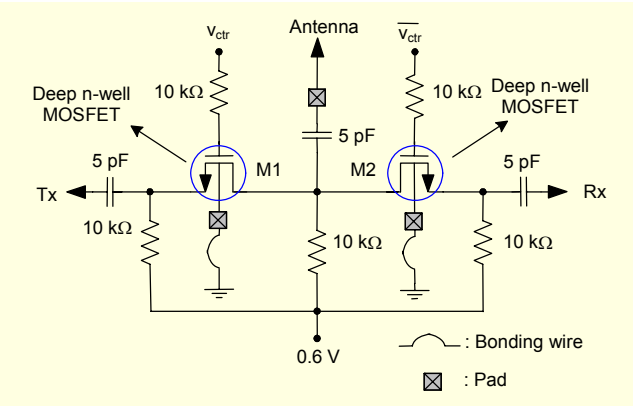


Fig. 8. Proposed on-chip T/R switch.

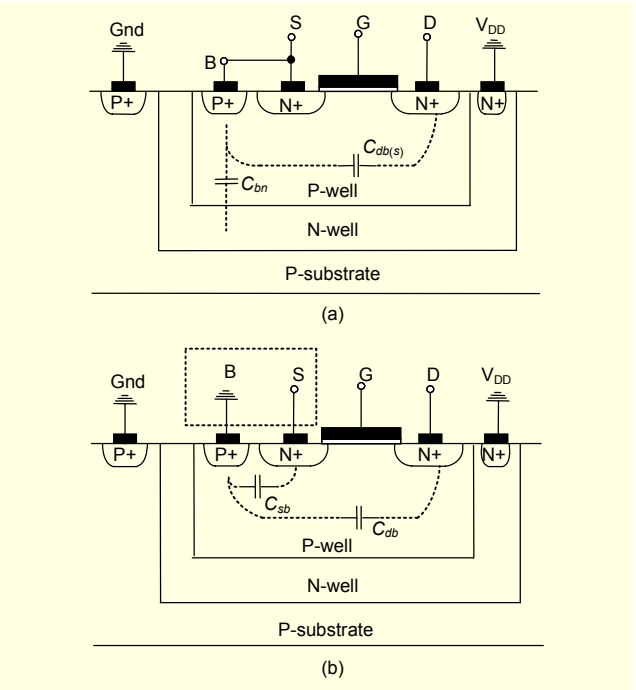


Fig. 9. (a) Conventional deep n-well NMOSFET cross structure in which the local body is connected to the source and (b) local body attached to the ground node, instead of the source in the deep n-well structure to remove parasitic capacitance between the drain and the source.

capacitances are omitted for simplicity. The deep n-well NMOSFET inherently produces additional parasitic capacitance $C_{db(s)}$ between the drain (D) and the source (S) because its local body is generally connected with the source. This parasitic capacitance $C_{db(s)}$ produces an unwanted signal path from the drain to the source when the transistor turns off; therefore, it considerably increases unwanted signal coupling between the drain and the source. To overcome this problem, the structure of the deep n-well NMOSFET is modified in this work, as shown in Fig. 9(b). In Fig. 9(b), the local body is disconnected from the source but attached to the ground node.

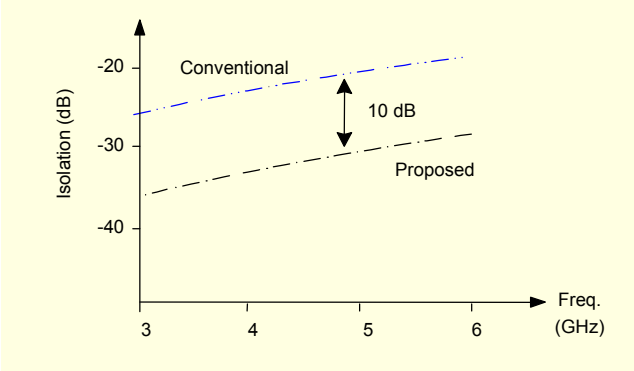


Fig. 10. Simulated isolation characteristic.

This modification can avoid parasitic capacitance $C_{db(s)}$ in the deep n-well MOSFET. When other parasitic capacitances (C_{gd}, C_{gs}, and so on) are ignored, only the drain/source to substrate junction capacitors (C_{db} and C_{sb}) affect the switch isolation.

Figure 10 shows the simulated isolation characteristics between a T/R switch using the device shown in Fig. 9(a) and the proposed T/R switch using the device shown in Fig. 9(b) , when they all operate as Tx mode; M_1 is on and M_2 is off. As shown in Fig. 10, isolation of the proposed configuration using the device shown in Fig. 9(b) is 10 dB better than that of the T/R switch using the deep n-well devices shown in Fig. 9(a). As shown in Fig. 8, all drain and source nodes are dc-biased to 0.6 V for less parasitic junction capacitances from the drain and source to the p+ silicon substrate and power handling capability. The values of V_{ctl} and $\overline{V_{ctl}}$ are 1.5 V and 0 V, respectively.

IV. Measurement Results

The proposed UWB transmitter chain was implemented using IBM 0.13 μm CMOS technology. The die micrographic image is shown in Fig. 11, and the core area is 1.1 mm^2 without pads. Chip evaluations were performed on MLF packaged samples. The chips were mounted on an FR4 PCB. Quadrature LO tones of -3 dBm are externally provided to the chip by a

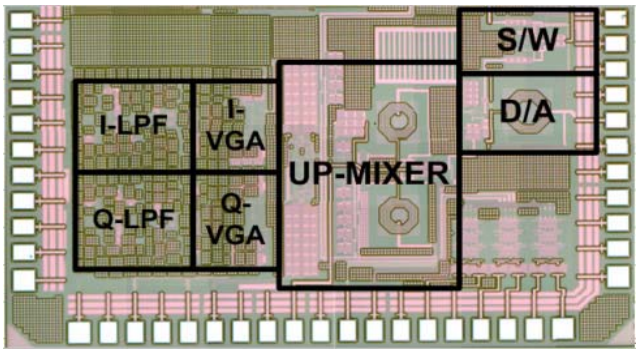


Fig. 11. Chip micrograph.

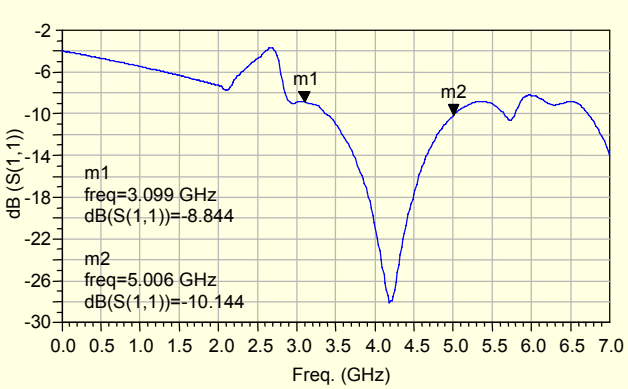


Fig. 12. Output return loss.

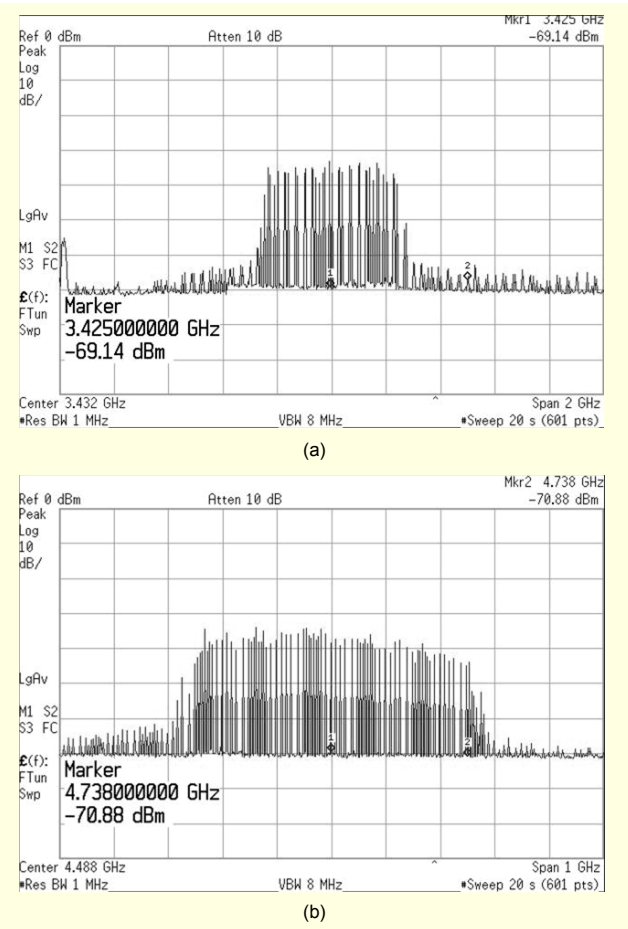


Fig. 13. Transmit spectra for (a) band 1 and (b) band 3.

hybrid module. The fabricated transmitter chain consumes 54 mA from a 1.5 V supply. Figure 12 shows the measured output return loss of the transmitter. Over the frequency range from 3.1 GHz to 5 GHz, the output return loss is more than -8 dB. Figure 13 shows the transmit spectra of bands 1 and 3 when OFDM baseband signals generated by an off-chip baseband chip are applied to the transmitter. The transmit spectra shown

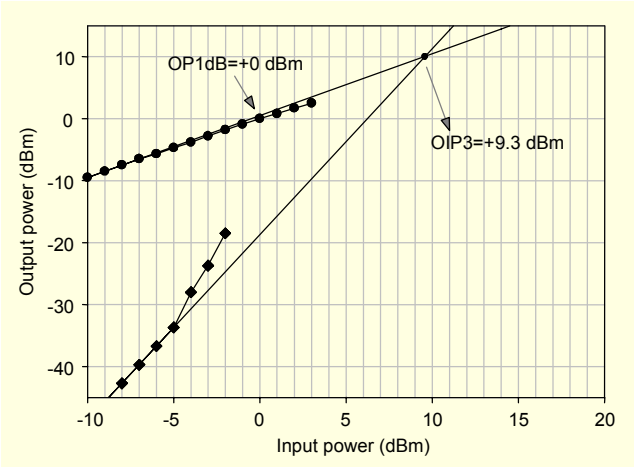


Fig. 14. Measured OP1dB and OIP3 for band 1.

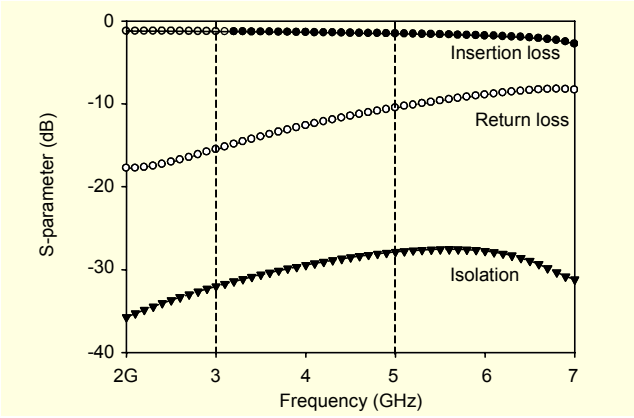


Fig. 15. Measured T/R switch performance.

Table 1. Performance summary.

	This work	[12]	[13]	[14]	[15]
Frequency range (GHz)	3-5	3.1-10.6	5.8	2.4-20	3-10
Insertion loss (dB)	1.5*	2.2*	0.8	1.5**	2.5*
Isolation (dB)	27*	34*	29	34**	30*
Input P1 dB (dBm)	10	n/a	17	30	20
CMOS technology	0.13 μm	0.13 μm	0.18 μm	0.13 μm	0.18 μm

*Measured results at 5 GHz, **Measured results at 5.8 GHz

in Fig. 13 were measured at the output of the external BPF, following the MLF packaged transmitter. They all meet the FCC UWB spectrum requirements [1]. The measured LO leakage power levels are -44, -44, and -43.3 dBm for each band, respectively. With an external quadrature baseband input signal of 10 MHz, the measured SSB rejection ratio for the three bands are is 28 dBc, 27.7 dBc, and 26.3 dBc, respectively.

Table 2. Performance summary.

	This work*	[2] & [11]	[3]	[4]
Output P1dB	+0 dBm	-10 dBm	+4.7 dBm	+5 dBm
EVM	n/a	n/a	-27.2dB	-27 dB
Output IP3	+9.3 dBm	n/a	11.8 dBm	n/a
Current consumption	54 mA	70 mA**	220.5 mA**	65 mA
Supply voltage	1.5 V	1.5 V	1.8 V	1.5 V
CMOS technology	0.13 μm	0.13 μm	0.18 μm	0.13 μm

*with an on-chip T/R switch, **with a frequency synthesizer

For linearity measurements, two baseband tones of 10 MHz and 11 MHz were applied to the transmitter input. As shown in Fig. 14, the measured output P1dB and output IP3 for band 1 are 0 dBm and 9.3 dBm, respectively.

The proposed T/R switch shown in Fig. 8 was also measured after it was mounted on the FR4 PCB to evaluate its characteristics. Bonding wire inductance effects were included in this test. As shown in Fig. 15, when the T/R switch operates in Tx mode, the measured insertion loss from Tx to the output port is less than 1.5 dB, and isolation between Tx and Rx is more than 27 dB between 3 GHz and 5 GHz. Return loss for the Tx port is more than -10 dB. As shown in Table 1, performance of the proposed T/R switch is comparable to on-wafer probing measurement results of the series-shunt T/R switches [14]-[17].

Table 2 summarizes the measurement results of the fabricated transmitter and those of previous works. The proposed UWB transmitter shows improved performance with lower DC power consumption than other mode 1 UWB transmitters.

V. Conclusion

We have demonstrated a fully integrated MB-OFDM mode 1 UWB transmitter including a T/R switch, which was fabricated using 0.13 μm CMOS technology. The measured results demonstrate that the proposed transmitter favorably supports the MB-OFDM requirements. Moreover, the proposed T/R switch is suitable for UWB applications.

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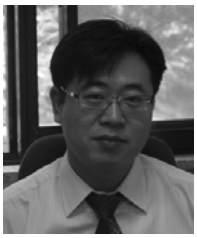

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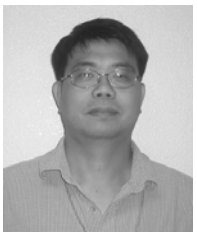

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