Low-Power 512-Bit EEPROM Designed for UHF RFID Tag Chip

Jae-Hyung Lee, Ji-Hong Kim, Gyu-Ho Lim, Tae-Hoon Kim, Jung-Hwan Lee, Kyung-Hwan Park, Mu-Hun Park, Pan-Bong Ha, and Young-Hee Kim

In this paper, the design of a low-power 512-bit synchronous EEPROM for a passive UHF RFID tag chip is presented. We apply low-power schemes, such as dual power supply voltage (VDD=1.5 V and VDDP=2.5 V), clocked inverter sensing, voltage-up converter, I/O interface, and Dickson charge pump using Schottky diode. An EEPROM is fabricated with the 0.25 μm EEPROM process. Power dissipation is 32.78 μW in the read cycle and 78.05 μW in the write cycle. The layout size is 449.3 μm × 480.67 μm.

Keywords: Low-power, EEPROM, UHF RFID, tag chip, sensing scheme, dual power, charge pump.

I. Introduction

Radio frequency identification (RFID) is the technology to provide various communication services between objects by collecting, storing, and revising information regarding these objects by using RFID tags installed or attached to them. RFID tags are classified according to communication ability, battery existence, and read/write function as shown in Table 1 [1]. They are standardized by Electronic Product Code (EPC) Global. Currently, passive RFID tags are more widely used than their active counterparts because they are low-cost and small-sized. Therefore, more effort has been devoted to the development of the passive tags [2].

A class 1 generation 2 tag is a passive tag like class 0 and class 2 tags, but it has advantages of cost and size. It can read and write, but it also has a lock function for security and a kill function, which causes the tag to be reprogrammed or instructs it to self-destruct. These advantages are expected to apply in logistics, traffic, and inventory management; therefore, there is a great deal of research progressing in this area.

A passive UHF RFID tag comprises an antenna and a tag chip as shown in Fig. 1. The tag chip consists of analog, logic, and memory blocks [3]. In the analog block there is a demodulator to convert frequency into data, a modulator to convert data into frequency, and a voltage multiplier to convert energy from the antenna into supply voltage in the analog circuit. The logic controls the operation modes of the analog block, checks the protocol, performs the cyclic redundancy check (CRC), and checks for errors. The memory block must be read out and written in; therefore, non-volatile memory, that is, EEPROM, which keeps data during power-down, is often used. A low-power circuit is required to transfer data to the

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Table 1. Classification of RFID tags.

EPC tag class	Capabilities	Memory
Class 0	Read only (i.e., the EPC number is encoded onto the tag during manufacture and can be read by a reader)	64 bits
Class 1	Read, write once→write many (Generation 2)	96 bits 128/256 bits (Generation 2)
Class 2	Read, write.	Larger memory
Class 3	Class 2 capabilities plus a power source to provide increased range and/or advanced functionality	
Class 4	Class 3 capabilities plus active communication and the ability to communicate with other active tags	
Class 5	Class 4 capabilities plus the ability to communicate with passive tags as well	

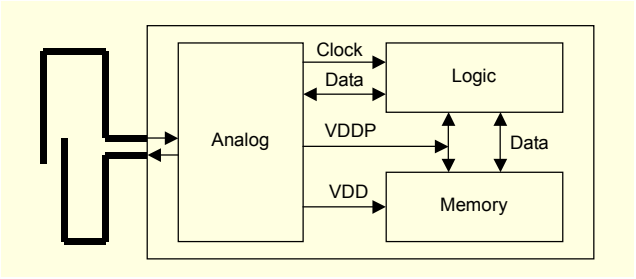

Fig. 1. Architecture of RFID tag chip.

reader and to check identifications because the voltage multiplier of the analog block transforms UHF signal into power [4].

II. Circuit Design

Figure 2 shows a block diagram of the 512-bit synchronous EEPROM. It consists of a cell array (64 rows × 8 columns), a row decoder, a data buffer, control logic to generate control signals at different operation modes, and a DC-DC converter to provide high voltages (VPP and VPPL). The interface signals are clock control signals, command control signals, address bus, and bi-directional data bus. The clock control signals are clock (CLK) and clock enable (CKE). For command control signals, there are REb (read enable), WEb (write enable), OEb (output enable), ERSb (erase), PGMb (program), and RSTb (reset).

The width of the address bus is 6, and that of the data is 8. One of 64 bytes is selected by 6 address lines, and the unit of operation is one byte in both read and write modes. The main features of the EEPROM are shown in Table 2.

Figure 3 shows the cross-sectional view of an EEPROM cell.

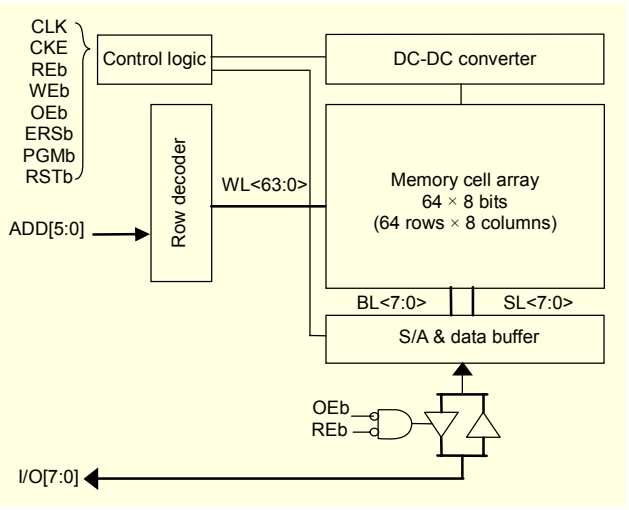

Fig. 2. Block diagram of 512-bit synchronous EEPROM.

Table 2. Main features of the EEPROM.

Items	Main features
Technology	0.25 μm EEPROM process
Memory cell	EEPROM
ONO thickness	100 Å
Operating modes	Erase / program / read / stand-by
Supply voltage	VDD=1.5 V / VDDP=2.5 V
BL sensing scheme	Clocked inverter
Charge pump	Dickson pump

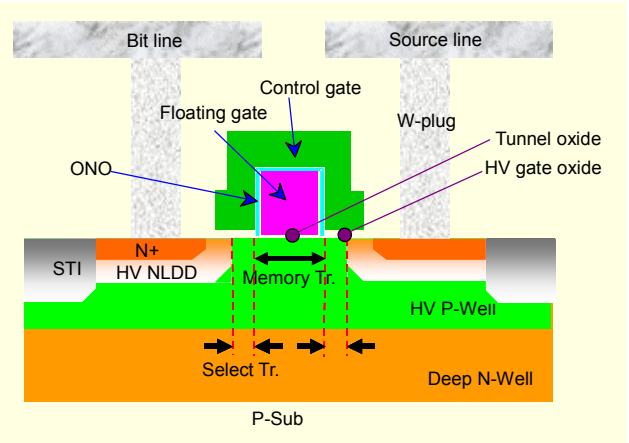

Fig. 3. Cross-sectional view of EEPROM cell.

The dielectric between the control gate and the floating gate is surrounded by oxide-nitride-oxide to get a high coupling ratio, and the EEPROM is in the triple-well [5]. The cells can be erased and programmed by Fowler-Nordheim tunneling. The control gate is connected to the word-line (WL), that is, the

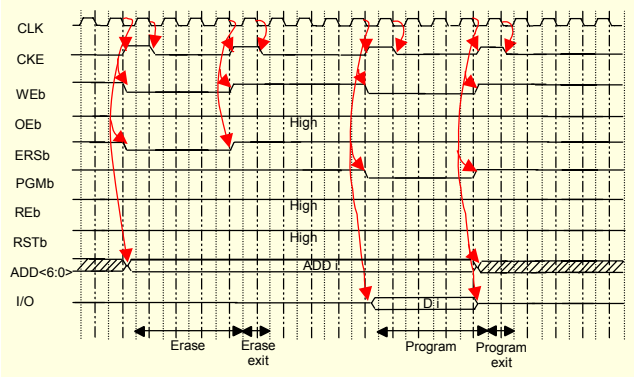

Fig. 4. Write timing diagram of synchronous EEPROM.

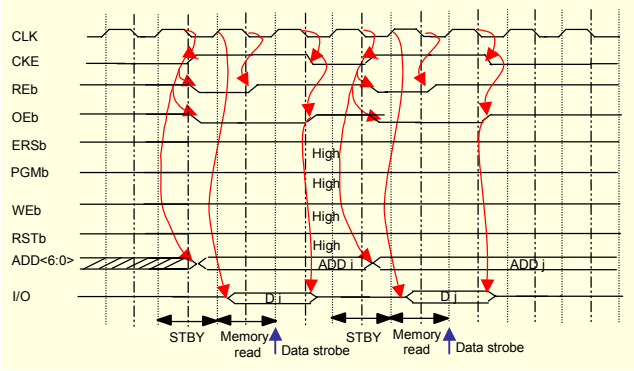

Fig. 5. Read timing diagram of synchronous EEPROM.

output node of the row decoder. The EEPROM has four operating modes: program, erase, read, and stand-by. They operate synchronously with the clock signal. Write mode includes program and erase modes. Dual power supply voltage, VDD (1.5 V) and VDDP (2.5 V), is used to reduce the current in both read and write modes.

Figure 4 shows a write timing diagram in which one byte cell is first erased and then data is programmed. Figure 5 shows a read timing diagram of the synchronous EEPROM. Data in the read cycle is transferred by the logic circuit of the tag chip at the rising edge of the next clock cycle after the read command is enabled.

Table 3 shows bias voltage levels of the EEPROM cell for the four operating modes. The WL voltage of the selected cell is 16.5 V, that is VPP (boosted voltage), in the program mode. The bit-line (BL) voltage is 15 V (VPP) in the erase mode. The non-selected BL voltage is 11.5 V (VPP-5 V) in the program mode and 11 V (VPP-4 V) in the erase mode. When normal transistors that have low break-down voltage are connected to the row decoder and column select circuits, device reliability problems occur. For that reason, high voltage transistors with threshold voltages between 0.87 V and 1.29 V have to be used to stand high voltage in the row decoder and column select circuits. If only VDDP is used, the circuits operate properly, but power

Table 3. Bias voltage conditions for the four operation modes of the EEPROM cell.

(V)

	Program		Erase		Read		Stand-by
	Selected cell	Non-selected cell	Selected cell	Non-selected cell	Selected cell	Non-selected cell	Selected cell
Word-line	16.5	0	0	11	2.5	0	0
Bit-line	0	11.5	15	11	1.5	Floating	Floating
Source-line	Floating	Floating	Floating	Floating	0	0	0
HV-Pwell	0	0	15	0	0	0	0
Deep-Nwell	2.5	2.5	15	15	2.5	2.5	2.5

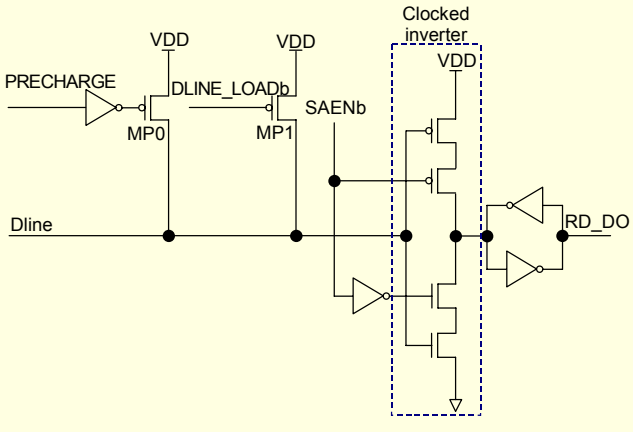

Fig. 6. Clocked inverter sensing circuit.

dissipation increases in proportion to VDDP in the read mode. On the other hand, if only VDD is used in the circuits, power dissipation decreases; however, circuits that have transistors with a threshold voltage of 1.29 V do not operate properly. Therefore dual power supply voltage (VDDP for high voltage transistors and VDD for the others) is used to reduce power dissipation.

A clocked inverter sensing method is applied to read out the data of EEPROM cells in the read mode [8]. Usually, a current sensing circuit is used for the non-volatile memory [6]. This is not proper in the EEPROM design for RFID tag chips because the current dissipation of the sensing circuit is large. Therefore, a low-speed low-power read data (RD) sense amplifier should be used without a reference current biasing circuit. The clocked inverter sensing circuit is shown in Fig. 6.

A short pulse is generated by the PRECHARGE signal before the control gate voltage (WL) is active in the read mode. It drives a PMOS transistor, MP0, to the precharge DLINE signal to VDD. After the WL is active, the DLINE signal keeps the VDD

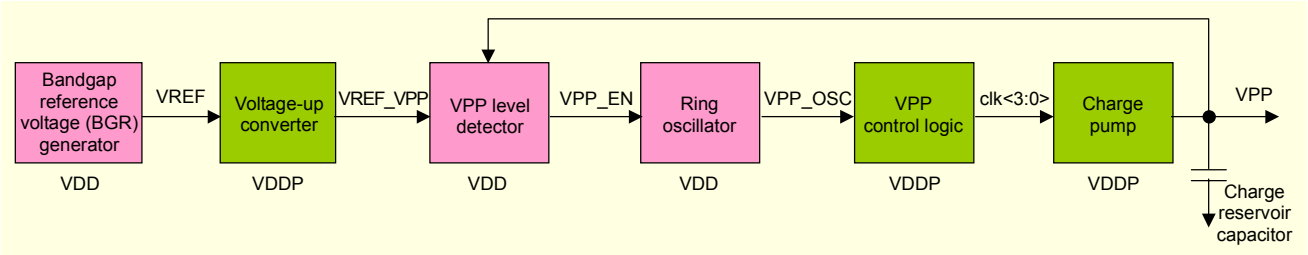

Fig. 7. Block diagram of the DC-DC converter.

Table 4. VREF, VREF_VPP, VPP, and VPPL voltage levels in different operating modes. (V)

	Program	Erase	Read	Stand-by
VREF	0.75	0.685	0	0
VREF_VPP	1.5	1.37	0	0
VPP	16.5	15	2.5	2.5
VPPL	11.5	11	2.5	2.5

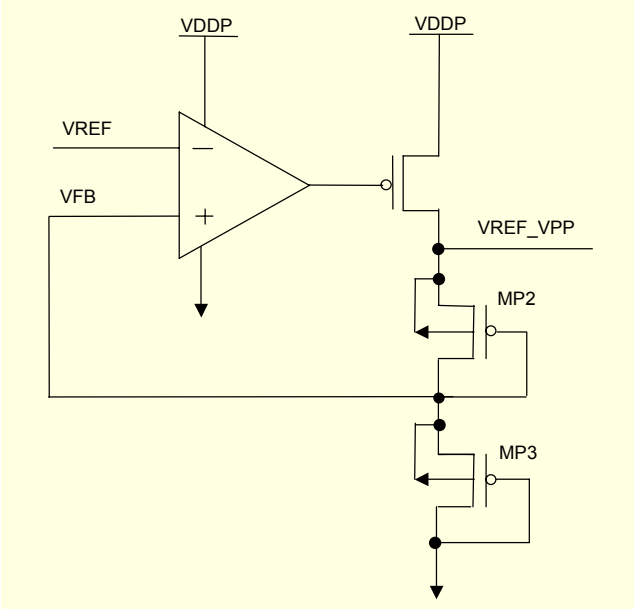

Fig. 8. Voltage-up converter circuit.

level because current cannot flow through the programmed cells. On the other hand, the DLINE signal is almost 0 V because current flows through the non-programmed cells. If there is enough data to be transferred to the DLINE signal, the SAENb signal in the clocked inverter is enabled, and the data is read out to DLINE. The load transistor, MP1, acts like an active load while WL is selected. It prevents DLINE falling to 0 V because the leakage current during EEPROM is off.

Figure 7 shows a block diagram of the DC-DC converter, which uses a Dickson charge pump [7] to generate high voltage

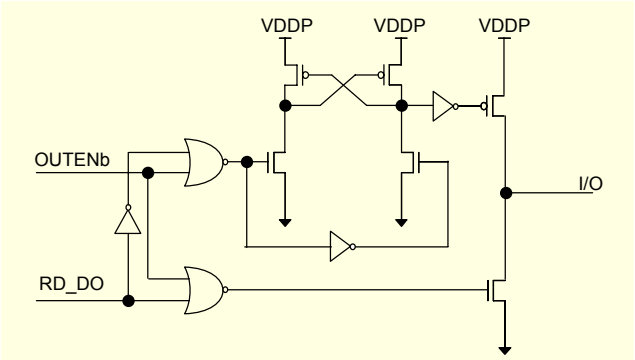

Fig. 9. I/O interface circuit.

Table 5. Power dissipation comparison in the program mode.

	PN diode	Schottky diode
Power dissipation in the program mode	65.7 μW	57.7 μW

in the write mode. It consists of a bandgap reference voltage generator, a VPP level detector, a ring oscillator, a VPP control logic, and a charge pump.

If VPP is lower than the target voltage of the load current, VPP_EN becomes high. Then, a ring oscillator oscillates to increase VPP. That causes a positive charge to pump into the VPP node and VPP increases. If VPP is higher than the target voltage, then VPP_EN (the output of the VPP level detector) is low and pumping stops in order to keep the output voltage to VPP by using negative feedback. To decrease power dissipation, VDD power is used in the bandgap reference voltage generator, VPP level detector, and ring oscillator circuits, and VDDP power is used in the voltage-up converter, VPP control logic, and charge pump circuits. In the VPP level detector circuit, an eleventh of VPP, which is divided by NMOS diodes in series, is compared with VREF_VPP to control the charge pump. The VREF_VPP is 1.5 V in the program mode and 1.37 V in the erase mode as shown in Table 4. For low power dissipation, the VDD power source which is lower than the VDDP power source is used in the bandgap reference voltage generator. However, it cannot generate the reference voltage, 1.5 V, using only VDD power.

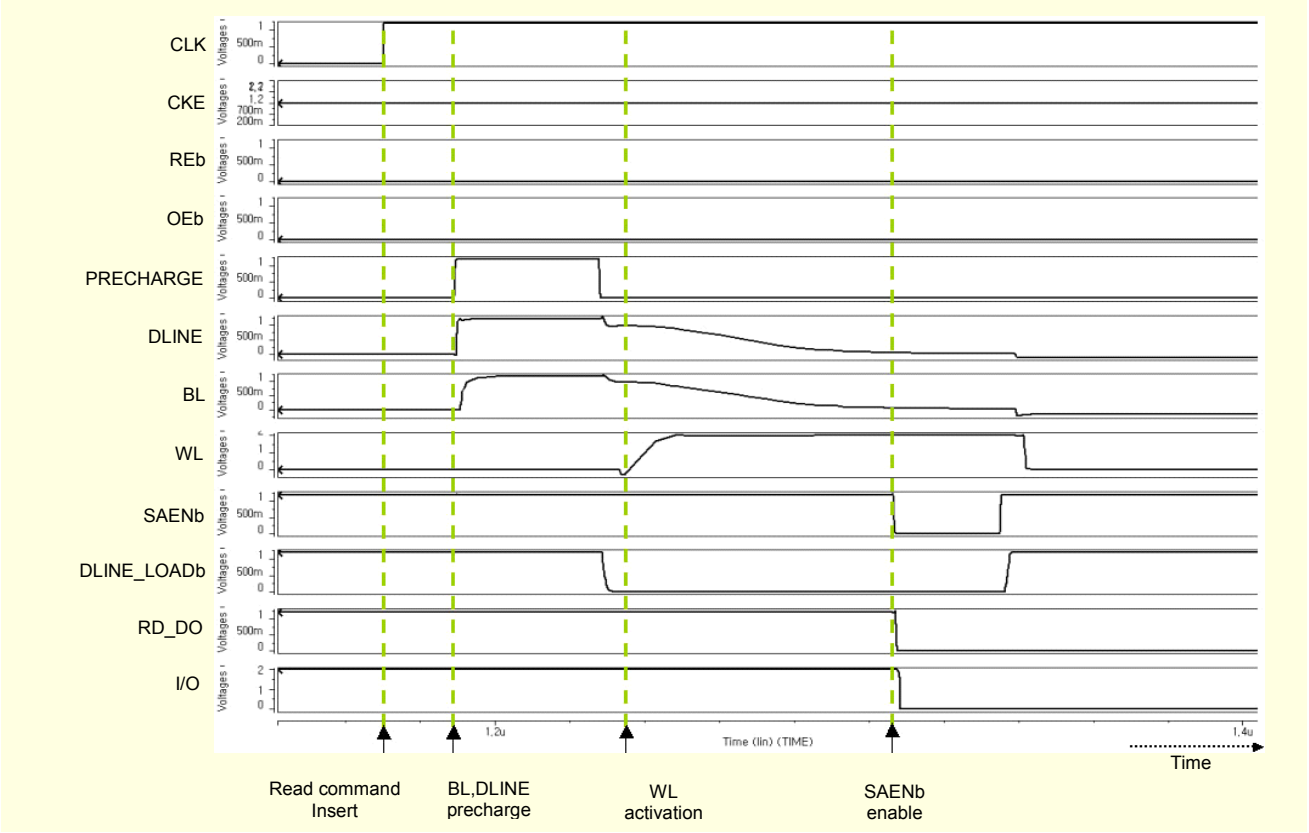

Fig. 10. Timing diagram for the case of critical path in the read cycle.

For this reason, a low-power voltage-up converter circuit is used to boost VREF, which can guarantee the reference voltage, VREF_VPP. Power dissipation can be lower when the voltage converter is used compared to using only a VDDP power source.

Figure 8 shows a voltage-up converter circuit which doubles the VREF in the reference voltage generator [8]. It generates the input voltage of the VPP level detector. The voltage-up converter consists of a differential amplifier, a common source amplifier, and a voltage divider using PMOS diodes. Identical PMOS diodes, MP2 and MP3, make up a voltage divider. The feedback voltage (VFB) is set to half of VREF_VPP. When VREF and VFB are equal by negative feedback, VREF_VPP makes VREF double.

The RD_DO data voltage swings between VDD and VSS. The I/O data voltage swings between VDDP and VSS. If the I/O voltage swings between VDD and VSS, it induces a short circuit in the adjacent block connected to I/O signal because it swings between VDDP and VSS. For this reason, the VDD-to-VDDP voltage-level translator shown in Fig. 9 is needed for the I/O interface.

The Dickson charge pump generates VPP and VPPL in the write mode. It has lower power dissipation by using the lower forward bias diode voltage drop. For this reason, a Schottky diode is used for the pump. Table 5 compares the power dissipation of the Dickson charge pump using a PN diode and using a Schottky diode in the program mode. The power dissipation using a Schottky diode is approximately 12% lower than that using a PN diode.

III. Simulation and Test Results

The EEPROM is designed using the 0.25 μm EEPROM process for UHF RFID tag chips. Figure 10 shows timing diagrams of CLK from the analog block; command control signals CKE, REb, and OEb from the logic block; and PCHARGE, DLINE_LOADb, and SAENb from the control logic block as shown in Fig. 2. When a read command enters at the rising edge, PCHARGE makes DLINE and BL precharge to VDD. The WL is active after the BL is precharged. When data is transferred to the BL, valid data comes out of the I/O by SAENb through the RD_DO within half a clock period.

Figure 11 shows a layout image for the 0.25 μm EEPROM process. The areas of the analog, logic, and cell array are marked. The layout size is 449.3 μm × 480.67 μm. Figure 12 shows an image of the fabricated EEPROM.

Figure 13 is a shmoo plot of the fabricated EEPROM. Functions are tested by performing the read cycle after the erase cycle and the read cycle after the program cycle, using

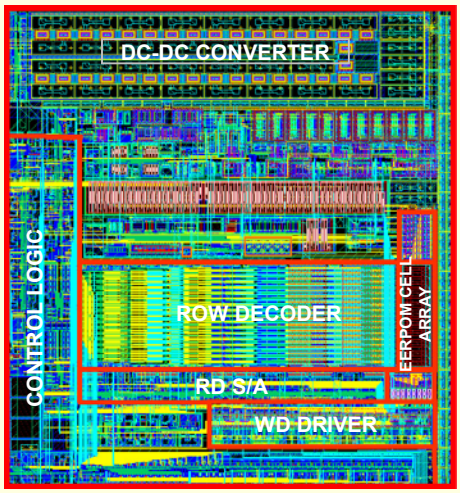

Fig. 11. EEPROM layout.

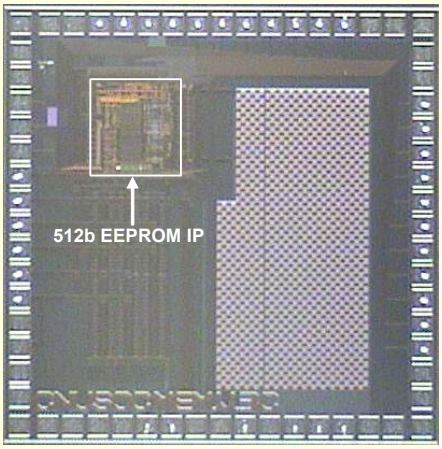

Fig. 12. Image of the fabricated EEPROM IP.

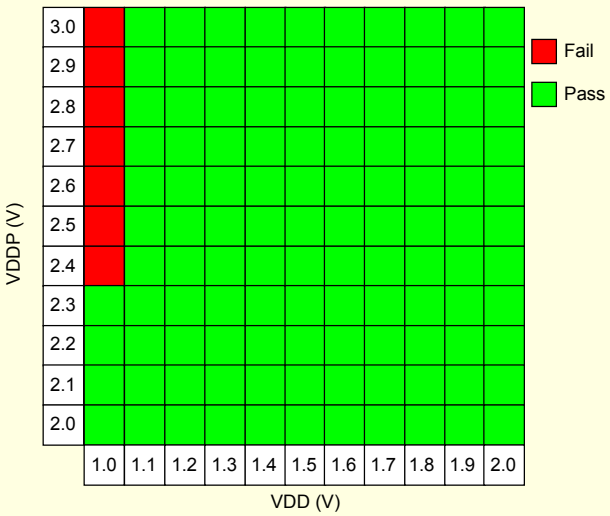

Fig. 13. Shmoo plot of the fabricated EEPROM.

Table 6. Power dissipation results at VDD=1.5 V, VDDP=2.5 V, and Temp=25℃.

Operating mode		Operating current	Dissipated power
Erase	VDD	24.7 μA	61.1 μW
	VDDP	9.6 μA	
Program	VDD	23.4 μA	78.1 μW
	VDDP	17.2 μA	
Read	VDD	16.8 μA	28.7 μW
	VDDP	1.4 μA	

the timing diagrams of Figs. 4 and 5. All cases are passed except at VDD=1.0 V. This means that the EEPROM has a wide operation margin.

Table 6 shows power dissipation test results for different operating modes. The results show that the designed 512-bit EEPROM is suitable for RFID tag chip memory applications.

IV. Conclusion

In this paper, the design of a low-power 512-bit synchronous EEPROM with EEPROM cells for a passive UHF RFID tag chip was presented. Dual power supply voltage, VDD (1.5 V) and VDDP (2.5 V), was used to reduce the current and the power in the read and write modes. Also, a sensing method using clocked inverter in the read mode was applied. The VREF_VPP was made by using a voltage-up converter in the write cycle. A level translator was applied to the I/O interface to reduce short circuiting. A Schottky diode was used for lower power dissipation in the Dickson charge pump.

We demonstrated that the EEPROM fabricated with a 0.25 μm EEPROM process has a wide operation margin and low power dissipation of 78.1 μW in the program mode, 61.11 μW in the erase mode, and 28.7 μW in the read mode. The proposed EEPROM is suitable for UHF RFID class 1 generation 2 tag chip applications.

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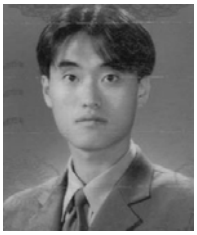

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