

3.5-Inch QCIF AMOLED Panels with Ultra-low-Temperature Polycrystalline Silicon Thin Film Transistor on Plastic Substrate

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In this paper, we describe the fabrication of 3.5-inch QCIF active matrix organic light emitting display (AMOLED) panels driven by thin film transistors, which are produced by an ultra-low-temperature polycrystalline silicon process on plastic substrates. The over all processing scheme and technical details are discussed from the viewpoint of mechanical stability and display performance. New ideas, such as a new triple-layered metal gate structure to lower leakage current and organic layers for electrical passivation and stress reduction are highlighted. The operation of a 3.5-inch QCIF AMOLED is also demonstrated.

Keywords: AMOLED, flexible, poly-Si, thin film transistor (TFT).

I. Introduction

Flexible displays are currently the subject of great interest due to their low weight, superior compactness, robustness, and design flexibility compared with conventional glass-based displays. To realize a mechanically stable display, however, several issues must be resolved [1]. Inorganic materials have very different mechanical properties than plastic substrates. In particular, the thermal expansion coefficients of plastic substrates are much larger than those of inorganic materials and consequently, stresses are introduced during the deposition process. Furthermore, film cracking and delamination may occur during the fabrication process and in operation.

If a freestanding substrate is employed, the curvature of the inorganic film structures on plastic substrates changes during circuit fabrication, causing misalignment between the layers. In order to prevent this misalignment, the plastic substrate is typically bonded to a rigid carrier. The adhesive used for bonding must withstand the thin film transistor (TFT) processing temperatures and chemicals; therefore, the use of an adhesive necessitates a reduction of the maximum process temperature from the value that the substrate itself would normally withstand. These issues and the low thermal resistance of most plastic substrates necessitate a low-temperature process. In addition, to drive an active matrix organic light emitting display (AMOLED) unit, devices with high mobility are required. For such requirements, an ultra-low-temperature poly-Si (ULTPS) TFT appears to be an appropriate choice for device fabrication. [2]-[7].

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The crystallization of sputter deposited a-Si films has been achieved by either excimer laser annealing [2]-[6] or sequential lateral solidification (SLS) [7]. Recently, we reported a successful SLS on a plastic substrate, which yielded micron-size large-grain poly-Si films [8]. To prevent damage to the plastic substrates during the laser dopant activation, a quarter wavelength Bragg reflector, made by successive depositions of plasma-CVD silicon dioxide and silicon nitride film [5], and the oxide-silicon-oxide (SiO₂-Si-SiO₂) buffer structure [9] was suggested.

For gate dielectrics, chemical vapor deposition SiO₂ [2], [4]-[6], sputter deposition SiO₂ [4], and plasma enhanced atomic layer deposition (PEALD) Al₂O₃ films [7], [10]-[12] have been reported. A two-layer gate insulator composed of a plasma oxidized SiO₂ and PEALD Al₂O₃ on a plastic substrate [12] shows high quality characteristics.

In this work, we present the key process and technological approaches for integrating a 3.5-inch QCIF AMOLED panel with ULTPS TFT on a plastic substrate.

II. Experimental Details

Figure 1 shows an optical microscopy image of a unit cell which was fabricated on a plastic substrate. The inset shows the OLED driving circuit, which has two TFTs. The unit cell is designed with a 10 μm design rule and is produced with five mask processes. An interlayer dielectric film is used as a capacitor which allows us to eliminate two mask processes. The unit cell size is 390 μm × 390 μm and is composed of two TFTs and one capacitor structure.

In this work, we used polyarylate (PAR) plastic substrates. Unless supported by a rigid flat support, flexible plastic substrates are always bent to have some finite curvature. Such curvature imposes great difficulty in achieving correct pattern

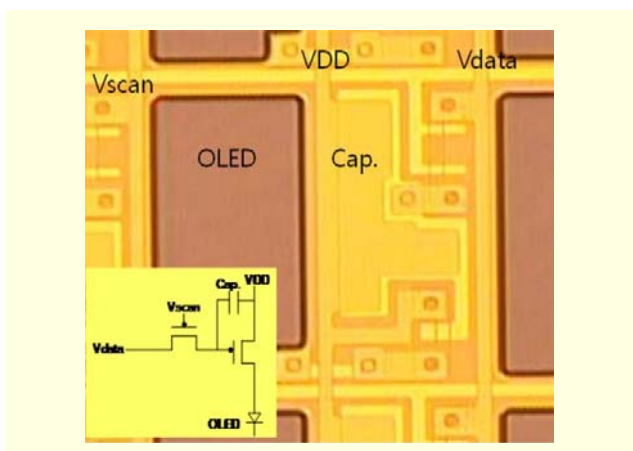


Fig. 1. Optical microscopy image of a unit cell. The inset shows the OLED driving circuit, which has two TFTs.

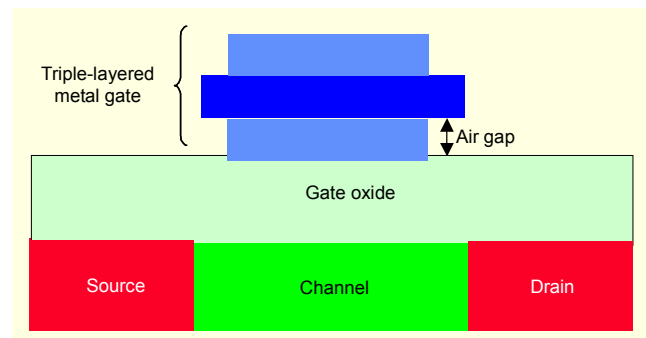


Fig. 2. Schematic TFT structure of triple-layered metal gate with Al (20 nm)/Cr (20 nm)/Al (150 nm).

alignment and uniformity in deposition. For this reason, we bonded the plastic substrate on a rigid glass carrier to ensure processing stability. The carrier has the geometry of a 5-inch wafer. The PAR substrate was attached to the glass carrier wafer with an adhesive having a peel strength of 600 gf/inch. The peel strength was optimized to be neither too weak to allow the delamination of the substrate nor too strong to make the final detachment of the plastic substrate from the glass carrier difficult. In the final step the plastic substrate was detached from the glass carrier by using solvents and heat to decompose the adhesive.

On the plastic substrate, a triple-layered buffer layer was deposited by a sputtering method. The buffer layer has a structure of oxide-silicon-oxide (SiO₂-Si-SiO₂). In our previous work, we have shown the usefulness of such a triple-layered buffer structure in preventing plastic damage which is induced during the laser activation process [9]. The thickness and deposition temperature are important to prevent the film cracking during the gate oxide deposition. After forming the buffer layer, an 80 nm thick amorphous Si film was deposited and crystallized by a sequential lateral solidification method [8].

The gate dielectric layer was formed by a PEALD method. Prior to the oxidation, the surface of the Si substrate was cleaned with a 100:1 hydrofluoric (HF) acid solution to remove the native oxide layer. We attempted to oxidize the Si surface with a pulsed O₂ plasma at an RF frequency of 13.56 MHz and a power of 0.41 W/cm² for 30 min in the PEALD chamber. A gate dielectric Al₂O₃ film containing nitrogen (< 1%) was deposited in situ with the O₂ gas mixed with N₂ gas as the oxidants and trimethylaluminum as the source of Al [11]. The plasma oxidized film and Al₂O₃ film are 5 nm and 70 nm thick, respectively.

The off leakage of LTPS TFT has already been studied and interpreted as a field enhanced thermionic emission. To reduce the leakage current, a lightly doped drain (LDD) structure was used on the glass substrate. However, on a plastic substrate, an LDD structure is not suitable because of the misalignment

issue due to the thermal deformation of the plastic substrate. Therefore, we developed a triple-layered metal gate structure as shown in Fig. 2, which is effective in reducing the electric field at the gate edge by a self-alignment method. We deposited metals in three layers: Al (20 nm)/Cr (20 nm)/Al (150 nm). After gate photo-lithography, the gate metals were sequentially wet-etched. The bottom Al was over-etched to make an air gap near the gate edge with a lateral depth of 100 nm. Although the air gap thickness is only 20 nm, if we compare it with the dielectric constant of Al₂O₃ film of 6.5, the vertical electric field will be reduced according to the air gap's effective thickness of 130 nm.

The top aluminum layer, which has a high reflectivity, is required to prevent metal gate damage during the laser activation. After the patterning of the gate electrode, the p+ source and drain (S/D) regions were formed and laser activated.

Because ductile organic materials can endure more stress than inorganic materials, an acryl-resin-based organic material was chosen for the interlayer dielectric (ILD) layer. However, two problems must be resolved for the application of an organic ILD layer in our device fabrication scheme. The first problem is the thermal budget issue. Forming a hard cured film usually requires a baking temperature over 200°C, which is too high for both the plastic substrate and the adhesive. The second problem is the chemical resistance issue. The ILD layer is exposed to the 100:1 HF acid during the wet etching of the gate dielectric Al₂O₃ film to establish electrical contacts. Therefore, we developed a new material for low temperature hard curing below 120°C.

Figure 3(a) shows an optical microscope image and an atomic force microscope (AFM) image of an organic ILD layer which was exposed to a 100:1 HF acid solution. The surface has many small defective dots which, as the AFM scan result shows, turn out to be swelling traces of the organic film. The swellings are an average of 30 μm in diameter and 15 nm in height. Because the S/D layer is used in addition to an anode layer, the swelling of the ILD layer induces surface roughness on the anode layer, which deteriorates the organic light emitting device (OLED) performance.

To suppress the appearance of damages induced by HF acid and to lower the curing temperature, we increased the content of the cross-linker. Figure 3(b) shows the surface morphology of the improved organic ILD, which was cured at 120°C, after being exposed to a 100:1 HF solution. As seen in the figure, the film is fairly stable against the HF solution.

Because the gate oxide layer, AlON, is hydrophilic, but the organic ILD layer is hydrophobic with a contact angle of 75 degrees, the interface between the gate oxide layer and the organic ILD layer is easily separated by the 100:1 HF solution. Therefore, the 10 nm gluing layer of silicon nitride is inserted

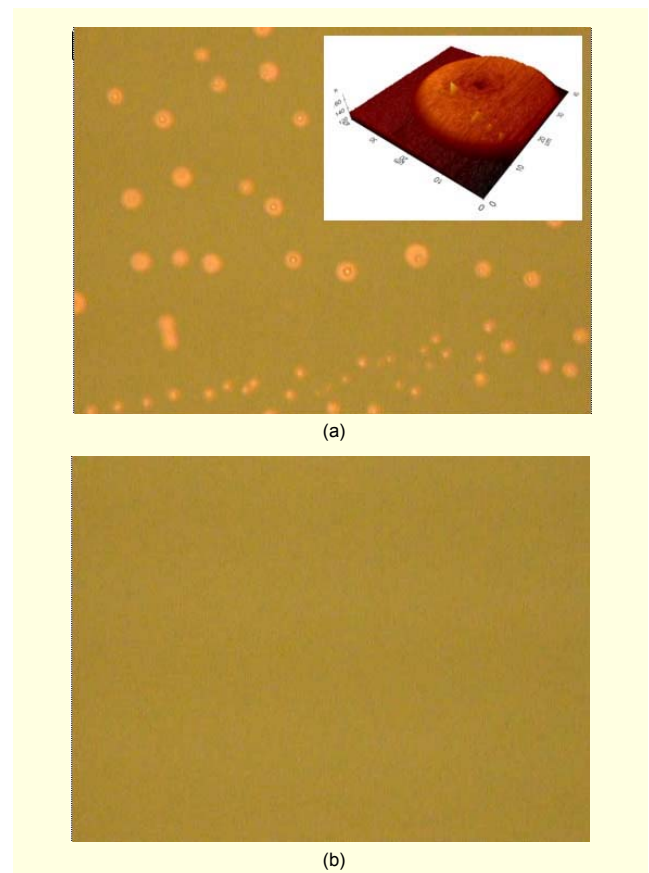


Fig. 3. Optical microscope image of the 100:1 HF solution damaged surface of the organic dielectric layer (a) before improvement (inset is an AFM image) and (b) after improvement.

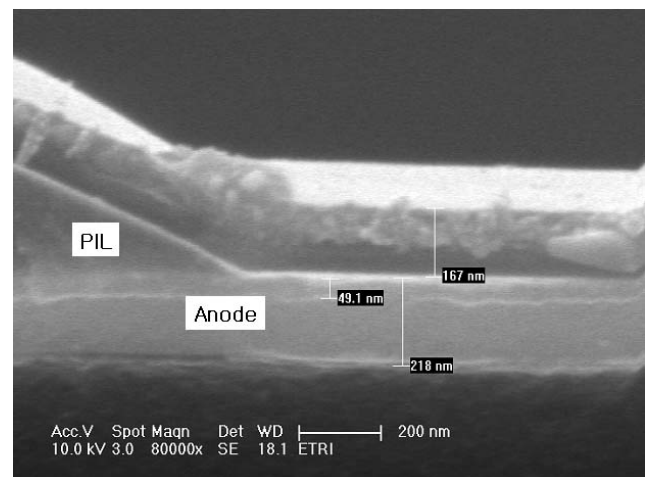


Fig. 4. SEM image of the photoactive insulating bank layer.

between them.

The S/D metal layers, which were deposited by a DC sputtering method, consist of a 10 nm thick Cr film, a 200 nm thick Al film, and a 10 nm Cr film. The bottom Cr metal is

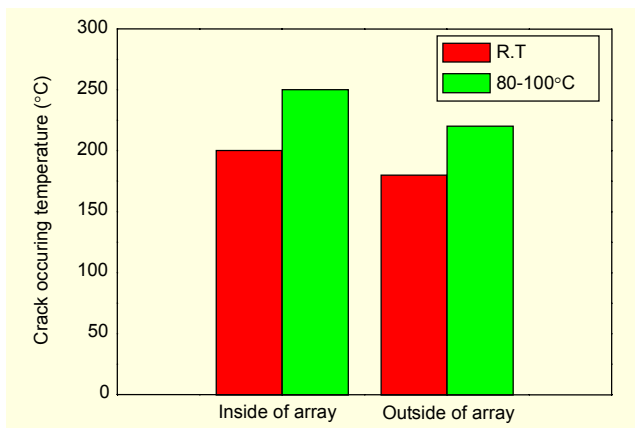


Fig. 5. Effect of sputtering temperature on the cracking temperature, above which the buffer layer is cracked. The layer endurance against thermal cracking is improved by increasing the sputtering temperature.

used for the adhesion promotion layer, and the top Cr metal is used as a matching layer to the hole injection layer of OLED film. The bank layer is made of the photoactive insulating layer (PIL) as shown in Fig. 4. By using a thick PIL layer of more than 3 μm , it was possible to prevent the occurrence of an electrical short circuit between the anode and the cathode. The slope of the bank was intentionally lowered to achieve uniform OLED evaporation at the bank edge, which is necessary to reduce the OLED leakage current.

The device structure of an OLED grown by vacuum thermal deposition is 2-TNATA (10 nm)/a-NPB (30 nm)/A1q:C545T (30 nm)/A1q (30 nm). The transparent cathode metal is composed of LiF (1 nm)/Al (1 nm)/Ag (15 nm). The bi-layer of a-NPB and LiF deposited by thermal evaporation and some inorganic layers, including AlOx grown by ALD, were used for thin film encapsulation [13].

A JEOL 6500F Schottky-type field-emission gun scanning electron microscope equipped with an Oxford INCA Crystal electron backscattered diffraction (EBSD) system was used to characterize the crystallized poly-Si thin film on the plastic substrate.

III. Results and Discussion

The thermal expansion coefficient of the plastic substrate is much larger than those of inorganic materials. Thus, the buffer layer which is in contact with the plastic substrate is expected to experience the most severe tensile stress during any subsequent processes accompanied by heat. Because the poly-Si film deposited on the buffer was already patterned into micron-sized discrete features, the stress transfer through the poly-Si was negligible. During the subsequent processes, the cracks in the buffer layer mainly occurred during the gate oxide

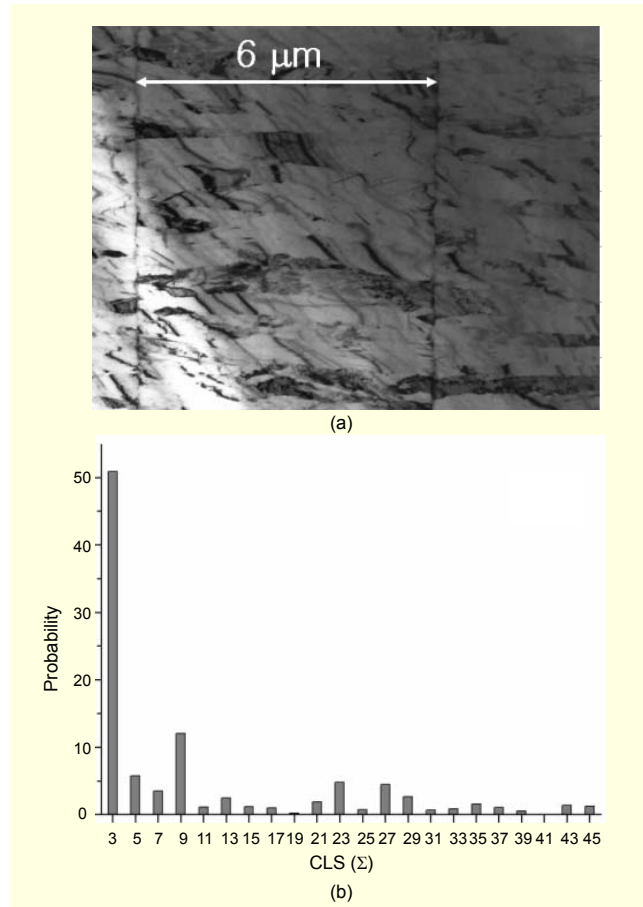


Fig. 6. (a) TEM image of polycrystalline Si, which was obtained by laser crystallization and (b) CSL distribution of Si grains.

step, during which the processing temperature ranged from 150°C to 180°C. To reduce the stress on buffer layer, we varied the sputtering temperature of the buffer layer [14].

Figure 5 summarizes the effect of the deposition temperature on the cracking temperature, above which cracking in buffer layer is observed. Compared to room temperature deposition, by depositing buffer layers at around 100°C, it was possible to increase the cracking temperature by approximately 30°C to 50°C.

Figure 6(a) shows a transmission electron microscopy (TEM) of poly-Si grains, which are about 6 μm long. To obtain the grain boundary (GB) characters of such grains, we obtained Kikuchi patterns using an EBSD facility. Figure 6(b) shows the statistical distribution of the coincidence site lattice (CLS) or Σ , which represents the reciprocal density of the sites shared by two adjoining grains. The CLS distribution reveals that $\Sigma 3$ and $\Sigma 9$ occupy the first and second appearance probability. Because such coherent GBs have low density of dangling bonds and charge trap sites, our poly-Si is expected to have high mobility.

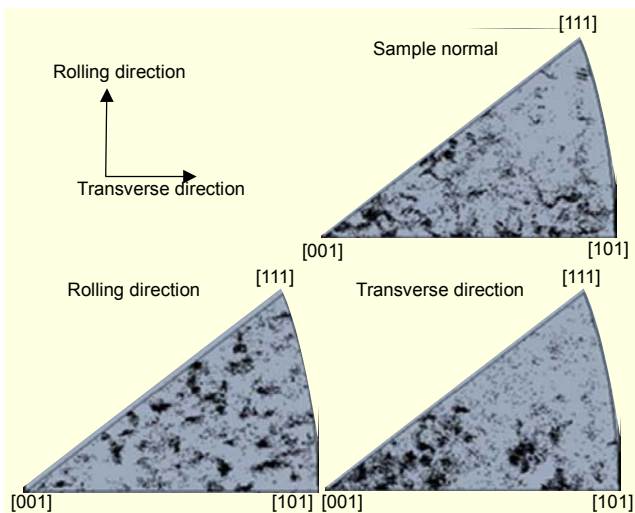


Fig. 7. Inverse pole figures of poly-Si. The transverse direction bears texture preference along [001].

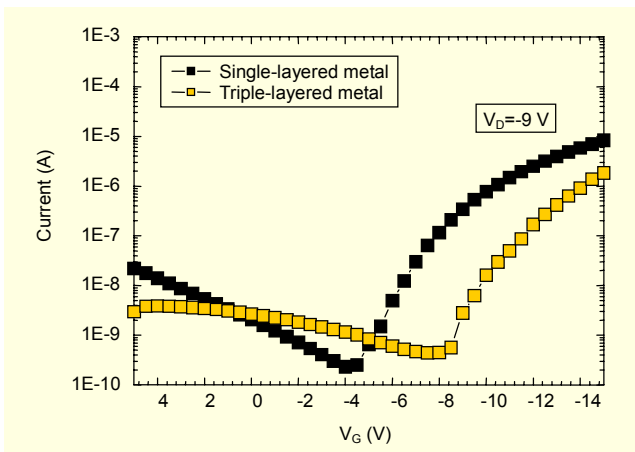


Fig. 8. Performances of TFTs with single- and triple-layered metal gate. Triple-layered TFT shows better drain leakage performance.

Figure 7 shows the inverse pole figures of surface normal, rolling, and transverse directions. Whereas the normal and the rolling directions did not bear any strong preferential texture, the transverse tended to have a $\langle 100 \rangle$ preference. The preferential growth in $\langle 100 \rangle$ reflects the fact that the advancing solidification front of the diamond cubic is [100], which has been interpreted as the facility in atom bonding to complete the relevant plane [15].

The TFT characteristics of the single-layered metal gate and the triple-layered metal gate TFTs are compared in Fig. 8 and are summarized in Table 1. Although the threshold voltage of the triple-layered metal gate TFT is increased by 3 V, the leakage current is reduced by one order of magnitude at $V_G = 5$ V. Furthermore, considerable decrement in the rate of leakage current ($\partial \log I_D / \partial V_G$) is observed, indicating improved

switching characteristics. In conjunction with this feature, because the leakage current of poly-Si TFTs mainly originates from the electric field, our triple gate TFTs give a lower electrical field at the gate edge.

The capacitance characteristics of the organic interlayer dielectric film as a function of frequency are shown in Fig. 9. The dielectric constant is fairly uniform in a frequency range from 10^3 Hz to 10^6 Hz as 3.16. Although the curing

Table 1. Threshold voltage, swing, mobility, and rate of leakage current of $W/L = 30 \mu\text{m} / 30 \mu\text{m}$ TFT according to gate metal structure variation.

Gate metal structure	Threshold (V)	Swing (V/dec)	Mobility (cm^2/Vs)	$\frac{\partial \log I_D}{\partial V_G}$ (dec/10 V)
Single layer	-5.5	0.99	6.9	2.1
Triple layer	-8.5	1.03	4	0.5

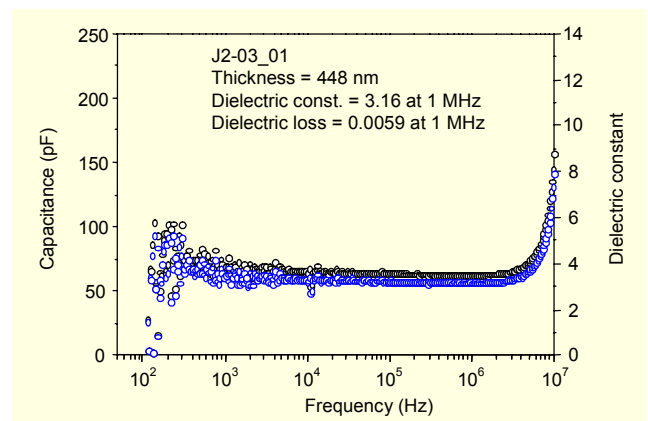


Fig. 9. Capacitance characteristics of the organic interlayer dielectric film.



Fig. 10. Operation of a 3.5-inch QCIF AMOLED panel on plastic substrate driven by LTPS TFTs with the mosaic pattern. The inset shows the panel driven to display an "8".

temperature of the organic interlayer dielectric film is below 120°C, the leakage current is below 1E-8 A/cm² at 1 MV/cm.

Based on this approach, we fabricated LTPS TFT panels on plastic substrates and integrated them to AMOLED display units. Figure 10 shows a 3.5-inch QCIF AMOLED panel operating with the mosaic pattern. The inset shows the panel driven to display an “8”. Even though many technical issues are challenges for the full operation of our LTPS TFT-AMOLED, we have demonstrated the feasibility of the LTPS TFT-AMOLED concept. We will develop a better display by reducing the defects, improving the TFT performance with triple-layered metal gate, and optimizing the operating voltages of the control board.

IV. Summary

A 3.5-inch QCIF flexible display unit was fabricated by integrating an LTPS-TFT array to an AMOLED panel on a plastic substrate, and its operation was demonstrated.

We have endeavored to improve the electrical characteristics of LTPS-TFTs. Poly-Si devices, especially those fabricated at low temperatures, suffer from high-level leakage currents. To reduce the TFT leakage current, we have developed a triple-layered metal gate structure, in which the bottom layer is laterally over-etched to have an air gap. Because no special lithographic technique is required, the misalignment issue is easily avoided in constructing the triple-layered gate metal structure.

Because tensile stress is accumulated by addition of layers, reducing the number of photo masking processes is always desirable. This issue was dealt with by developing a low temperature (120°C) curable organic ILD, which has an electrical insulating property sufficient for it to be used as a capacitor. We were also successful in eliminating two masking steps.

To obtain high mobility, which is a prerequisite to drive an OLED, Si films were crystallized by an SLS method to obtain 6 μm poly-Si grains on plastic substrates. The grain boundaries of poly-Si were characterized by EBSD to have high coherency with low density of dangling bonds.

References

- [1] S. Wagner, H. Gleskova, I-C. Cheng, J.C. Sturm, and Z. Suo, “Mechanics of TFT Technology on Flexible Substrates,” *Flexible Flat Panel Displays*, G.P. Crawford (ed.), West Sussex, England: John Wiley & Sons Ltd., 2005, pp. 263-282.
- [2] D.P. Gosain, T. Noguchi, and S. Usui, “High Mobility Thin Film Transistors Fabricated on a Plastic Substrate at a Processing Temperature of 110°C,” *Jpn. J. Appl. Phys. Part 2*, vol. 39, 2000, pp. L179-L181.
- [3] T. Serikawa and F. Omata, “High-Mobility Poly-Si Thin Film Transistors Fabricated on Stainless-Steel Foils by Low-Temperature Processes Using Sputter-Depositions,” *Jpn. J. Appl. Phys. Part 2*, vol. 39, 2000, pp. L393-L395.
- [4] P.G. Carey, P.M. Smith, S.D. Theiss, and P. Wichboldt, “Polysilicon Thin Film Transistors Fabricated on Low Temperature Plastic Substrates,” *J. Vac. Sci. Technol.*, vol. A17, 1999, pp. 1946-1949.
- [5] F. Lemmi, W. Chung, S. Lin, P.M. Smith, T. Sasagawa, B.C. Drews, A. Hua, J.R. Stern, and J.Y. Chen, “High-Performance TFTs Fabricated on Plastic Substrate,” *IEEE Electron Device Lett.*, vol. 25, 2004, pp. 486-488.
- [6] J.Y. Kwon, D.Y. Kim, H.S. Cho, K.B. Park, J.S. Jung, J.M. Kim, Y.S. Park, and T. Noguchi, “Low Temperature Poly-Si Thin Film Transistor on Plastic Substrates,” *IEICE Trans. Electron.*, vol. E88-C, 2005, pp. 667-671.
- [7] Y.H. Kim, C.Y. Sohn, J.W. Lim, S.J. Yun, C.S. Hwang, C.H. Chung, Y.W. Ko, and J.H. Lee, “High-Performance Ultra-Low-Temperature Polycrystalline Silicon Using Sequential Lateral Solidification,” *IEEE Electron Device Lett.*, vol. 25, 2004, pp. 550-552.
- [8] Y.H. Kim, C.H. Chung, S.J. Yun, J. Moon, D.J. Park, D.W. Kim, J.W. Lim, Y.H. Song, and J.H. Lee, “Large Grain Polycrystalline Silicon Film by Sequential Lateral Solidification on a Plastic Substrate,” *Thin Solid Films*, vol. 493, 2005, pp. 192-196.
- [9] Y.H. Kim, C.H. Chung, J. Moon, G.H. Kim, D.J. Park, D.W. Kim, J.W. Lim, S.J. Yun, Y.H. Song, and J.H. Lee, “Oxide-Silicon-Oxide Buffer Structure for Ultra-Low Temperature Polycrystalline Silicon Thin Film Transistor on Plastic Substrate,” *IEEE Electron Device Lett.*, vol. 27, 2006, pp. 579-581.
- [10] J.W. Lim, S.J. Yun, Y.H. Kim, C.Y. Sohn, and J.H. Lee, “Investigation of a Two-Layer Gate Insulator Using Plasma-Enhanced ALD for Ultralow Temperature Poly-Si TFTs,” *Electrochem. Solid-State Lett.*, vol. 7, 2004, pp. G185-G187.
- [11] J.W. Lim and S.J. Yun, “Electrical Properties of Alumina Films by Plasma-Enhanced Atomic Layer Deposition,” *Electrochem. Solid-State Lett.*, vol. 7, 2004, pp. F45-F48.
- [12] Y.H. Kim, J. Moon, C.H. Chung, S.J. Yun, D.J. Park, J.W. Lim, Y.H. Song, and J.H. Lee, “Performance Improvement of Ultralow Temperature Polycrystalline Silicon TFT on Plastic Substrate by Plasma Oxidation of Polycrystalline Si Surface,” *IEEE Electron Device Lett.*, vol. 27, 2006, pp. 896-898.
- [13] S.H.K. Park, J. Oh, C.S. Hwang, J.I. Lee, Y.S. Yang, and H.Y. Chu, “Ultrathin Film Encapsulation of an OLED by ALD,” *Electrochem. Solid-State Lett.*, vol. 8, 2005, pp. H21-H23.
- [14] Y. Leterrier, L. Medico, F. Demarco, J.A.E. Manson, U. Betz, M.F. Escola, M. Kharrazi Olsson, and F. Atamny, “Mechanical Integrity of Transparent Conductive Oxide Films for Flexible

Polymer-Based Displays,” *Thin Solid Films*, vol. 460, 2004, pp. 156-166.

- [15] R. Drosd and J. Washburn, “Some Observations on the Amorphous to Crystalline Transformation in Silicon,” *J. Appl. Phys.*, vol. 53, 1982, pp. 397-403.



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