

A 40 Gb/s Clock and Data Recovery Module with Improved Phase-Locked Loop Circuits

Hyun Park, Kang Wook Kim, Sang-Kyu Lim, and Jesoo Ko

A 40 Gb/s clock and data recovery (CDR) module for a fiber-optic receiver with improved phase-locked loop (PLL) circuits has been successfully implemented. The PLL of the CDR module employs an improved D-type flip-flop frequency acquisition circuit, which helps to stabilize the CDR performance, to obtain faster frequency acquisition, and to reduce the time of recovering the lock state in the event of losing the lock state. The measured RMS jitter of the clock signal recovered from 40 Gb/s pseudo-random binary sequence ($2^{31}-1$) data by the improved PLL clock recovery module is 210 fs. The CDR module also integrates a 40 Gb/s D-FF decision circuit, demonstrating that it can produce clean retimed data using the recovered clock.

Keywords: Phase-locked loop, clock and data recovery, CDR, clock recovery, fiber-optic communication system, 40 Gb/s.

I. Introduction

Ever-growing demands for ultra-broadband data communications has led to many studies on 40 Gb/s fiber-optic transmission systems [1]. One of the key components in such a transmission system is the clock and data recovery (CDR) circuit, which recovers the clock signal from the input binary signal and retimes the distorted data.

The CDR module can be implemented either in the form of a monolithic circuit [1] or a hybrid microwave integrated circuit module [2]-[5]. In addition, the CDR module can be categorized according to the method of recovering the clock as either open-loop type [2] or phase-locked loop (PLL) type [3]-[6]. The practical design and implementation method of the CDR module for 40 Gb/s optical communication systems, however, is still in progress and is being actively investigated worldwide.

We previously reported the implementation of a low-cost 40 Gb/s PLL clock recovery (CR) module, which used a frequency acquisition circuit based on a D-type flip-flop (D-FF) circuit [6]. In this paper, however, the D-FF-based frequency acquisition circuit is further improved, and a decision circuit is integrated with the CR module to form a compact CDR module. In addition, a detailed description of operation principles for the frequency acquisition circuit is given. Previously, circuits employing D-FFs were used in PLLs [7], [8]. The D-FF circuit presented in [8] acquired the frequency in a PLL by directly comparing the phases of the data and clock, while the D-FF circuit proposed in this paper utilizes the phase polarity of the down-converted I and Q signals depending on the frequency difference of the data and clock signals. In comparison with the conventional frequency acquisition circuits implemented with a frequency sweep

Manuscript received Aug. 13, 2007; revised Jan. 07, 2008.

This work was supported by the IT R&D program of MIC/IITA, Rep. of Korea (2006-S060-02, OTH-based 40G Multi-service Transmission Technology).

Hyun Park (phone: + 82 53 939 3211, email: hyun@em-wise.com) is with EM-Wise Communications Co., Daegu, Rep. of Korea.

Kang Wook Kim (phone: + 82 53 950 5510, email: kang_kim@ee.knu.ac.kr) is with the Department of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, Rep. of Korea.

Sang-Kyu Lim (email: sklim@etri.re.kr) and Jesoo Ko (email: jsko@etri.re.kr) are with Optical Communications Research Center, ETRI, Daejeon, Rep. of Korea.

circuit [9] or an IF mixer circuit [10], the frequency acquisition circuit proposed in this paper provides better stability, faster frequency acquisition, and faster recovery time when the clock recovery circuit loses the locking state.

This paper describes the circuit configurations of the 40 Gb/s CDR module, including the principle of the improved frequency acquisition circuit, and provides the experimental results.

II. Circuit Configurations of the CDR Module

Figure 1 shows a typical configuration of a 40 Gb/s fiber-optical receiver. A photodiode (PD) converts a 40 Gb/s optical signal into an electrical signal, which is amplified before it is applied to the CDR. The clock signal recovered by the CR circuit is applied to the decision circuit in order to retime the distorted data and is then applied to the demultiplexer.

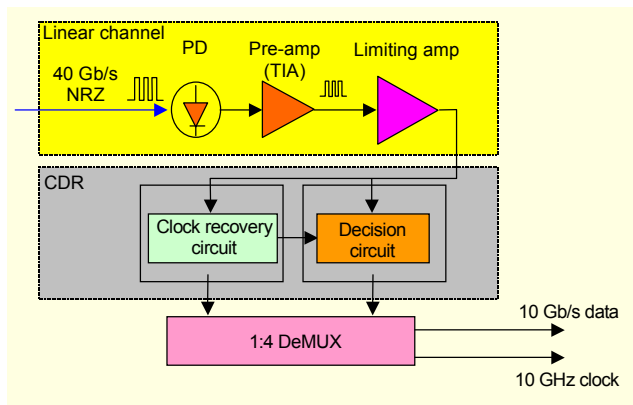


Fig. 1. Block diagram of a typical 40 Gb/s fiber-optic receiver.

The function of a CR circuit is to extract the clock signal component from NRZ input data. Typically, the CR circuit consists of a nonlinear circuit block, a filter block, and an amplifier block. The nonlinear circuit enables extraction of the clock component from an NRZ signal that does not have a discrete clock spectrum. For the filtering, the open-loop CR circuit uses a passive high-Q filter, such as a dielectric resonator (DR) filter. The PLL CR circuit utilizes a PLL acting as a very narrowband filter.

The open-loop type CDR has advantages of structural simplicity, cost effectiveness, and low power dissipation, but it also has several drawbacks, including relatively high timing jitter and the inability to maintain the clock signal when the temporary loss of an input signal occurs. The problems with the open-loop CDRs can be solved with the PLL designs [3]-[6]. The proposed CDR module shown in Fig. 2 consists of a clock extractor, two phase detectors, an improved frequency acquisition circuit using a D-FF, a voltage-controlled dielectric resonator oscillator (VC-DRO), a loop filter, two phase shifters, two quadruplers, and a 40 Gb/s D-FF as a decision circuit.

1. Clock Extractor

Figure 3 is a block diagram of the implemented clock extractor circuit [6]. The clock extractor consists of a pre-amplifier, a nonlinear circuit, a bandpass filter, and a clock amplifier. The nonlinear circuit consists of two Schottky diodes and a branch line coupler. It works like a full-wave rectifier to generate the 40 GHz clock spectrum from the 40 Gb/s NRZ signal.

2. Phase-Locked Loop Circuits

As shown in Fig. 2, to stabilize the extracted clock and to

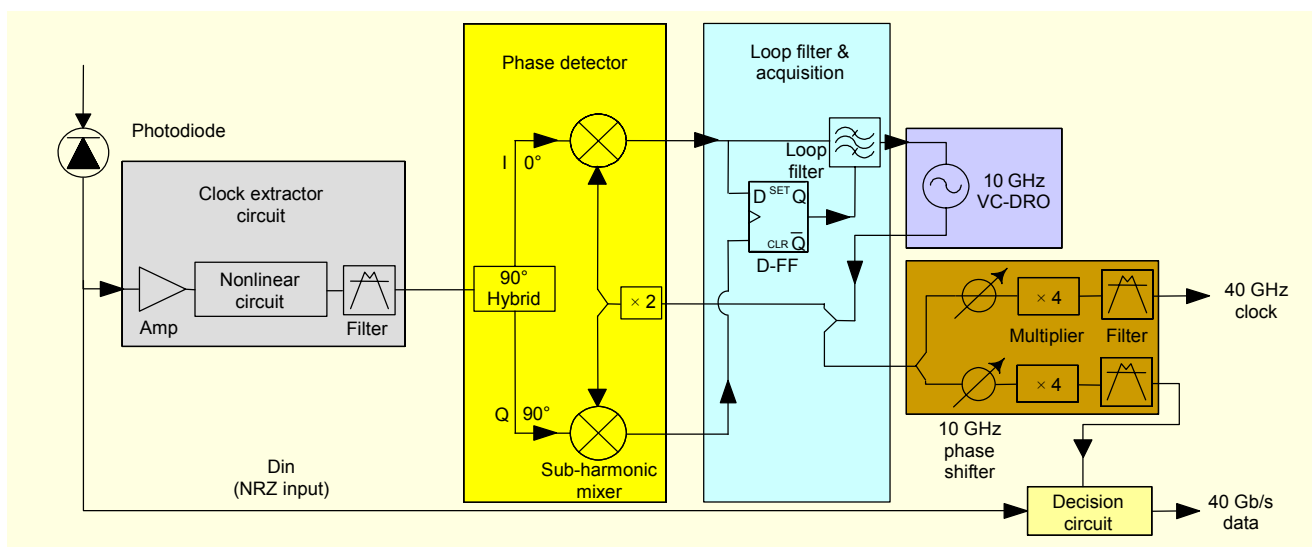


Fig. 2. Block diagram of the proposed PLL CDR.

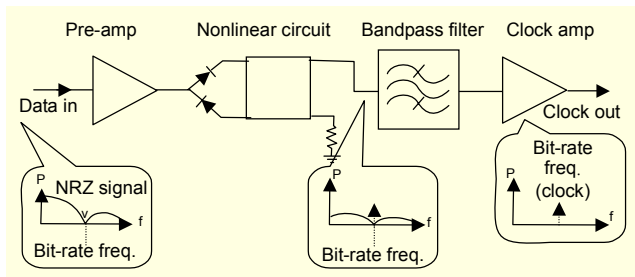


Fig. 3. Block diagram of the clock extractor circuit.

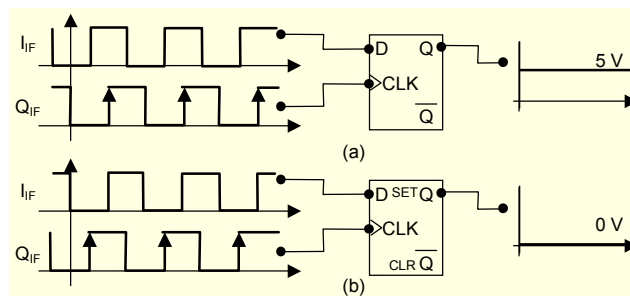


Fig. 5. Frequency detection based on I and Q signals.

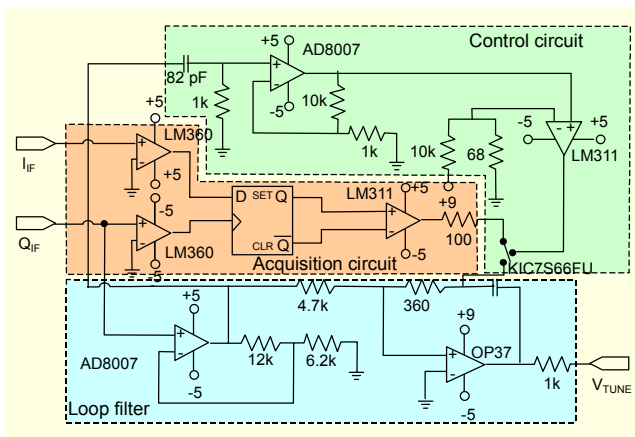


Fig. 4. Schematic of the loop filter and acquisition circuit.

improve the jitter characteristics, a PLL block is used. The extracted 40 GHz clock signal passes through a 90° hybrid coupler, generating I and Q signals. Then, the I and Q signals are mixed in the sub-harmonic mixers with 20 GHz LO signals, which are frequency-doubled from the 10 GHz VC-DRO. These subharmonic mixers serve as phase detectors and work to synchronize the phases when the input (RF) and the doubled LO signals are near the same frequency, that is, within the PLL frequency locking range. The locking range of the phase detector (for example, with the implemented PLL) is approximately given as $K_{VCO} \times V_{lp-p} = 2.7 \text{ (MHz/V)} \times 0.2 \text{ (V)} = 540 \text{ kHz}$, where V_{lp-p} is the peak-to-peak voltage of the I signal, and K_{VCO} is voltage sensitivity of the VC-DRO. In most cases, the frequency of the doubled LO signal, which is four times the VC-DRO output, is out of the lock range; therefore, the phase detector alone cannot provide the phase locking. For this reason, a frequency acquisition circuit is additionally needed for phase locking.

The frequency acquisition circuit utilizing a D-FF circuit was previously presented in [6], but it is further improved in this paper by adding a control circuit for frequency acquisition and replacing a voltage adder by an adaptive switch. The proposed frequency acquisition circuit for PLLs significantly improves the acquisition speed and stability of the PLLs.

Down-converted I_{IF} and Q_{IF} signals, generated by the I and Q mixers, are directed to the acquisition circuit as shown in Fig. 4. Depending on the polarity of the frequency difference between the doubled mixer LO signal and the input signal (signal from the clock extractor), the phase relationship between the I_{IF} and Q_{IF} signals is determined. We define $\Delta\omega = 2\omega_{LO} - \omega_{IN}$, where ω_{IN} is the frequency of the input signal, and ω_{LO} is the frequency of the subharmonic mixer LO signal. If the frequency of the doubled LO signal (four times the VCO signal) is higher than that of the input signal, that is, $\Delta\omega > 0$, the phase of the I_{IF} signal leads by 90° as compared with that of the Q_{IF} signal. On the other hand, if $\Delta\omega < 0$, then the phase of the I_{IF} signal lags by 90°.

By utilizing the phase relationship of the I_{IF} and Q_{IF} signals, which depends on the sign polarity of $\Delta\omega$, the operation principle of the frequency detector can be explained as shown in Fig. 5. If the I_{IF} and Q_{IF} signals are connected to the D-FF, the output of the D-FF is determined depending only on the polarity of the quadrature phase relationship between the I_{IF} and Q_{IF} signals. As shown in Fig. 5(a), if the phase of the I_{IF} signal leads by 90°, that is, $\Delta\omega > 0$, the output of the D-FF becomes +5 V. This is the case when the frequency of the doubled LO signal is greater than that of the RF input signal, and the frequency of the VCO should be reduced. Therefore, this control voltage should subsequently be inverted to -5 V. On the other hand, if $\Delta\omega < 0$, the output of the D-FF becomes 0 V. In this case, the VCO control voltage should subsequently be changed to +5 V in order to increase the VCO frequency. These VCO control voltages are generated by an inverted comparator connected at the output of the D-FF. Therefore, this frequency detector circuit achieves the frequency acquisition by charging and discharging the capacitor in the loop filter with the bipolar VCO control voltages. If $\Delta\omega$ becomes close to zero, then the PLL, consisting of the mixers as phase detectors and the loop filters, is activated to complete the phase-locking.

A control circuit for frequency acquisition shown in Fig. 4 is also implemented. It monitors the frequency of the Q_{IF} signal using a high-pass filter and controls the switch to disconnect the frequency acquisition circuit from the PLL when the input

frequency is located within the lock range ($\Delta\omega \cong 0$). By disconnecting the frequency acquisition circuit from the PLL when $\Delta\omega \cong 0$, unnecessary voltage loading (± 5 V) to the capacitor in the loop filter is eliminated, which enhances the lock stability. Finally, the loop filter block eliminates high frequency components from the VCO control voltage and determines the lock range and transient response of the total PLL.

The improved frequency acquisition circuit provides many advantages over conventional acquisition circuits. A typical frequency acquisition circuit for PLLs is often implemented with a sweep circuit [9]. This frequency acquisition circuit generates a VCO frequency sweep signal, and stops the sweep when it detects a signal indicating that the frequency difference between the input and LO signals is within the locking range. However, this process is very sensitive to the sweep time. If the sweep speed is too fast, the acquisition circuit cannot stop the frequency sweep due to the loop response time of the PLL. Therefore, the fine-tuning of the circuits might be time-consuming. When the lock state is lost due to temporary input signal or environmental changes, the sweep circuit should trigger another frequency sweep, which is a very slow process.

On the other hand, the proposed D-FF-based frequency acquisition circuit possesses its own feedback capability. When the lock status changes, the fast feedback function of the frequency acquisition circuit is activated to restore locking in an instant. The proposed frequency acquisition circuit offers the following advantages. Since the acquisition circuit is controlled by the polarity of the quadrature phase of the I and Q signals, the operation provides better stability in the presence of temperature variations. Also, since the acquisition circuit is a feedback circuit, the time required for frequency detection and acquisition is much faster, and the recovery time after temporary loss of the clock is much shorter.

Also, compared with the frequency acquisition circuit with an IF mixer [10], the proposed acquisition circuit has the

Table 1. Performance comparison of typical frequency acquisition circuits.

	D-FF	IF mixer	Sweep circuit
Lock stability	Excellent	Poor	Poor
Feedback capability	Yes	Yes	No
Acquisition range	Wide (~30 MHz)	Narrow (~1 MHz)	Very wide (Full VCO tune range)
Acquisition speed	Excellent (< 0.5 ms)	Excellent (< 0.5 ms)	Poor (5 ms) [11]
Lock recovery time	Excellent	Excellent	Poor (12 ms)

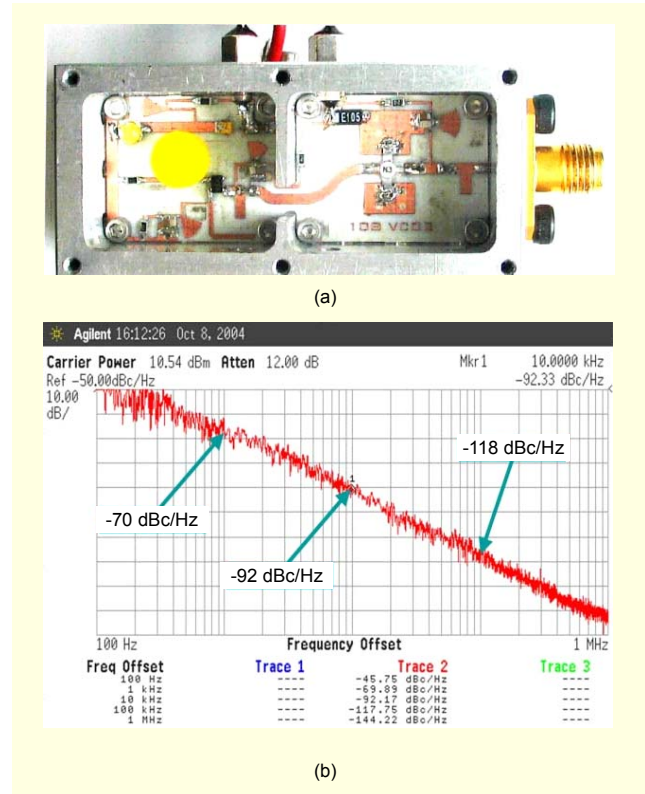


Fig. 6. Implemented VC-DRO: (a) layout and (b) phase noise.

advantages of a broader frequency acquisition range, lower current consumption, much simpler circuit configuration, and more stable frequency acquisition. Table 1 summarizes the performance comparison among different frequency acquisition circuits.

3. 10 GHz VC-DRO

As a stable source, a 10 GHz VCO with a dielectric resonator is implemented. The VC-DRO is tunable using a GaAs hyper-abrupt varactor diode (M/A-Com MA46451-186). The tuning bandwidth is about 10 MHz ($V_R = 1$ to 10 V) at 10 GHz. Figures 7(a) and (b) show the implemented layout of the VC-DRO and the measured result. The output frequency of the VC-DRO is 9.953 GHz, and the output power is 11 dBm. Phase noise at 9.953 GHz is -92 dBc/Hz at 10 kHz offset frequency and -118 dBc/Hz at 100 kHz offset frequency.

4. 10 GHz Reflection-Type Analog Phase Shifter

As a 10 GHz continuous phase-shifter, a hybrid-coupled reflection-type phase shifter is used. The phase shifter consists of a 90° hybrid coupler and two varactors, which change their impedances with change of the control voltage, resulting in the desired phase shift characteristics. The 10 GHz reflection-type analog phase shifter is fabricated using two GaAs flip-chip

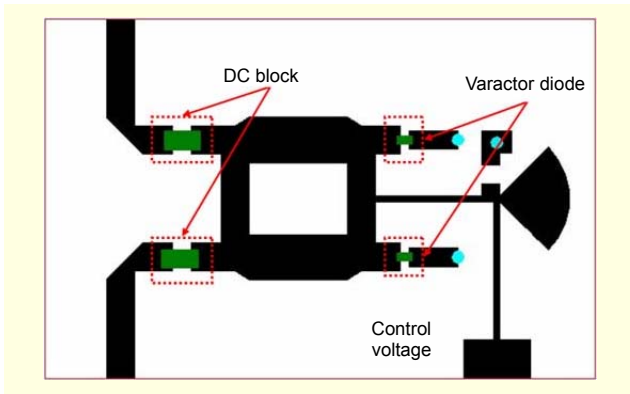


Fig. 7. Layout of a 10 GHz reflection-type phase shifter.

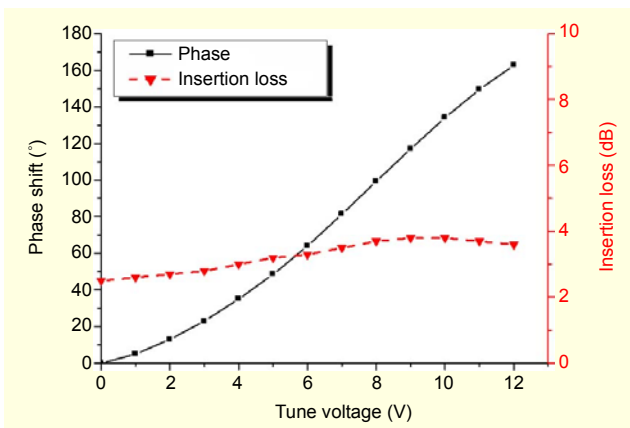


Fig. 8. Measurement result of the 10 GHz phase shifter.

varactor diodes (GMV-9821) and a 10 GHz 90° branch-line coupler. The GaAs hyper-abrupt varactor diode (GMV9821) has the capacitance of $C_{12} = 0.8$ pF for a bias voltage $V_R = 10$ V and a capacitance ratio of $C_{12}:C_1 = 1:6.15$. Figure 8 shows the layout of the fabricated 10 GHz phase shifter. The measured insertion loss and phase shifting performance at 10 GHz are shown in Fig. 8. The total phase shift is about 160°, and the insertion loss is 3.5 ± 0.5 dB for a given bias voltage (1 to 12 V). Input and output return loss is more than 10 dB. Since the signal is multiplied four times in the 40 Gb/s CDR module, total phase shift can be as much as 640° at 40 GHz.

5. Multiplier and Bandpass Filter

An active frequency multiplier is used. To suppress the unwanted spurious signal and jitter, a 40 GHz tapped coupled-line bandpass filter is fabricated [6] and connected at the output of the multiplier. Measured insertion loss and return loss of the filter at 40 GHz are 3.7 dB and 20 dB, respectively.

6. Decision Circuit

A decision circuit recovers the distorted binary data by retiming the noisy input data signal using the recovered clock

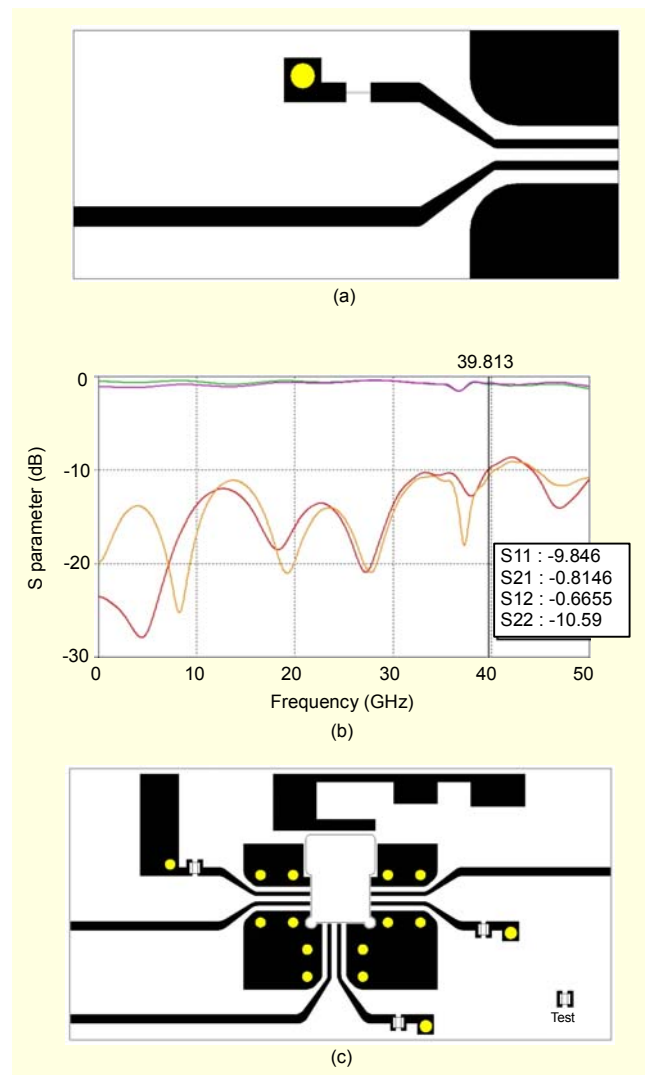


Fig. 9. (a) Input (or output) transition layout, (b) transition performance, and (c) layout of the decision circuit.

signal from the output of the CR circuit. The decision circuit uses a 40 Gb/s D-FF (Inphi 43700DF). The D port of the D-FF is connected with the input NRZ signal and CLK port of the D-FF is connected with the phase-shifted recovered clock signal.

This decision circuit is implemented with the alumina thin-film substrate ($\epsilon_r=9.98$). Figure 9(a) shows the layout of the input (or output) port of the decision circuit. The input microstrip line is transformed to a differential line (coupled microstrip line with the odd mode impedance of 100 Ω) to match the input impedance of the D-FF. Figure 9(b) shows the simulated performance of the transition. With this transition, for the frequency range of DC to 40 GHz, the return loss, $|S_{11}|$, is greater than 10 dB, and the insertion loss is less than 1 dB. Figure 9(c) shows the layout of the complete decision circuit.

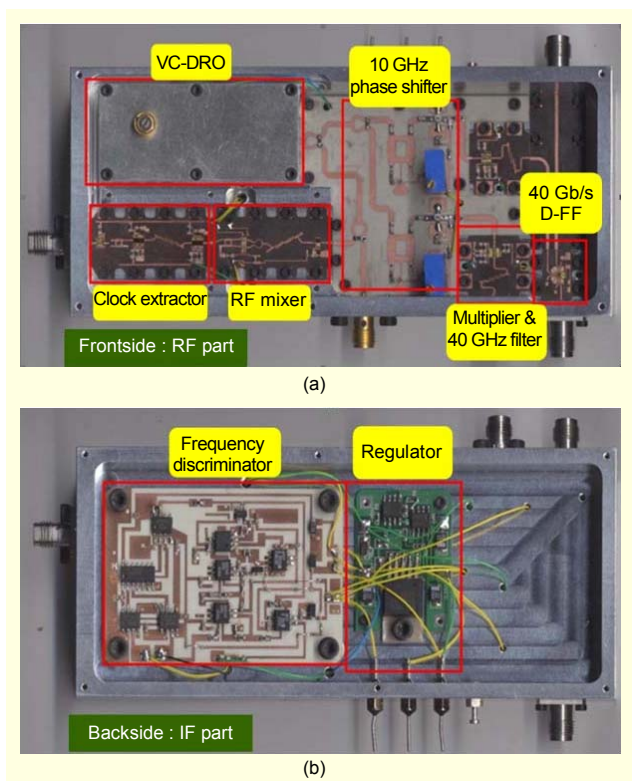


Fig. 10. Implemented 40 Gb/s PLL clock recovery module.

III. Implementation and Experimental Results

A 40 Gb/s CDR module, which consists of the clock extractor, the PLL block, and the D-FF decision circuit, was integrated as one compact module, as shown in Fig. 10. The RF boards for circuits working at 40 GHz and 10 GHz were fabricated with the Rogers RT/Duroid 5880 ($h = 5$ mil, $\epsilon_r = 2.2$) substrate and the Rogers 4003 ($h = 20$ mil, $\epsilon_r = 3.38$) substrate, respectively. The size of the CDR module is 59 mm \times 137 mm \times 34 mm, and the power consumption is 565 mA at 6 V, 110 mA at 9 V, and 220 mA at -3.3 V.

When the phase of the 39.813 GHz clock signal extracted from the clock extractor is synchronized with the phase of the 9.953 GHz VC-DRO, the loop bandwidth of the PLL acts as a very narrow bandpass filter. The synchronized 9.953 GHz VC-DRO clock signal is then amplified, phase-shifted, and multiplied by the quadrupler. The frequency lock range of the CR circuit is about 23 MHz, which is currently limited by the bandwidth of the OP-AMP comparator (LM360) shown in Fig. 4. Figure 11(a) shows the clock waveform recovered by the clock extractor and a 40 GHz-band DR filter. Figure 11(b) shows the clock waveform obtained by the clock extractor and the PLL circuit. The RMS jitter of the clock signals recovered with the PLL circuit was measured to be 210 fs, which is better than that of clock signals recovered with the DR filter (650 fs).

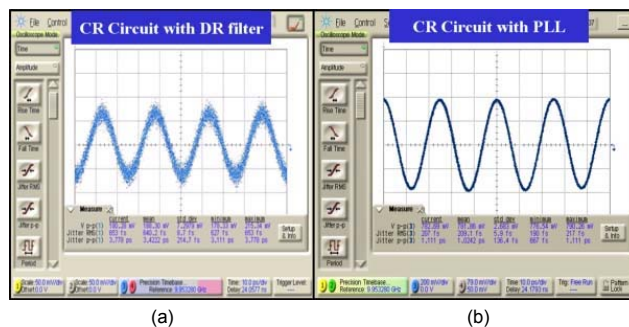


Fig. 11. Recovered clock waveforms using (a) the clock extractor and a DR filter and (b) clock extractor and the PLL circuit.

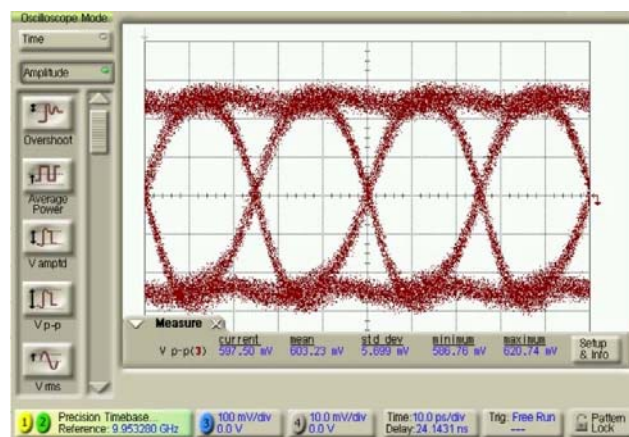


Fig. 12. Eye diagram of the recovered data.

The output power of the recovered clock signal was measured to be 0 dBm for the wide power variation of optical input signals from -5 to +5 dBm. Finally, the eye diagram of the retimed data obtained with the implemented CDR module is shown in Fig. 12, which was measured using an Agilent 86100A digital oscilloscope with a precision time-base module and a 70 GHz remote sampling module. Error free operation of the PLL CDR module was confirmed for 40 Gb/s pseudo-random binary sequence ($2^{31}-1$) data.

IV. Conclusion

A reliable 40 Gb/s CDR module for a fiber-optical receiver was successfully implemented. The CDR module utilizes a PLL, which acts as a very high-Q bandpass filter for the extracted clock. The PLL of the CDR module was implemented with an improved D-FF-based frequency acquisition circuit, which significantly enhances the lock speed and stability of the loop as compared with conventional acquisition circuits. Moreover, the proposed acquisition circuit helps to reduce power consumption and broaden the frequency acquisition range. The implemented PLL CDR module was

demonstrated to have a lower timing jitter (RMS) of 210 fs.

References

- [1] K. Murata and T. Otsuji, "A Novel Clock Recovery Circuit for Fully Monolithic Integration," *IEEE Trans. Microwave Theory & Tech.*, vol. 46, no. 12, Dec. 1999, pp. 2528-2533.
- [2] D. Briggmann, G. Hanke, U. Langmann, and A. Pottbacker, "Clock Recovery Circuits up to 20 Gbit/s for Optical Transmission Systems," *1994 IEEE MTT-S Int. Microwave Symp. Dig.*, June 1994, pp. 1093-1096.
- [3] S. Vehovc, M. Vidmar, and A. Paoletti, "80 Gbit/s Optical Clock Recovery with Automatic Lock Acquisition Using Electrical Phase-Locked Loop," *Electronics Letters*, vol. 39, no. 8, Apr. 2003, pp. 673-674.
- [4] S. Vehovc, "Clock Recovery at Gigabit-per-Second Data Rates," *Microwave Journal*, July 2000, pp. 22-34.
- [5] J.H. Song, T.W. Yoo, J.H. Ko, C.S. Park, and J.K. Kim, "Design and Characterization of a 10 Gb/s Clock and Data Recovery Circuit Implemented with Phase-Locked Loop," *ETRI Journal*, vol. 21, no. 3, Sept. 1999, pp. 1-5.
- [6] D.S. Woo, K.W. Kim, S.K. Lim, and J.S. Ko, "Implementation of a Low-Cost Phase-Locked Loop Clock Recovery Module for 40 Gb/s Optical Receivers," *Microwave and Optical Technology Letters*, vol. 48, no. 2, June 2006, pp. 312-315.
- [7] Y. DuFour, "A Phase-Locked Loop Lock Condition Detector," US Patent no. 6229864 B1, May 8, 2001.
- [8] H. Nosaka, K. Ishii, T. Enoki, and T. Shibata, "A 10-Gb/s Data-Pattern Independent Clock and Data Recovery Circuit With a Two-Mode Phase Comparator," *IEEE J. Solid State Circuits*, vol. 38, no. 2, 2003, pp. 192-197.
- [9] A. Brilliant, "Understanding Phase-Locked DRO Design Aspects," *Microwave Journal*, Sept. 1999, pp. 22-42.
- [10] R.R. Cordell, J.B. Fomey, C.N. Dunn, and W.G. Garrett, "A 50 MHz Phase- and Frequency-Locked Loop," *IEEE J. Solid-State Circuits*, vol. SC-14, no. 6, Dec. 1979, pp. 1003-1010.
- [11] J. Tusch, "On Frequency Sweeping in Phase-Locked Loops," *IEEE Trans. Comm.*, vol. 32, no. 8, Aug. 1984, pp. 969-972.



Hyun Park received the BS and MS degrees in electrical engineering from Kyungpook National University in 2005 and 2008, respectively. In 2008, he joined EM-Wise Communications Company, and currently serves as team manager at the RF R&D team 1. His current research interests and specialties include ultra-wideband components and systems, low phase-noise microwave sources, and microwave/millimeter-wave transceivers.



Kang Wook Kim received the BS and MS degrees in electrical engineering from Seoul National University in 1985 and 1987, respectively. In 1996, he received the PhD degree from the University of California, Los Angeles. From 1987 to 1990, he worked as a researcher at the Korea Electrotechnology Research Institute, Changwon, Rep. of Korea. From 1996 to 1998, he held a position as a post-doctoral researcher at the University of California, Los Angeles. From 1998 to 1999, he was employed as a microwave design engineer at P-Com, Inc, Campbell, California. From 1999 to 2001, he worked as an RF design engineer at Narda DBS Microwave, an L-3 Communications Company, California. Since September 2001, he has held a professorship at the School of Electrical and Computer Science at Kyungpook National University, Daegu, Rep. of Korea. In 2007, he founded a venture company, EM-Wise Communications Company, of which he is CEO. His current research interests and specialties include ultra-wideband components and systems, low phase-noise microwave sources, microwave/millimeter-wave transceivers, antennas for wireless personal communications, and plasma diagnostics using microwave/mm-wave components.



Sang-Kyu Lim received the BS degree in physics in 1995, and the MS and PhD degrees in electronics engineering from Sogang University, Seoul, Rep. of Korea, in 1997 and 2001, respectively. In 2001, he joined Electronics and Telecommunications Research Institute (ETRI), Daejeon, Rep. of Korea, where he has worked on passive and active microwave circuits for 40 Gb/s optical transmission technologies. His research interests include the design and fabrication of microwave and millimeter-wave circuits for high-speed optical transmission systems. He is currently a senior member of engineering staff at the Optical Communications Research Center in ETRI.



Jesoo Ko received the BS degree in electrical engineering from Ulsan University, Ulsan, Rep. of Korea, in 1981, and the MS degree in electronic engineering from Korea University, Seoul, Rep. of Korea, in 1983. In 1983, he joined Electronics and Telecommunications Research Institute (ETRI), Daejeon, Rep. of Korea, where he engaged in research and development of next-generation optical transmission technologies. His main research interests include high-speed optical transport systems, optical modules, and related devices. He is currently a principal member of engineering staff at the Optical Communications Research Center in ETRI.