Design and Implementation of Open-Loop Clock Recovery Circuit for 39.8 Gb/s and 42.8 Gb/s Dual-Mode Operation

Sang-Kyu Lim, Hyunwoo Cho, Jongyoon Shin, and Jesoo Ko

This paper proposes an open-loop clock recovery circuit (CRC) using two high-Q dielectric resonator (DR) filters for 39.8 Gb/s and 42.8 Gb/s dual-mode operation. The DR filters are fabricated to obtain high Q-values of approximately 950 at the 40 GHz band and to suppress spurious resonant modes up to 45 GHz. The CRC is implemented in a compact module by integrating the DR filters with other circuits in the CRC. The peak-to-peak and RMS jitter values of the clock signals recovered from 39.8 Gb/s and 42.8 Gb/s pseudo-random binary sequence (PRBS) data with a word length of 2^{31}–1 are less than 2.0 ps and 0.3 ps, respectively. The peak-to-peak amplitudes of the recovered clocks are quite stable and within the range of 2.5 V to 2.7 V, even when the input data signals vary from 150 mV to 500 mV. Error-free operation of the 40 Gb/s-class optical receiver with the dual-mode CRC is confirmed at both 39.8 Gb/s and 42.8 Gb/s data rates.

Keywords: Clock recovery circuit, clock and data recovery, CDR, open-loop clock recovery, 40 Gb/s optical transmission system.

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I. Introduction

These days, the capacity of backbone networks is increasing rapidly to support the proliferation of high-speed access networks and the growth of multimedia services. Recently, 40 Gb/s channels have begun to be required in addition to existing 2.5/10 Gb/s channels. To fulfil this need, various 40 Gb/s optical and electrical components have been developed [1]-[4].

The clock recovery circuit (CRC), a key component in a transmission system, extracts the clock signal from the incoming data stream. An optical receiver performs data regeneration and demultiplexing into the tributary signals using the recovered clock signal.

Clock recovery circuits can be classified into two types. One type is the closed-loop or adaptive CRC using a phase-locked loop (PLL) technique. It achieves inherently superior performance with low timing jitter and can be implemented in a fully monolithic circuit. Recently, several variations of 40 Gb/s-class monolithic CRCs or clock and data recovery (CDR) circuits based on the PLL technique have been demonstrated [5]-[9]. Another type is the open-loop or passive CRC using a passive filter. Examples include the surface-acoustic-wave (SAW) filter, the dielectric resonator (DR) filter, and the tank filter. They have simpler circuit configuration and can be implemented at lower cost than the closed-loop CRC.

SAW filters are limited to a maximum of around 2 Gb/s due to very small electrode spacing [10]-[12]. For higher transmission rates, a dielectric resonator has been used to build a passive filter since it shows a high dielectric constant, good

temperature stability, and low loss [13]-[17]. However, it has been pointed out that such passive filters are difficult to integrate with other electrical circuits in the CRC [18]. The open-loop CRC has been almost always built with combinations of individual module components and cables or connectors.

A DR filter is commonly composed of a disc-shaped dielectric resonator, a metal cavity, and feeding probes realized by microstrip or coaxial line. The resonant frequency of a DR filter is determined by the dielectric constant and size of the DR and the volume of the metal cavity. Usually, a tuning screw is attached to the cavity to adjust the resonant frequency. However, the tuning range is not wide enough to cover all 40 Gb/s-class signals including STM-256 (39.813 Gb/s), OTU-3 (43.018 Gb/s) or multiplexing of four ODU-2 (4×10.709 Gb/s = 42.837 Gb/s). The open-loop CRC using passive filters to support multi-data-rates in the 40 Gb/s class has not been reported to our knowledge.

In this paper, we propose a dual-mode CRC using two DR filters, which can be applied to both 39.8 Gb/s and 42.8 Gb/s operation. The DR filters are designed to achieve high Q-values and to suppress spurious resonant modes. In addition, the proposed CRC can be easily integrated with other circuits. It is implemented in a compact module using hybrid microwave integrated circuit (MIC) technology. We discuss the circuit architecture and design details in section II. We show the measurement results in section III, and conclusions are presented in section IV.

II. Circuit Design and Implementation

Figure 1 is a block diagram showing the function of a clock and data recovery circuit in an optical receiver. The data amplified by a buffer amplifier is applied to both the decision circuit and the CRC. The CRC extracts the clock signal from the non-return-to-zero (NRZ) data and supplies the recovered clock to the decision circuit and the demultiplexer through phase shifters. The decision circuit retimes and regenerates the data using the recovered clock.

Figure 2 shows a block diagram of a typical open-loop CRC

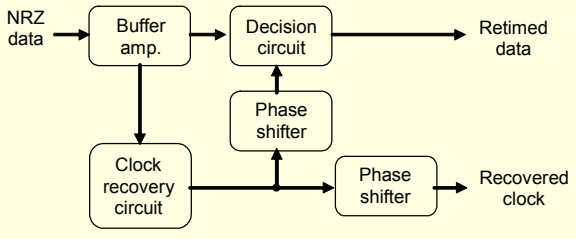


Fig. 1. Block diagram of CDR circuit in an optical receiver.

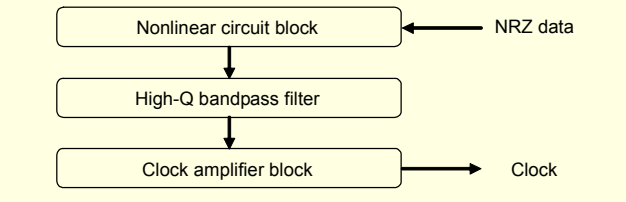


Fig. 2. Block diagram of typical open-loop CRC using a passive filter.

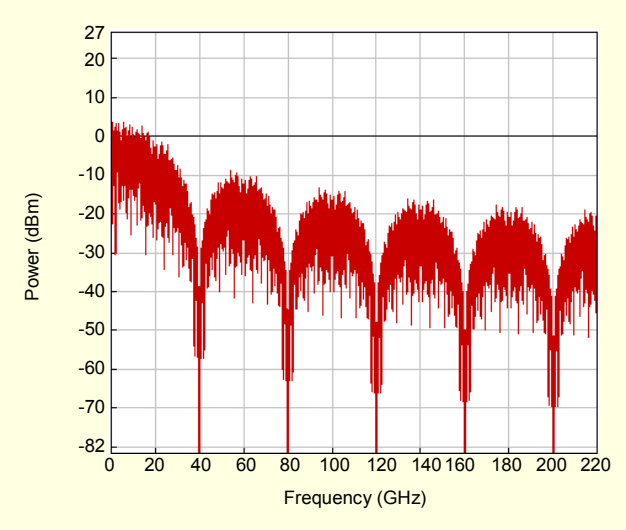


Fig. 3. Calculated spectra of 40 Gb/s NRZ signal.

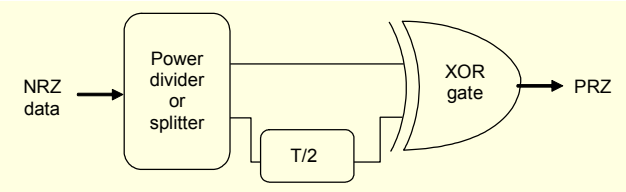


Fig. 4. Block diagram of conventional delay and XOR circuit.

using a passive filter. The nonlinear circuit produces the clock frequency component which is not contained in NRZ data, as shown in Fig. 3. It was reported that the nonlinear function could be implemented by various techniques, such as a full-wave rectifier, a squarer, or a delay and exclusive-OR (XOR) circuit [19]. A delay and XOR circuit has often been applied to the open-loop CRC because of its simple configuration. Figure 4 shows the block diagram of a conventional delay and XOR circuit for a fixed input data rate. It converts the NRZ signal into modified return-to-zero (RZ) or pseudo-return-to-zero (PRZ) signal containing the clock spectral line through the XOR logic operation of a pair of NRZ signals. Therefore, the delay and XOR circuit is also called an NRZ-PRZ converter.

In Fig. 4, the time difference between two NRZ data streams of the XOR input to obtain the maximum clock spectral line at

the XOR output is half of the time period *(T*/2) of the input NRZ data. For example, if the signals are transmitted through the coaxial lines from the power divider to the XOR input, as shown in Fig. 4, the length difference between two coaxial lines, L_{diff}, to satisfy the *T*/2 time difference condition can be expressed as

$$L_{diff} = \frac{c}{\sqrt{\varepsilon_r}}\left(\frac{T}{2}\right), \quad (1)$$

where c is the speed of light in free space, and ε_r is the relative dielectric constant of dielectric material in the coaxial line.

The bandpass filter extracts only the clock component in the spectrum generated by a nonlinear circuit. The bandwidth of the bandpass filter must be narrow enough to obtain the high quality clock. The clock amplifier increases the clock amplitude to be sufficient for data recovery and demultiplexing.

Figure 5 shows the block diagram of the proposed dual-mode CRC using two DR filters. It is composed of an NRZ-PRZ converter, a power divider, two DR filters, and two clock amplifiers. The NRZ-PRZ converter is a kind of nonlinear circuit. It consists of a resistive-T divider using three thick-film resistors (IMS 0302PW), a pair of microstrip delay lines, an XOR device, and 40 GHz-band amplifiers, as shown in Fig. 6. The resistive-T divider was selected to divide the NRZ signal because it shows good impedance matching characteristics over a wide frequency range despite high insertion loss. Each component was assembled on a Rogers RT/duroid 5880 (thickness=5 mil, dielectric constant=2.2) substrate.

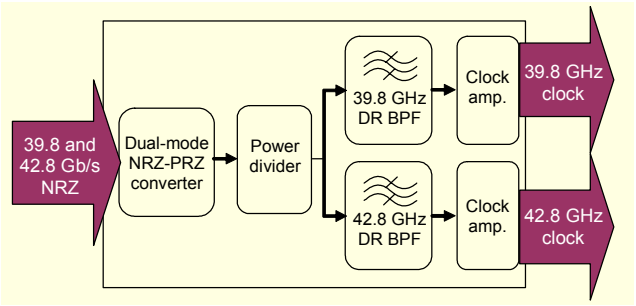


Fig. 5. Block diagram of dual-mode CRC for 39.8 Gb/s and 42.8 Gb/s operation.

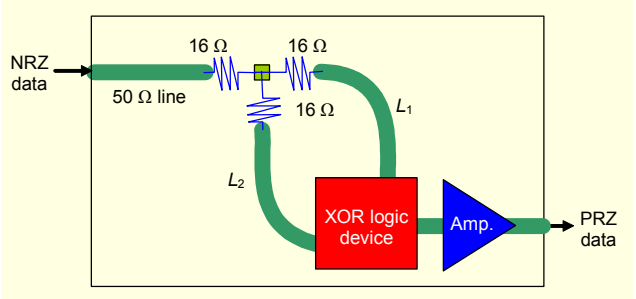


Fig. 6. Schematic of NRZ-PRZ converter for dual-mode operation.

It can be empirically shown that when the time difference between two XOR input signals transmitted through the microstrip delay lines L_1 and L_2 (see Fig. 6) is close to half the time period of 39.8 Gb/s, or 12.56 ps, the 39.8 GHz clock spectral power obtained from 39.8 Gb/s input is greater than the 42.8 GHz clock power due to 42.8 Gb/s input. Likewise, if the time difference is close to half the time period of 42.8 Gb/s, or 11.67 ps, the 42.8 GHz clock power is greater than the 39.8 GHz clock power. Therefore, the time difference between two XOR input signals for dual-mode operation was designed to be 12.1 ps, which corresponds to half the time period at 41.3 Gb/s (the mean of 39.8 Gb/s and 42.8 Gb/s). This allows the NRZ-PRZ converter to generate the same clock spectral power when operating at 39.8 Gb/s or 42.8 Gb/s. The length difference between delay lines, $|L_2 - L_1|$, can be expressed as

$$|L_2 - L_1| = \frac{c}{2\sqrt{\varepsilon_{eff}}}\left(\frac{T_1 + T_2}{2}\right), \quad (2)$$

where T_1 and T_2 are time periods of 39.8 Gb/s and 42.8 Gb/s, c is the speed of light in free space, and ε_{eff} is the effective dielectric constant of the microstrip line.

The power divider in Fig. 5 divides the 39.8 GHz or 42.8 GHz clock power into two paths. This allows the 39.8 GHz and 42.8 GHz clock signals to be extracted at each path. We used a Wilkinson divider, as shown in Fig. 7, because it shows low insertion loss and the reflected power can be dissipated. In Fig. 7, the length of 70.71 Ω line was optimized to be λ/4 near 41.3 GHz, where λ is the wavelength, in order that the return loss ($-S_{11}$) was more than 15 dB at both 39.8 and 42.8 GHz.

The DR filters have been designed so that they can be connected with other circuits through ribbon bonds as shown in Fig. 8. The metallic cover to form the resonance cavity has a simple C-shaped structure and can be easily attached or detached.

The resonant frequency of the DR filter is mainly determined by the dielectric constant, the thickness, and the diameter of a dielectric resonator, as well as the volume of the metal cavity.

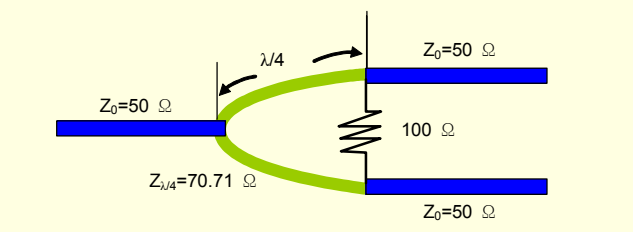


Fig. 7. Schematic of Wilkinson divider.

The $TE_{01\delta}$ resonant frequency range of a cylindrical dielectric resonator can be calculated from the equations and the root-finding algorithms described in [20]. We selected the cylindrical dielectric resonators with a dielectric constant of 30 and a diameter of 1.6 mm. From the electromagnetic (EM) simulation (Ansoft HFSS) results, the inner height and width of the metallic cover were designed to be 1.7 mm and 2.4 mm, respectively, for the suppression of spurious resonant modes. For a high Q-value, the gap between the DR and the feeding microstrip line was designed to be 0.2 mm to 0.4 mm. The fine tuning of the resonant frequency was accomplished by slightly reducing the thickness of the DR while measuring the resonant frequency. A tuning screw was not used because it could cause spurious modes and degradation of the recovered clock quality.

The clock amplifiers raise the clock amplitude to a constant level although the amplitudes of the input data may vary within a wide range. The 40 GHz-band monolithic MIC amplifiers (UMS CHA2194) were used, and a shunt-type open-stub was inserted for the improvement of input impedance matching.

All circuit blocks were designed to have good impedance matching performance because impedance mismatch causes output clock jitter. They were assembled into a high-speed package with 1.85 mm connectors after the measurements for each block. Then, they were connected to each other by 2 mil ribbon bonds, as shown in Fig. 9. The top of each circuit block was at the same level to minimize ribbon bond lengths.

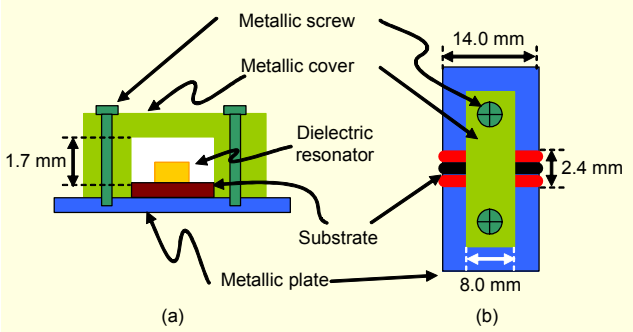


Fig. 8. Schematic of DR bandpass filter: (a) side view and (b) top view.

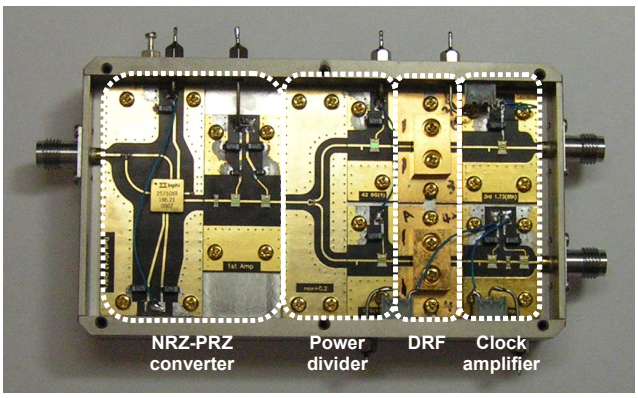


Fig. 9. Photograph of implemented 39.8 Gb/s and 42.8 Gb/s dual-mode CRC.

III. Measurement Results

Figures 10(a) and (b) show the spectra measured at the output of the XOR in the NRZ-PRZ converter when the input data rates were 39.8 Gb/s and 42.8 Gb/s, respectively. These measurements were performed using a microstrip test fixture (ICM WK-3001-G) to verify the dual-mode operation of the NRZ-PRZ converter before packaging. Each clock spectral power generated from 39.8 Gb/s and 42.8 Gb/s NRZ inputs was measured to be -18 dBm and -20 dBm, respectively. The power extinction ratio between a clock component and noise was more than 20 dB. Figures 11(a) and (b) show the waveforms converted from the 39.8 Gb/s and 42.8 Gb/s NRZ data, respectively.

The measured narrowband frequency responses around the

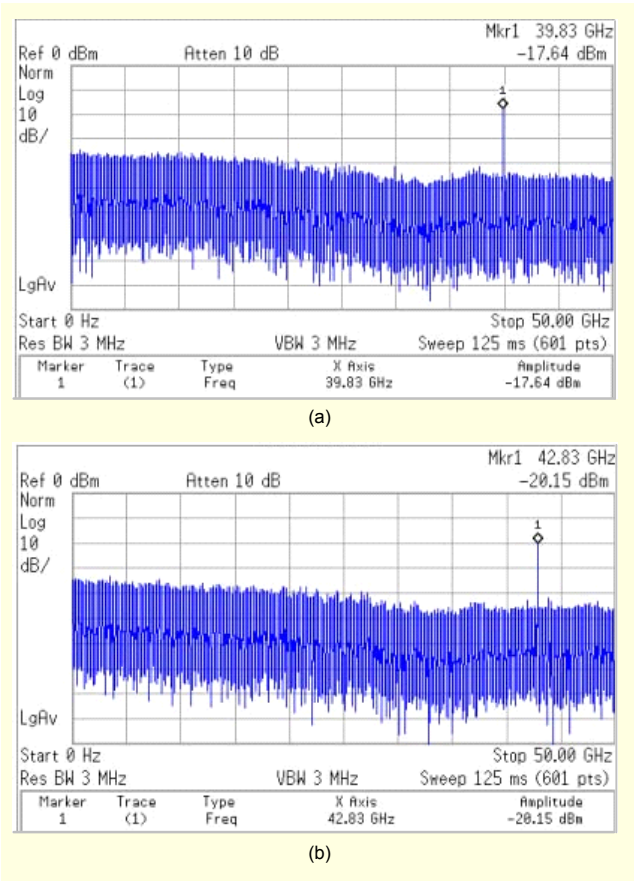


Fig. 10. Spectra measured at the output of XOR in the NRZ-PRZ converter: (a) 39.8 Gb/s operation and (b) 42.8 Gb/s operation.

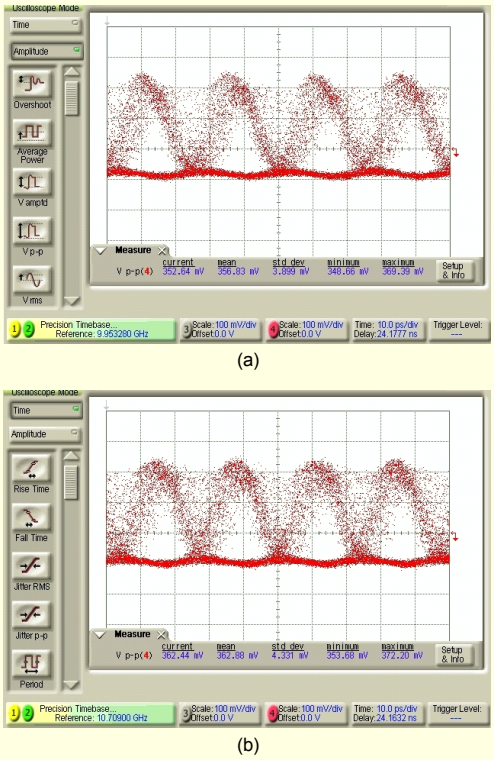


Fig. 11. Waveforms measured at the output of XOR in the NRZ-PRZ converter: (a) 39.8 Gb/s operation and (b) 42.8 Gb/s operation.

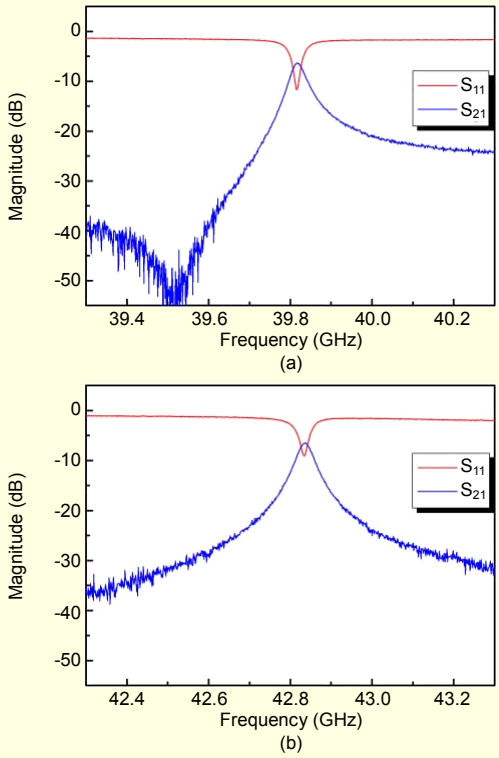


Fig. 12. Measured narrowband frequency responses of the DR filters.

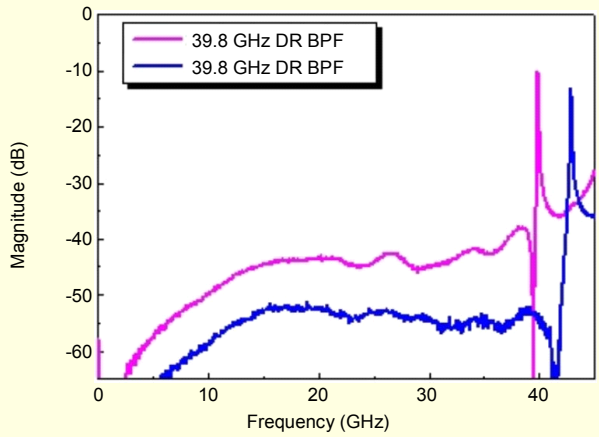


Fig. 13. Measured broadband frequency responses of the DR filters.

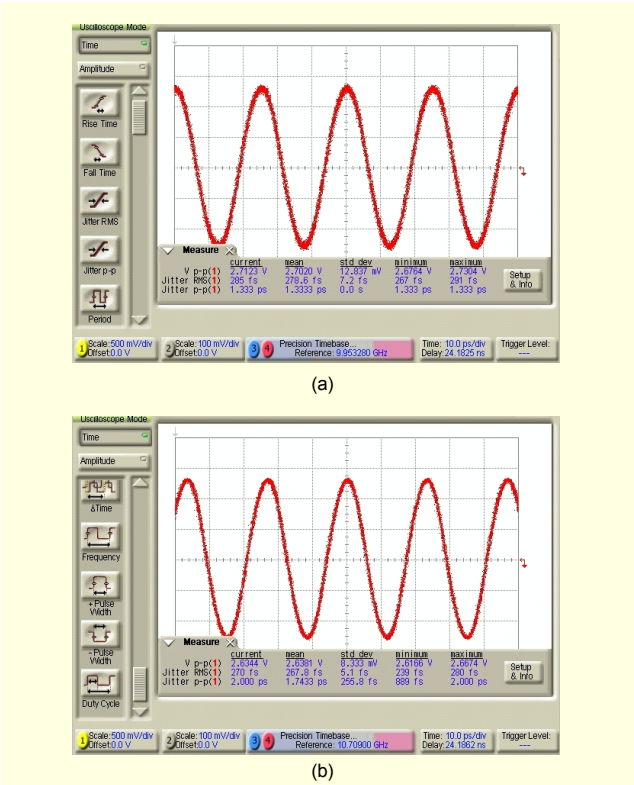
Table 1. Measured characteristics of the DR filters.

Center frequency (GHz)	39.813 / 42.837
Q-value	~ 950
Insertion loss (dB)	~ 6.5
Return loss (dB)	> 8.5

passband of the DR filters for 39.8 GHz and 42.8 GHz clock extraction are shown in Figs. 12(a) and (b), respectively. The broadband characteristics are shown in Fig. 13. The Q-value and insertion loss at each clock frequency are approximately 950 and 6.5 dB, respectively. The return losses are more than 8.5 dB. No spurious mode except the clock frequency band is found up to 45 GHz. The performance of the DR filters is summarized in Table 1.

The 39.8 Gb/s and 42.8 Gb/s (PRBS 2^{31}–1) electrical data converted from optical data through a 40 Gb/s-class photo-receiver was applied to the input of the CRC module in order to evaluate the performance.

Figures 14(a) and (b) show the clock waveforms recovered from 39.8 Gb/s and 42.8 Gb/s input data, respectively. The peak-to-peak and RMS jitter values of the recovered clock signals were less than 2.0 ps and 0.3 ps, respectively. The peak-to-peak amplitudes of the clocks were quite stable and within the range from 2.5 V to 2.7 V, even when the input data varied in the range from 150 mV to 500 mV. Error-free operation of the 40 Gb/s-class optical receiver with the dual-mode CRC was confirmed at both 39.8 Gb/s and 42.8 Gb/s data rates. The power dissipation of the CRC was 1.4 W at supply voltages of +3.5 V and -3.3 V. Table 2 summarizes the performance of the dual-mode CRC module, and the comparison of the recovered clock jitter values in the 40 Gb/s-class CRC or CDR including this work is shown in Table 3.



(a)

(b)

Fig. 14. Clock waveforms recovered from (a) 39.8 Gb/s PRBS (2^{31}–1) data and (b) 42.8 Gb/s PRBS (2^{31}–1) data.

Table 2. Performance summary of dual-mode CRC.

Input data rate	39.8 Gb/s and 42.8 Gb/s
Recovered clock jitter	2.0 ps (peak-to-peak), 0.3 ps (rms) for 2^{31}–1 PRBS
Recovered clock amplitude	2.5 V to 2.7 V (peak-to-peak)
Power dissipation	1.4 W @ +3.5 V and -3.3 V
Module size	100 mm × 60 mm × 21 mm
Technology	Open-loop CRC using DR bandpass filters and hybrid MIC technology

Table 3. Comparison of recovered clock jitters in 40 Gb/s-class CRC or CDR.

	[6]	[7]	[9]	This work
Input data rate	43 Gb/s	39 to 45 Gb/s	43 Gb/s	39.8 Gb/s, 42.8 Gb/s
Peak-to-peak clock jitter (for 2^{31}–1 PRBS)	4.5 ps @ 21.5 GHz	3.6 ps	N/A	2.0 ps
RMS clock jitter (for 2^{31}–1 PRBS)	N/A	0.48 ps	1.2 ps	0.3 ps
Type	Closed loop	Closed loop	Closed loop	Open loop

IV. Conclusion

In this paper, we presented a compact clock recovery circuit for dual-mode operation in the 40 Gb/s class. This open-loop CRC was implemented using an NRZ-PRZ converter, a power divider, two high-Q DR filters, and two clock amplifiers. The DR filters were fabricated to obtain high Q-values (approximately 950) and to suppress spurious resonant modes up to 45 GHz. The CRC was implemented in a compact module by integrating the DR filters with other electrical circuits in the CRC.

The peak-to-peak and RMS jitter values of the clock signals obtained from 39.8 Gb/s and 42.8 Gb/s input data were less than 2.0 ps and 0.3 ps, respectively. These values are smaller than those of the clock achieved by a fully monolithic CRC using a PLL architecture.

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