Design of a Frequency Locked Loop Circuit

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Abstract—In this paper, I propose the full CMOS FLL(frequency locked loop) circuit. The proposed FLL circuit has a simple structure which contains a FVC(frequency-to-voltage converter), an operational amplifier and a VCO(voltage controlled oscillator). The operation of FLL circuit is based on frequency comparison by the two FVC circuit blocks. The locking time of FLL is short compared to PLL(phase locked loop) circuit because the output signal of FLL is synchronized only in frequency. The circuit is designed by 0.35μm process and simulation carried out with HSPICE. Simulation results are shown to illustrate the performance of the proposed FLL circuit.

Index Terms—frequency locked loop, frequency-to-voltage converter, voltage controlled oscillator

I. INTRODUCTION

A PLL(Phase Locked Loop) circuit is an important electronic block widely used in many integrated circuits. It is used in systems involving automatic control of frequency or phase, such as communication systems, frequency synthesis circuit and telemetry systems[1]. A PLL circuit is built in a phase detector, a charge pump, a low pass filter and VCO(Voltage Controlled Oscillator). However a PLL can not be fully integrated and the low pass filter is implemented externally with discrete components.

In this paper, a FLL(frequency Locked Loop) circuit similar to PLL is designed. It generates an output signal which tracks an input reference frequency. The designed FLL circuit is based on frequency comparison by the FVC(Frequency to Voltage Converter) which does not required the charge pump and the low pass filter. Therefore the designed FLL can be integrated on the one chip. The architecture of FVC circuit is built on the charge redistribution principle based on switching capacitor.

The remainder of this paper covers the description and the operation of the designed FLL. In Section II the design steps of the FLL and in Section III the simulation results will be shown. Finally, I conclude in Section IV .

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II. FLL Circuit implementation

Fig. 1 shows the block diagram of the FLL circuit. First, the frequency of the input signal is divided by 2^{n1} and converted to a voltage by the FVC1. The converted voltage, V_{O_FVC1}, is linearly dependent on the frequency of the input signal. The output of the VCO is divided by 2^{n2} in the same way. And the frequency information is converted to the voltage signal, V_{O_FVC2}, by the FVC2. The buffer is used for driving which is implemented an opamp. The voltage difference between V_{M1} and V_{M2} is then amplified by the opamp and the output voltage of the opamp, V_{IN_VCO}, is employed to control the output frequency of the VCO. The voltage V_{M2} will increase or decrease until the frequency of V_{O_FVC2} becomes equal to the frequency V_{REF}.

In Fig. 1 the frequency divider is implemented by using flip flops. The FVC1 and FVC2 act as a frequency comparator[2].

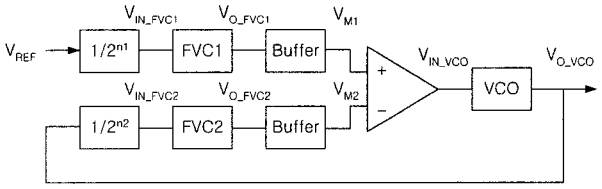


Fig. 1 Block diagram of the FLL circuit

Fig. 2 shows the structure of the FVC and operation steps and Fig. 3 shows control signals of switch S1, S2 and S3[3]. As shown in Fig. 2 when the switch S1 is on the capacitor C1 is charged to the supply voltage V_{DD}. When the switch S1 is off and S2 is on the capacitor C1 is discharged by the current source I_S. The charge stored in capacitor C1 is distributed between two capacitors C1 and C2 by the following equation:

$$C1 \cdot V_{T\_FVC} = C2 \cdot V_{O\_FVC} \quad (1)$$

Switch S1 and S2 are turned on and off alternatively as shown in Fig. 2 and Fig. 3. Switch S3 is on during very short time and then the charge redistribution is accomplished.

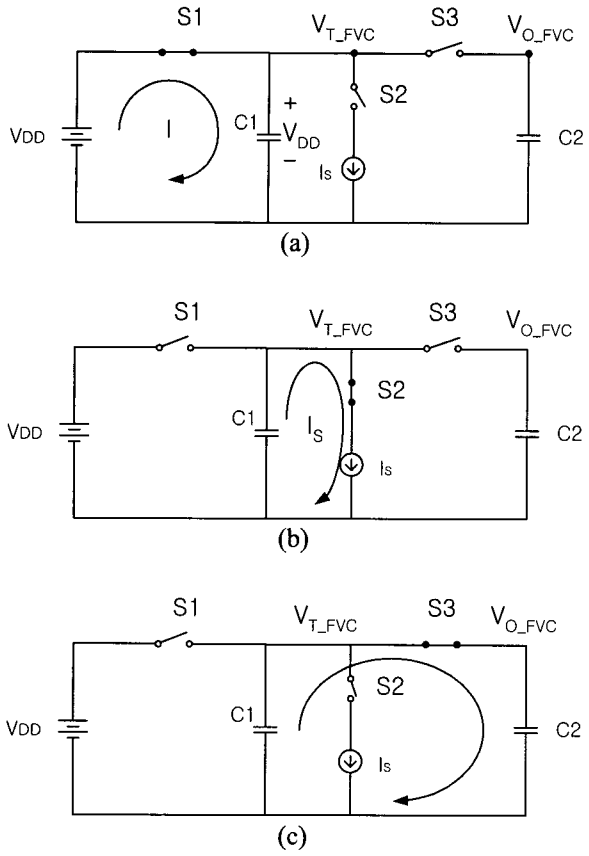


Fig. 2 Operation of the FVC circuit
(a) Charging of capacitor C1
(b) Discharge of capacitor C1
(C) Charge redistribution of C1 and C2

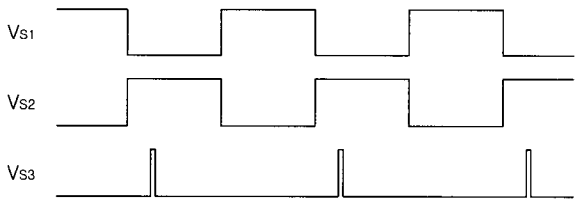


Fig. 3 Control signals of switch S1, S2 and S3

If the input frequency decreases the discharge time increases. As a result, the voltages of capacitor C1 and capacitor C2 decrease. Therefore the output voltage FVC is dependent on the frequency of input signal. Fig. 4 shows the circuit block to generate the control signals of switch S1, S2 and S3[4]. V_{S1}, V_{S2} and V_{S3} are the control of switch S1, S2 and S3, respectively. The time between the positive edge of V_{S2} and V_{S3} signals is controlled the bias voltage.

Fig. 5 shows the VCO circuit. The current, I_{IN}, flows through R5 which is given by $V(f_o)/R5$. The capacitor C1 is charged or discharged the current source kI_{IN}. The capacitor C1 is charged until the voltage is V_{REF1} when transistor MP67 is on. Also the capacitor C1 is discharged until the voltage is V_{REF2} when transistor MN61 is on. The peak voltages of the VCO are V_{REF1} and V_{REF2}.

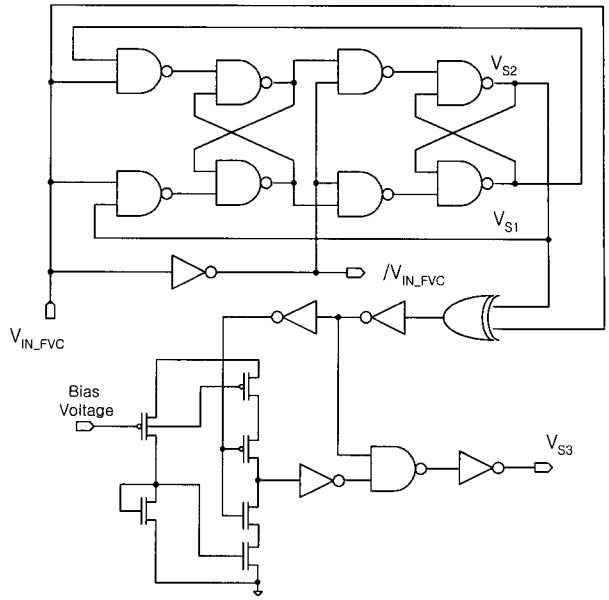


Fig. 4 Circuit to generate the switch control signals

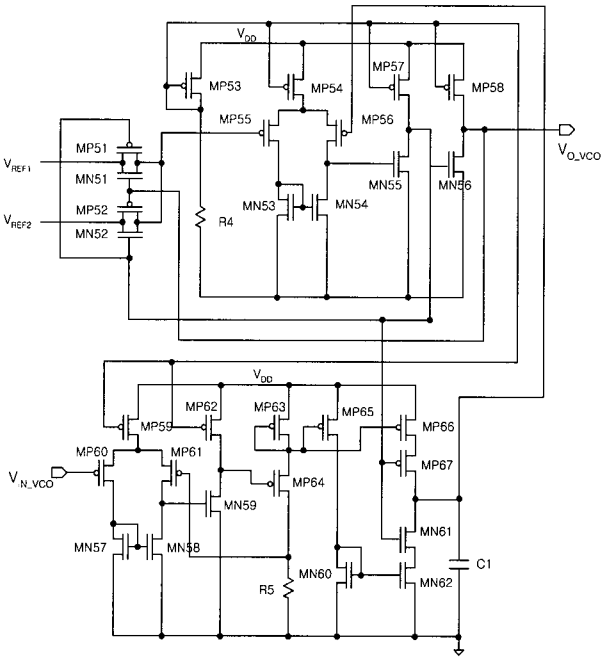


Fig. 5 VCO Circuit to generate output signal

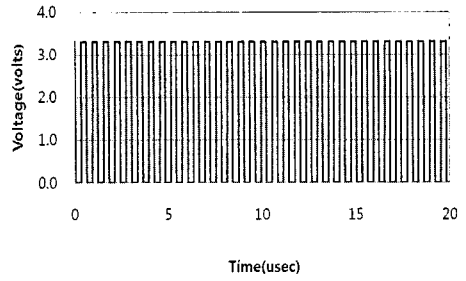
Eq. (2) is the output frequency of the VCO, and the output frequency can be controlled by the capacitor C1, R5 and the peak voltages V_{REF1} and V_{REF2}.

$$f_O = \frac{V_{IN\_VCO} / R5}{C1 \times (V_{REF1} - V_{REF2})} \tag{2}$$

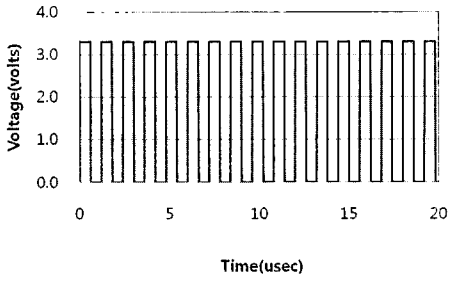
III. Simulation results

Fig. 6(a) shows V_{REF} signal and Fig. 6(b) shows V_{IN_FVC1} signal. Fig. 6(c) shows V_{T_FVC} signal in Fig. 2 and Fig. 6(d) shows V_{S3} signal in Fig. 3. V_{O_FVC} signal is

dependent on the input frequency and the voltage reaches its final value after about 15 cycle of V_{IN_FVC1} signal as shown in Fig. 6(e).



(a)



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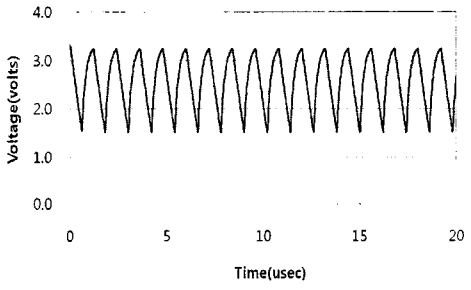
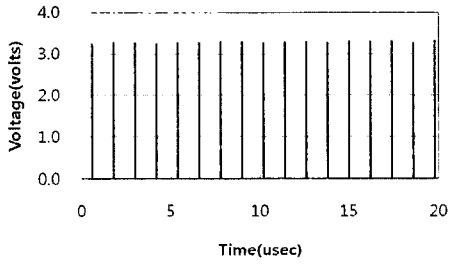
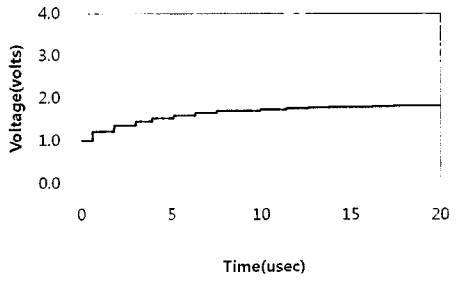


(c)



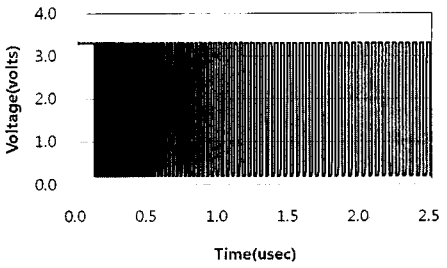
(d)



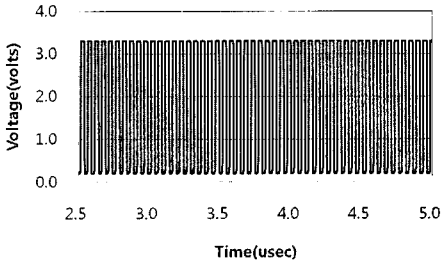
(e)

Fig. 6 The control signals of FVC
(a) V_{REF} (b) V_{IN_FVC1} (c) V_{T_FVC} (d) V_{S3} (e) V_{O_FVC}

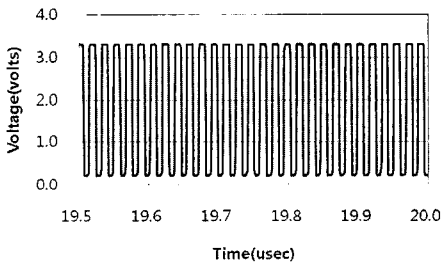
The output frequency of V_{O_VCO} signal tracks an input frequency with the time as shown in Fig. 7. The frequencies of V_{O_VCO} and V_{REF} signals are the same after about 19μsec.



(a)



(b)



(c)

Fig. 7 V_{O_VCO} with the time (a) $0 \leq t \leq 2.5\mu sec$ (b)$2.5\mu sec \leq t \leq 5.0\mu sec$ (c) $19.5\mu sec \leq t$

The performance of the designed FLL circuit is shown in Fig. 8. Fig. 8 shows the ratio output frequency and input frequency when the input frequency is varied from 40MHz to 60MHz. From the simulation results when the input frequency is varied in range from 41.7MHz to 58MHz the error can be neglected.

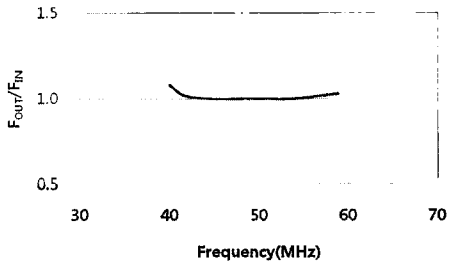


Fig. 8 F_{OUT}/F_{IN} with input frequency

IV. CONCLUSIONS

The FLL circuit is proposed to generate an output signal that tracks an input reference signal. And the FLL is designed to allow the circuit to be fully integrated. The FLL was simulated by using 0.35μm CMOS technology and the simulation results show enough performance in the viewpoint of the locking time.

ACKNOWLEDGMENT

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