Theoretical Study of Electron Mobility in Double-Gate Field Effect Transistors with Multilayer (strained-)Si/SiGe Channel

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***Abstract*—Electron mobility has been investigated theoretically in undoped double-gate (DG) MOSFETs of different channel architectures: a relaxed-Si DG SOI, a strained-Si (sSi) DG SSOI (strained-Si-on-insulator, containing no SiGe layer), and a strained-Si DG SGOI (strained-Si-on-SiGe-on-insulator, containing a SiGe layer) at 300K. Electron mobility in the DG SSOI device exhibits high enhancement relative to the DG SOI. In the DG SGOI devices the mobility is strongly suppressed by the confinement of electrons in much narrower strained-Si layers, as well as by the alloy scattering within the SiGe layer. As a consequence, in the DG SGOI devices with thinnest strained-Si layers the electron mobility may drop below the level of the relaxed DG SOI and the mobility enhancement expected from the strained-Si devices may be lost.**

***Index Terms*—Electron mobility modeling, double-gate SOI, strained silicon on insulator, strained silicon on silicon-germanium-on-insulator**

I. INTRODUCTION

The progress in the silicon MOS technology over the last decades involved the evolution of planar bulk MOSFETs into three-dimensional ultrathin body (UTB) structures, employing new materials and strain [1-3]. Particular benefits, mainly due to so-called volume inversion in the channel, have been expected from the double-gate (DG) devices [4-6]. Due to the second gate, which gives an extra control of the charge, DG devices are rich in phenomena relating to the semiconductor thickness and affecting the charge distribution and carriers mobility [7,8]. Theoretical investigations predict better performance and electron mobility in ultrathin symmetrical DG SOI MOSFETs than in single-gate (SG) devices [9,10]. However, the competition between UTB SG and DG devices depends on device thickness, transverse field and body crystal orientation [11-14].

It has been observed empirically and explained theoretically that carriers confined in UTB devices suffer from mobility degradation [15-19]. The most promising way to enhance the mobility is straining the channel area. Influencing most of material parameters, the strain explicitly modifies the energy band structure and affects the transport properties [20-23]. Although not all aspects of the effect of the strain on mobility have been so far satisfactorily explained [24], the strained Si/SiGe technology is already well established. The original way for straining Si, Ge, or SiGe layers was utilizing the crystal lattice mismatch between Si and Ge. Today, various techniques are available making it possible to obtain global stress within the whole layers as well as local stress, affecting selected regions of devices [25-28]. Biaxial tensile strain applied to (100) Si surface is particularly advantageous for the electron mobility due to higher population of the non-primed subbands (of smaller in-plane electron conduction mass) and suppression of the intersubband scat-tering. Tensely strained Si layers are epitaxially grown on relaxed $Si_{(1-x)}Ge_x$ virtual substrates, the magnitude of the strain depending on the Ge content in the SiGe alloy. In this way, bulk strained-Si MOSFETs as well as SOI-like strained-Si-on-SiGe-on-insulator

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devices (SGOI) can be produced [29,30]. Even more promising are techniques giving strained silicon bonded directly to the buried oxide, without the underlying SiGe layer, most frequently called strained-SOI (SSOI) or strained-silicon-directly-on-insulator (SSDOI) [31-33]. Thus drawbacks related to the presence of a SiGe layer are avoided. Therefore, there exist a justified motivation for combining the advantages of the strain with the benefits offered by the double-gate architecture within double-gate MOSFETs with strained channels [34-37].

In this paper we analyze the electron mobility in symmetrical DG NMOSFETs with strained-Si channel and compare it with the mobility obtained in relaxed-Si DG SOI (denoted here simply as SOI). We consider two types of double-gate devices with strained-Si channel: the double-gate strained-Si-on-insulator type (denoted here as SSOI), having the structure of Metal/Oxide/sSi/ Oxide/Metal, and the double-gate strained-Si-on-SiGe-on-insulator (denoted as SGOI), having the structure of Metal/Oxide/sSi/SiGe/sSi/Oxide/Metal. The same total semiconductor thickness of 12 nm is maintained for all the modeled devices. Such a thickness is perhaps not "ultrathin" but we hope it is still thin enough to enjoy the main advantages of the DG SOI MOSFETs [9], while being "thick" enough to contain the complex structure of the DG SGOI devices. Obviously, the DG SGOI structure is strongly handicapped in this comparison, because electrons are confined within two much narrower, actually ultrathin, strained-Si channels located on both sides of the SiGe layer, which itself introduces alloy scattering for a portion of electrons. So, the question arises whether such a structure is still competitive against the relaxed-Si DG SOI. To answer we employ our 1-D self-consistent Poisson-Schrödinger solver and analyze the low field electron mobility within the relaxation time approximation, taking into account the main scattering mechanisms believed to limit the electron mobility in the modeled devices at room temperatures, i.e., the phonon scattering and the interface roughness scattering along with the scattering due to thickness nonuniformity. Because we assumed non-doped devices, the Coulomb scattering was not included. In the case of DG SGOI devices, the alloy scattering has been considered.

The paper is organized as follows. In Section II details of the modeled devices are presented along with the description of the employed scattering models. In Section III we discuss obtained results. Finally, in Section IV the paper is summarized with the most important conclusions.

II. Simulated Structures and Mobility Model

As mentioned above, electron mobility at 300K is modeled and compared for three types of symmetrically operated double-gate devices, the first type being a conventional relaxed-Si DG SOI MOSFET (Fig. 1a), while the second type and the third type being devices having biaxially, tensely strained-Si channels, i.e., a DG SSOI MOSFET, containing no SiGe layer, (Fig. 1b), and a DG SGOI MOSFET (Fig. 1c), in which a relaxed SiGe layer is located between two strained-Si layers. All the devices have the same total semiconductor thickness of 12 nm. Therefore, the silicon thickness T_{Si} of the SOI device is equal to the strained-Si thickness T_{sSi} of the SSOI device, whereas the structure of the SGOI device gives an extra degree of freedom related to the thicknesses

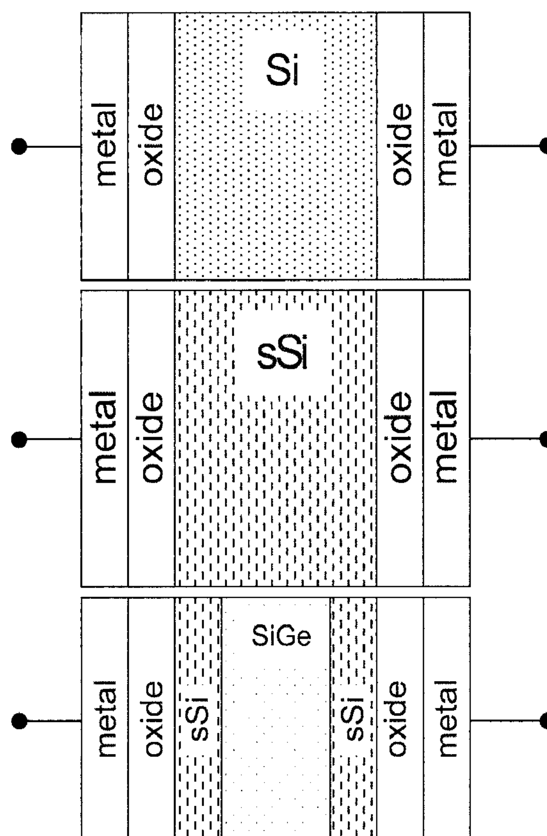

Fig. 1. Modeled double-gate MOSFETs: a) relaxed-Si DG SOI, b) DG SSOI (strained-Si-on-insulator), and c) DG SGOI (strained-Si-on-SiGe-on-insulator). The same total thickness of the semiconductor is preserved – 12 nm. The oxide thickness is 2 nm.

of the component layers. Thus, we investigated three configurations sSi/SiGe/sSi of the SGOI structure, maintaining the total thickness of 12 nm, namely a) 3 nm/6 nm/3 nm, b) 2.5 nm/7 nm/2.5 nm, and c) 2 nm/8 nm/2 nm. Another parameter, inherent to the strained-Si devices, is the strain level related to the germanium content x in the relaxed $Si_{(1-x)}Ge_x$ layer, which is present in the SGOI devices or which has been utilized (and then removed) in the manufacture process of SSOI devices. So, we investigated strained-Si devices for the germanium concentrations, x_{Ge} in the range 0.2 - 0.4. The silicon layers in the modeled devices are assumed to lie in the (100) crystallographic plane. No doping of the semiconductor is assumed. The gate oxide thickness T_{ox} is assumed to be 2 nm, and the structures are biased symmetrically by mid-gap metal gates.

The distributions of the potential energy and electron concentration, along with electron energy levels and corresponding envelope wave functions, were calculated within the effective mass approximation by self-consistent solution to 1-D Poisson and Schrödinger equations. Our solver was validated by comparison with simulation models developed by different research groups [38]. The parameters related to the energy band structure under strain were taken from [39].

Fig. 2 shows exemplary electrostatics results for the three types of simulated devices. Relative to the relaxed SOI device, the distribution of electron concentration, $n(z)$, in the SSOI device exhibits higher maximums moved slightly towards the SiO_2/Si interfaces, due to the strain, which increases the occupation of the *unprimed* subbands. A more pronounced change may be observed for the SGOI device. In this case the SiGe layer, because of the energy band discontinuity between Si and SiGe, practically divides the electron concentration into two "side channels" created by the sSi layers, which are much narrower than the Si or sSi layers in the SOI or SSOI devices. Hence, electrons in the SGOI device are supposed to suffer from more intensive phonon scattering. Moreover, the multilayer structure of the channel is more sensitive to the scattering due to thickness deviations. At last, a portion of electrons, still residing in the SiGe layer, is affected by the alloy scattering, which belongs to the dominant scattering mechanisms in SiGe alloys [40]. As shown in Fig. 3, the fraction of electrons occupying the SiGe layer may reach more than 40% for the configuration with narrowest sSi layers at low electron densities, N_{inv}, and for low Ge content. The fraction decreases with the inversion density increase as electrons are attracted towards the strained-Si layers. Also, it decreases with an increase of Ge content due to higher conduction band discontinuity, which deepens the potential wells for electrons in the both sSi layers.

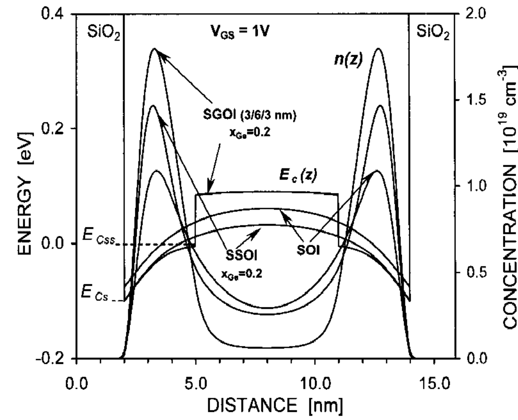

Fig. 2. Exemplary distributions of the conduction band edge $E_c(z)$ and the electron concentration $n(z)$ along the direction z, perpendicular to the surface.

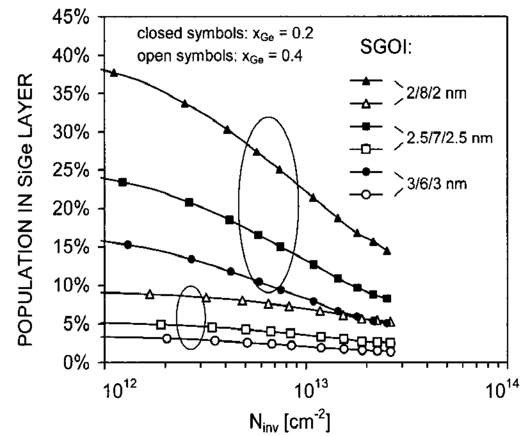

Fig. 3. A fraction of electrons residing in the SiGe layer vs. inversion charge density, N_{inv}, for the three considered configurations of the SGOI devices and two values of germanium content x_{Ge}.

Electron mobility was calculated within the momentum relaxation time approximation in the following manner. Subband mobilities, $\mu_{r,i}$ were obtained for each rth scattering mechanism:

$$\mu_{r,i} = \frac{e}{m_{ci}} \tau_{r,i} , \tag{1}$$

where m_{ci} is the conduction mass in i^{th} subband and

$\langle \tau_{r,i} \rangle$ is the subband relaxation time averaged over the energy distribution:

$$\tau_{r,i} = \frac{\sum_{\mathbf{k}} E(k)\tau_{r,i}(E(k))\left(-\frac{\partial f}{\partial E(k)}\right)}{\sum_{\mathbf{k}} E(k)\left(-\frac{\partial f}{\partial E(k)}\right)}. \quad (2)$$

Then, the mobility μ_r was calculated as an average over the relative subband occupations, N_i:

$$\mu_r = \frac{\sum_i \mu_{r,i} N_i}{N_{inv}}. \quad (3)$$

Finally, the effective electron mobility was derived by applying the Matthiessen's rule:

$$\frac{1}{\mu_{eff}} \approx \sum_r \frac{1}{\mu_r} \quad (4)$$

Scattering mechanisms believed to be the most significant suppressors of electron mobility in MOSFETs' channels have been included in this study, i.e., the phonon scattering, surface roughness scattering (due to roughness at the oxide/semiconductor interfaces), remote roughness scattering (due to oxide thickness deviations), scattering due semiconductor thickness deviations, and alloy scattering for structures including a SiGe layer. No doping as well as no interface states were assumed, so the corresponding Coulomb scattering components were excluded from the model. In practice, the Coulomb scattering is also related to unintended dopants present in the channel. The effect of unintentional doping is usually analyzed in terms of statistical fluctuation of devices' parameters. As evidenced in [41], also the drain current, hence the channel mobility, is strongly affected by unintended ions, even a single one, present in the channel, especially at the source end. These effects are particularly evident in narrow and short devices. Our study is focused, however, on electron low-field mobility in idealized structures, so no statistical fluctuations between a set of devices have been investigated and the unintentional doping has not been considered.

Another Coulomb interaction, possible even though analyzing an undoped channel is electron-electron scattering. Electron-electron scattering is traditionally attributed to very high electron concentrations, as in metals or heavily doped semiconductors. Therefore, it is usually not included in typical low-field mobility studies for inversion layer electrons, also to some extent because of implementation difficulties. However, there are studies suggesting significant coupling between channel electrons and gate electrons, via long-range interaction, leading to strong suppression of electron mobility for oxides below 3 nm [42]. However, this effect is not distinguishable in a straightforward manner in experimental data and may be overlapped with other scatterers. Also, short-range electron-electron interaction is predicted to have a significant influence, along with the electron-ions interactions, on electron transport [43]. In our study we stayed at the more conventional approach, neglecting the electron-electron scattering in the inversion layer.

Phonon scattering has been analyzed within the isotropic approach with the effective acoustic deformation potential D_{ac} = 12 eV. In order to reflect observed electron mobility enhancement in strained-Si channels, a set of phonon parameters was employed (a single type-f phonon: E_k = 59 meV, $D_k = 8.0\text{x}10^8$ eV/cm and a single type-g phonon: E_k = 63 meV, $D_k = 8.0\text{x}10^8$ eV/cm), which corresponds to stronger coupling for intervalley phonons [44] than the usually employed Jacoboni-Reggiani set [45].

The surface roughness scattering, including the screening effect, was treated according to the Ando's approach [46] revised for SOI devices [47,48]. Exponential spectrum of the surface roughness has been assumed [49] with the roughness rms of Δ_{rms} = 0.3 nm, and the correlation length of λ_{sr}=1.5 nm.

The values of the above scattering parameters were derived as the model was calibrated to the available experimental mobility data for unstrained DG SOI devices [11,12] (Fig. 5. Note, in this paper the mobility is plotted and analyzed versus the total inversion charge density, N_{inv}, and not versus $N_{inv}/2$ as in the referenced papers). Then, with the same parameters for the phonon scattering and the surface roughness scattering the model was employed for strained channel DG devices investigated in this paper.

Because the structure of the SGOI devices consists of several ultrathin layers, these devices are supposed to be particularly susceptible to the scattering due to thickness deviations. Therefore, we analyzed the deviations of the oxide thickness (remote scattering) as well as the relaxed/

strained silicon thickness. For the SGOI devices also the deviations of the SiGe layer thickness were included. The investigation was based on varying the thickness of a layer under consideration while keeping constant thicknesses of other layers.

A deviation of the oxide thickness from its average value, being assumed not to deviate the SiO_2/Si border, generates a perturbation *ΔV(z)* of the potential energy and introduces a scattering mechanism [50-52]. We treated the remote roughness similarly to the surface roughness, assuming arbitrarily the exponential spectrum of the oxide thickness deviations with the rms values of Δ_{Tox} ranging from 0.2 nm to 0.4 nm and the correlation length λ_{ox}=1.5 nm. The matrix elements of transitions between subbands *i* and *j* were calculated including only the "direct scattering" term as:

$$M_{ij}^{ox}(q) = \Delta_{Tox}(q) \int \xi_i(z) \frac{\partial V(z)}{\partial T_{ox}} \xi_j(z) dz \tag{5}$$

where ξ_i, ξ_j are corresponding electron envelope functions. For simplicity, both gate oxides were assumed to deviate in a correlated manner.

The scattering due to thickness deviations of the channel component layer(s) has been separated from the surface roughness scattering in that the surface roughness is interpreted here as lateral shifts of the whole structure without any thickness change. Thickness deviations explicitly induce fluctuations of quantized energy levels. These fluctuations are believed to contribute to the scattering and to limit the mobility in ultrathin devices [53-58]. The matrix element is usually defined only for intrasubband transitions as a change of a given energy level due to a change of the Si layer thickness T_{Si}:

$$M_{ii}^{Si}(q) = \Delta_{TSi}(q) \frac{\partial E_i}{\partial T_{Si}} \tag{6}$$

In extremely thin structures the potential energy distribution resembles an ideal rectangular well, in which energy levels may be expressed analytically [53]. Then, the derivative of the energy level with respect to the silicon thickness follows the dependency $(T_{Si})^{-3}$ and the scattering rate is proportional to $(T_{Si})^{-6}$. Such a behaviour of electron mobility was observed in ultrathin SOI devices, for which this type of scattering has been proved to be

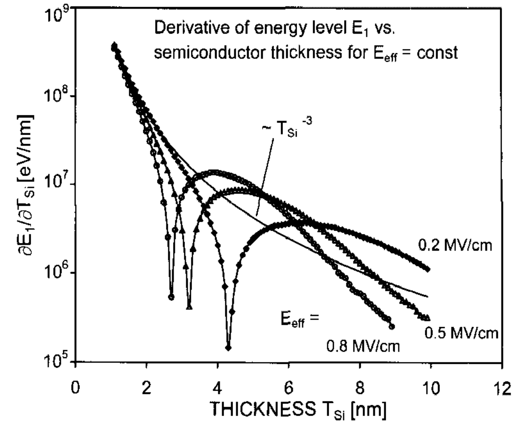

Fig. 4. A derivative of the first allowed energy level E_I with respect to the semiconductor thickness, $\partial E_I/\partial T_{Si}$, obtained for symmetrical DG SOI and plotted versus silicon thickness T_{Si} at constant effective fields. The derivative follows the $(T_{Si})^{-3}$ curve (as for an ideal rectangular well) only in very small range of the semiconductor thickness.

dominant in low temperatures and low effective fields [19]. However, in thicker structures this simple dependency is not valid. As show self-consistent results obtained for DG SOI structure (Fig. 4), the derivative of the first allowed energy level, E_I, follows the $(T_{Si})^{-3}$ dependency up to the thickness of only ca. 3 nm for weak effective field, whereas for stronger effective fields this boundary thickness falls down even below 2 nm. Moreover, the $\partial E_I/\partial T_{Si} = f(T_{Si})$ dependency dynamically changes its character, reflecting the evolution of the potential well "experienced" by electrons occupying the considered energy level, from rectangular, through parabolic to triangle-like, while increasing the semiconductor thickness. Therefore, we derived the matrix elements (2) numerically. The exponential spectrum with the rms values of Δ_{TSi} in the range 0.2 - 0.4 nm and the correlation length λ_{Si}=1.5 nm was assumed. In the SGOI devices, both strained-Si layers were deviated symmetrically, in a correlated manner. The same methodology was employed to analyze deviations of the SiGe layer SGOI structures, with the same parameters Δ_{TSiGe} = 0.2 - 0.4 nm and λ_{SiGe}=1.5 nm. For these structures also alloy scattering was considered, following the approach of [59] proposed for 2DEG, with the alloy scattering potential E_{all} = 0.8 eV.

III. RESULTS

Fig. 5 presents a comparison of the calculated effective

electron mobility vs. electron inversion density N_{inv} for the DG SOI device (along with experimental data from [11] and [12]), the DG SSOI device, and the DG SGOI of the configuration 3 nm/6 nm/3 nm, as defined previously. In this figure the total impact of thickness deviations is shown, i.e., including the oxide thickness deviations, the Si/sSi thickness deviations, and the SiGe thickness deviations, with a moderate rms magnitude of Δ_{Tox} = $\Delta_{TS/sSi}$ = Δ_{TSiGe} = 0.2 nm. As can be seen, with the moderately selected rms $\Delta_{Tox/Si/SiGe}$ values of 0.2 nm, the impact of the thickness deviations is also moderate. It is a little bit more pronounced for the SGOI device due to its more complicated structure, and for the higher germanium content, since the electron distribution is then closer to the SiO_2/Si interface. More detailed analysis for the SGOI device may be done referring to Fig. 6, in which three components of the thickness deviations limited mobility are shown, namely the mobility $\mu_{\Delta Tox}$ due to the oxide thickness deviations (open symbols), the mobility $\mu_{\Delta sSi}$ due to the strained-Si thickness deviations (closed symbols), and the mobility $\mu_{\Delta SiGe}$ due to the SiGe layer thickness deviations (crossed symbols). The results of $\mu_{\Delta Tox}$ and $\mu_{\Delta sSi}$ are for a single configuration of 3/6/3 nm and for various rms $\Delta_{Tox/sSi}$ values. The $\mu_{\Delta SiGe}$ mobility is shown for a single Δ_{TSiGe} rms value of 0.4 nm, i.e., the "worst case", and for the three configurations: 3/6/3 nm, 2.5/7/2.5 nm, and 2/8/2 nm. As can be seen, the mobilities $\mu_{\Delta Tox}$ and $\mu_{\Delta sSi}$ have opposite trends versus the inversion density N_{inv}. The $\mu_{\Delta Tox}$ component becomes stronger (i.e., decreases) as the inversion charge increases. It should be noted that this type of scattering is still significant in the range of higher N_{inv} densities, even though the screening effect has been included. On the contrary, the $\mu_{\Delta sSi}$ component dominates for lower charge densities, where the potential well is most "rectangular-like" and energy levels are most sensitive to the variations of the potential well. Moreover, a significant $\mu_{\Delta sSi}$ mobility maximum can be seen in the range of N_{inv}, in which the first allowed energy level E_1, the most significant one, enters the "triangle" of the well, i.e., drops below the potential E_{Css} at the strained-Si/SiGe interface (see Fig. 2 and Fig. 7). However, this gain in mobility is canceled by the $\mu_{\Delta Tox}$ component dominating in this range of N_{inv}. The component due to deviations of the SiGe layer thickness turns out to be negligible. Actually, according to the

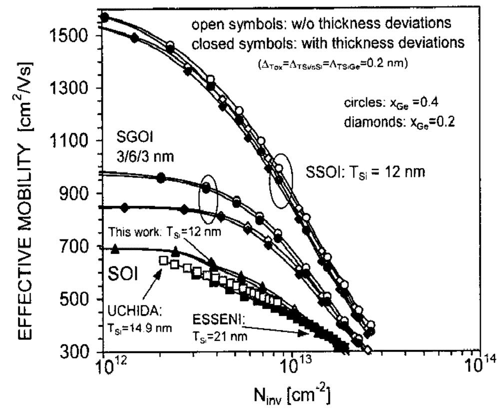

Fig. 5. Calculated electron mobility vs. the inversion charge density for the three types of modeled DG devices: SOI, SSOI, and SGOI (one configuration of 3/6/3 nm). Impact of thickness deviations is shown as well as the impact of germanium content for strained-Si devices. Experimental data of Uchida [11] and Esseni [12] for DG SOI MOSFETs are also included.

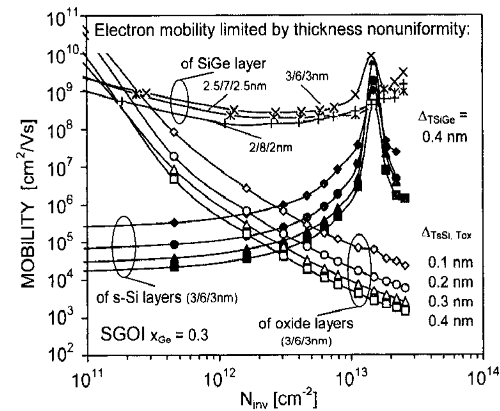

Fig. 6. Mobility components due to thickness nonuniformity in SGOI devices: of the oxide layers (open symbols), of the both strained-Si layers (closed symbols), and of the central SiGe layer (cross symbols).

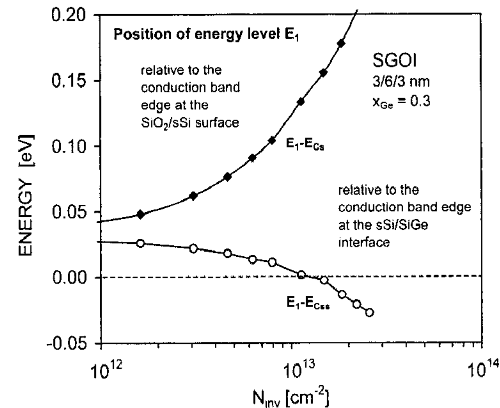

Fig. 7. Position of the first allowed energy level E1 relative to the conduction band edge: at the SiO_2/sSi interface ($E_1 - E_{Cs}$, closed symbols), and at the sSi/SiGe interface ($E_1 - E_{Css}$, open symbols).

formulated model, the thickness of the SiGe layer does not affect the subband energy levels very much, since they are located (at least the most significant of them) below the steps created by the sSi/SiGe interfaces. However, this result may be misleading, because there is a doubt if the effects of surface roughness (the lateral shifts of the potential) and thickness deviations (the quantized energy levels fluctuations) may be completely separated and treated absolutely independently.

Another investigated effect is the dependence of the electron mobility on the actual (SGOI) and equivalent (SSOI) germanium content x_{Ge} for devices with strained silicon channels. Two x_{Ge} levels, 0.2 and 0.4, have been compared, corresponding to the strain levels of 0.75% and 1.54%, respectively [21]. It has been proven that SSOI layers retain the strain after removing the SiGe layer in a wide range of thicknesses of SSOI layers [31,32]. Because the stress retainers in the SSOI case are the oxide layers, it is a matter of investigation to find the boundary ratio of oxide/SSOI thicknesses for which the strain will be maintained in the SSOI layer. Nevertheless, in this work we have assumed similar strain levels for SSOI devices as well as for SGOI structures.

It is believed, in the context of electron transport in strained Si, that the advantageous effect of the tensile strain is mainly due to splitting between the two-fold valleys and four-fold valleys with the resulting valley repopulation and separation, promoting transport in the plane of the channel and suppressing intervalley scattering. However, similar valley splitting and repopulation, obtained basing on the quantum-mechanical description of the channel, occurs when the inversion layer of a MOSFET is narrowed, either electrically, by applying strong gate bias and inducing strong transverse field, or "physically" in UTB devices. Due to overlapped effects of strain and quantum narrowing, one could expect a diminishing influence of strain on electron mobility in the above described conditions. However, reported mobility enhancement relative to relaxed Si channels is still significant for high gate biases, making modeling of the mobility in strained devices troublesome and the theoretical explanation not satisfactory. In order to reflect experimental data, electron mobility models must be modified, for example by increasing the intervalley phonon coupling [44] (this approach being followed in this paper) or reducing the strength of the interface roughness scattering in strained channels [24].

The calculated dependence on x_{Ge} is much stronger for SGOI devices than for SSOI. The explanation of this effect may be supported by the analysis of the alloy scattering affecting electrons residing in the SiGe layer of a SGOI device. As can be seen in Fig. 8, the alloy scattering noticeably suppresses the effective mobility in SGOI devices, particularly strongly for the 2/8/2 nm configuration, i.e., with the thinnest strained-Si layers and thickest SiGe layer, and especially for lower ranges of N_{inv}, where a significant portion of electrons still resides in the SiGe layer (Fig. 3). An increase of the germanium content x_{Ge} increases the conduction band discontinuity at the sSi/SiGe border and "sweeps" the electrons down to the deepened wells of the strained-Si layers. This effect prevails the corresponding increase of alloy scattering for higher x_{Ge} values, thus the net effect being said significant increase of the electron mobility.

The effective electron mobility for all simulated devices is summarized in Fig. 9. Not surprisingly, in this comparison the SiGe free SSOI device gives the highest electron mobility since it does not suffer from adverse effects resulting from channel narrowing nor the presence of actual SiGe layer. Also, the mobility enhancement factor relative to the relaxed SOI has been compared in Fig. 10, which includes experimental data extracted from [32] for SSOI (single gate operated, silicon thickness of 19 nm). The calculated mobility enhancement for SSOI expresses the issues discussed in the previous paragraph. Namely, according to the theoretical model the strain effect becomes consumed already at smaller electron densities

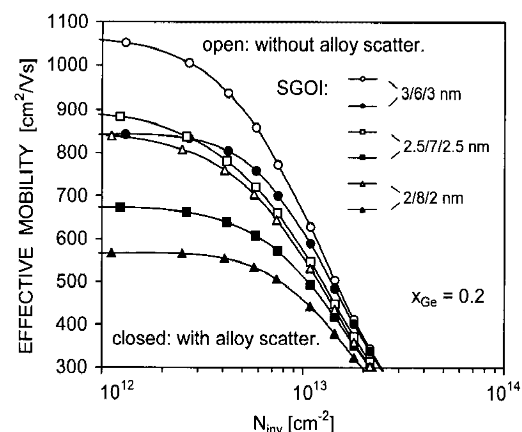

Fig. 8. Illustration of the impact of the alloy scattering on the electron mobility for SGOI devices of different sSi/SiGe/sSi configurations.

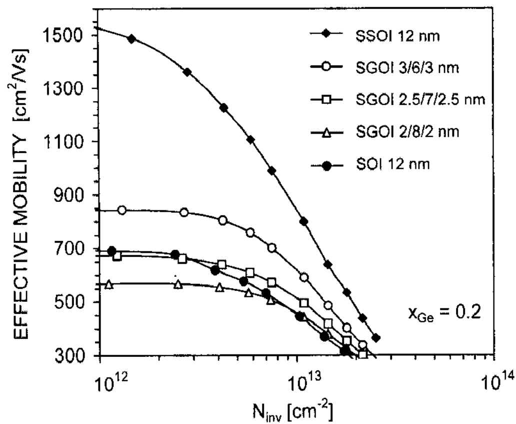

Fig. 9. Calculated effective electron mobility vs. inversion charge density for all modeled devices and one value of the germanium content for devices with strained-Si channels (SSOI and SGOI).

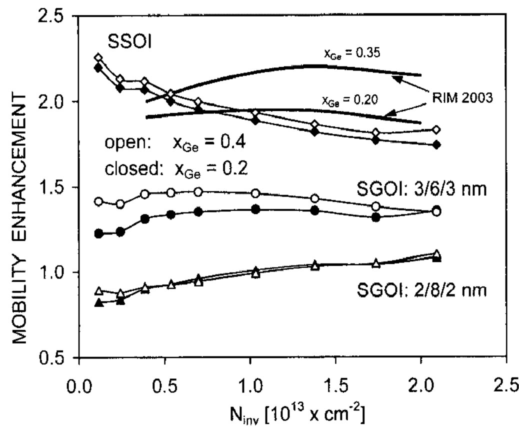

Fig. 10. Electron mobility enhancement factor (relative to relaxed-Si DG SOI) for devices with strained-Si channels with two values of the germanium content xGe. Also, experimental results extracted from [32] are included for SSOI.

and germanium content. The obtained enhancement factor decreases with increasing the electron density and transverse field, where even in a relaxed channel phenomena occur attributed to the net effect of strain. Moreover, an increase of the equivalent germanium content form 0.2 to 0.4 and related increase of strain does not improve the mobility significantly. This result is against the observed experiments in which even smaller increase of germanium content (0.2 to 0.35) induces much stronger electron mobility improvement, the improvement not exhibiting such explicitly decreasing character toward higher electron densities.

Performance of the SGOI devices strongly depends on the thicknesses of the component sSi/SiGe/sSi layers. Also, the dependency on the Ge content, which may be a tool for improving the gain electron mobility, depends on the device configuration. For the 3/6/3 nm configuration, which has the thickest strained-Si layers, electron mobility still reaches an enhancement of about 1.3 even for the lowest considered value of x_{Ge} = 0.2. However, electron mobility for the configuration with the thinnest strained-Si layers, 2/8/2 nm, in a wide range of inversion density significantly drops below the reference level defined by the relaxed SOI, particularly at small electron densities with the enhancement factor being 0.8-0.9, the factor merely reaching a value of 1.1 only for the highest N_{inv} densities. The enhancement factor may be improved by increasing the germanium content, however, as the calculations suggest, the improvement is efficient mainly for SGOI devices of the 3/6/3 nm configuration. As shows more detailed analysis of the mobility components for 2/8/2 nm configuration (Fig. 11), an increase of germanium content sweeps electrons out from the SiGe layer towards the side channel layers, thus weakening the net effect of alloy scattering. However, this gain in mobility is reduced, and actually almost lost in the considered case, because of increased surface roughness scattering experienced in the channels due to increased band bending and transverse electric field induced in these regions.

IV. CONCLUSIONS

Electron mobility has been studied in 12 nm thick DG MOSFETs of different types: a relaxed-Si DG SOI, a strained-Si DG SSOI (not containing a SiGe layer), and a strained-Si DG SGOI (containing a centrally located SiGe layer). The SSOI device exhibits the highest electron

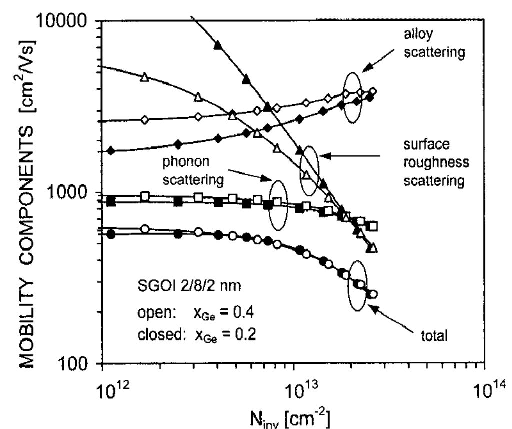

Fig. 11. Electron mobility components for the SGOI 2/8/2 nm device compared for two germanium contents of 0.2 and 0.4.

mobility with significant enhancement factor (from 1.7 to 2.3) relative to the relaxed-Si DG SOI MOSFET, and minor dependence on the equivalent x_{Ge}-content. On the contrary, the electron mobility in the simulated SGOI devices is determined mainly by their internal structure, i.e., the thicknesses of their component layers sSi/SiGe/sSi. This is due to the fact that electrons in these devices are confined in two strained-Si side-channels, which are much narrower than the channel in the homogenous devices, SOI and SSOI. Additionally, significant portion of electrons suffer from alloy scattering, which is absent in SiGe free devices. The influence of the alloy scattering on the effective mobility may be reduced by an increase of the germanium content in the SiGe layer. The resulting increase of the conduction band edge discontinuity reduces the electron concentration in the SiGe layer. Therefore, SGOI devices exhibit strong sensitivity to the germanium content in the SiGe layer. However, for SGOI devices with the thinnest strained-Si layers (2/8/2 nm configuration) the effective electron mobility may drop below values for relaxed DG SOI, thus loosing the expected mobility enhancement, and, moreover, an increase of the germanium content above 0.2 does not improve the effec-tive mobility significantly due to increased surface roughness scattering.

Other scattering mechanisms, not considered in this paper, include the surface optical phonon modes [57] and the effect of the acoustic phonon confinement [60]. Also, short-range and long-range Coulomb interactions have been predicted to affect significantly the transport of electrons in the MOSFET's channel [43,42]. The importance of the mentioned effects is especially evident in ultrathin devices, so they may introduce still further degradation of electron mobility, particularly in the SGOI devices, which contain strained-Si channels in the ultrathin range.

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REFERENCES

[1] H.-S. P. Wong, "Beyond the conventional transistor," *IBM J. Res. & Dev.*, Vol.46, No.2/3, pp.133-167, May 2002.

[2] D. A. Buchanan, "Beyond microelectronics: materials and technology for nano-scale CMOS devices," *phys. stat. sol.* (c) 1, No. S2, pp.S155-S162, 2004.

[3] International Technology Roadmap in Semiconductors (ITRS).

[4] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance," *IEEE Electron Device Lett.*, Vol.ED-8, pp.410-412, Sept. 1987.

[5] J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-on-insulator gate-all-around device," in *IEDM Tech. Dig.*, pp.595-598, 1990.

[6] D. Hisamoto, T. Kaga, and E. Takeda, "Impact of the vertical SOI 'Delta' structure on planar device technology," *IEEE Trans. Electron Devices*, Vol.38, pp.1419-1424, June 1991.

[7] B. Majkusiak, T. Janik, and J. Walczak, "Semiconductor thickness effects in the double-gate SOI MOSFET," *IEEE Trans. Electron Devices*, Vol.45, No.5, pp.1127-1134, May 1998.

[8] H.-S. Wong, D. Frank, and P. Solomon, "Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation," in *IEDM Tech. Dig.*, pp.407-410, 1998.

[9] F. Gámiz and M. V. Fischetti, "Monte Carlo simulation of double-gate silicon-on-insulator inversion layers: The role of volume inversion," *J. Appl. Phys.*, Vol.89, pp.5478-5487, 2001.

[10] F. Gámiz, J. B. Roldan, A. Godoy, and F. Jimenez-Molinos, "Double gate silicon-on-insulator transistors: n^+-n^+ gate versus n^+-p^+ gate configuration," in *Proc. IEEE ESSDERC*, pp.173-176, 2004.

[11] K. Uchida , J. Koga, and S. Takagi, "Experimental study on carrier transport mechanisms in double- and single-gate ultrathin-body MOSFETs – Coulomb scattering, volume inversion, and δTSOI-induced scattering," in *IEDM Tech. Dig.*, pp.805-808, 2003.

[12] D. Esseni, M. Mastrapasqua, G. K. Celler, C. Fiegna, L. Selmi, and E. Sangiorgi, "An Experimental Study of Mobility Enhancement in Ultrathin SOI Transistors Operated in Double-Gate Mode," *IEEE Trans. Electron. Devices*, Vol.50, No.3, pp.802-808,

Mar. 2003.

[13] G. Tsutsui , M. Saitoh, T. Saraya, T. Nagumo, and T. Hiramoto, "Mobility enhancement due to volume inversion in (110)-oriented ultra-thin body double-gate nMOSFETs with body thickness less than 5 nm," in *IEDM Tech. Dig.*, pp.747-750, 2005.

[14] V. Sverdlov, E. Ungersboeck, H. Kosina, and S. Selberherr, "Volume inversion mobility in SOI MOSFETs for different thin body orientations," *Solid-State Electron.*, Vol.51, pp.299-305, 2007.

[15] S. Takagi, J. Koga, and A. Toriumi, "Subband structure engineering for performance enhancement of Si MOSFETs," in *IEDM Tech. Dig.*, pp.219-222, 1997.

[16] F. Gámiz, J. A. Lopez-Villanueva, J. B. Roldan, J. E. Carceller, and P. Cartujo, "Monte Carlo Simulation of Electron Transport Properties in Extremely Thin SOI MOSFET's," *IEEE Trans. Electron. Devices*, Vol.45, pp.1122-1126, May 1998.

[17] M. Shoji and S. Horiguchi, "Electronic structures and phonon-limited electron mobility of double-gate silicon-on-insulator Si inversion layers," *J. Appl. Phys.*, Vol.85, No.5, pp.2722-2731, 1999.

[18] D. Esseni, M. Mastrapasqua, G. K. Celler, C. Fiegna, L. Selmi, and E. Sangiorgi, "Low field electron and hole mobility of SOI transistors fabricated on ultrathin silicon films for deep submicrometer technology application," *IEEE Trans. Electron. Devices*, Vol.48, No.12, pp.2842-2850, Dec. 2001.

[19] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental study on carrier transport mechanism in ultrathin-body SOI nand p-MOSFETs with SOI thickness less than 5 nm," in *IEDM Tech. Dig.*, pp.47-50, 2002.

[20] R. People, "Physics and applications of Ge_xSi_{1-x}/Si strained-layer heterostructures," *J. Quant. Elec.*, Vol.QE-22, pp.1696-1710, 1986.

[21] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys.*, Vol.80, No.4, pp.2234-2252, 1996.

[22] P. R. Chidambaram, C. Bowen, S. Chakravarthi, C. Machala, and R. Wise, "Fundamentals of silicon material properties for successful exploitation of strain engineering in modern CMOS manufacturing," *IEEE Trans. Electron Devices*, Vol.53, No.5, pp.944-964, May 2006.

[23] D. Rideau, M. Feraille, L. Ciampolini, M. Minondo, C. Tavernier, H. Jaouen, and A. Ghetti, "Strained Si, Ge, and Si1-xGex alloys modeled with a first-principles-optimized full-zone k·p method," *Phys. Rev. B*, Vol.74, No.19, pp.195208-1-195208-20, 2006.

[24] M. V. Fischetti, F. Gámiz, and W. Hänsch, "On the enhanced electron mobility in strained-silicon inversion layers," *J. Appl. Phys.*, Vol.92, No.12, pp.7320-7324, 2002.

[25] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, "Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, Vol.97, No.011101, pp.1-27, 2005.

[26] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, et al., "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," in *IEDM Tech. Dig.*, pp.978-980, 2003.

[27] K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, et al., "Delaying forever: Uniaxial strained silicon transistors in a 90 nm CMOS technology," in *VLSI Symp. Tech. Dig.*, pp. 50-51, 2004.

[28] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap," *IEEE Trans. Electron Devices*, Vol.53, No.5, pp.1010-1020, May 2006.

[29] S. Takagi, T. Mizuno, T. Tezuka, N. Sugiyama, T. Numata, K. Usuda, et al., "Channel structure design, fabrication and carrier transport properties of strained-Si/SiGe-on-insulator (strained-SOI) MOSFETs," in *IEDM Tech. Dig.*, pp.57-60, 2003.

[30] T. Mizuno, N. Sugiyama, T. Tezuka, T. Numata, S. Takagi, "High performance strained-SOI CMOS devices using thin film SiGe-on-insulator technology," *IEEE Trans Electron Devices*, Vol.50, No.4, pp. 988-994, 2003.

[31] T. A. Langdo, M. T. Currie, A. Lochtefeld, R. Hammond, J. A. Carlin, M. Erdtmann, et al., "SiGe-free strained Si on insulator by wafer bonding and layer transfer," *Appl. Phys. Lett.*, Vol.82, No.24, pp.4256-4258, June 2003.

[32] K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, et al., "Fabrication and mobility charac-

teristics of ultra-thin strained-Si directly on insulator (SSDOI) MOSFETs," in *IEDM Tech. Dig.*, pp.49-52, 2003.

[33] I. Aberg, O.O. Olubuyide, C.N. Chleirigh, I. Lauer, D.A. Antoniadis, J. Li, R. Hull, and J.L. Hoyt, "Electron and hole mobility enhancements in sub-10 nm-thick strained silicon directly on insulator fabricated by a bond and etch-back technique," in *VLSI Symp. Tech. Dig.*, pp.52-53, 2004.

[34] W. F. Clark, D. M. Fried, L. D. Lanzerotti, and E. J. Nowak, "Strained FIN FETS structure and method," U.S. Patent 6 635 909 B2, October 21, 2003.

[35] N. Barin, C. Fiegna, E. Sangiorgi, "Analysis of strained-silicon-on-insulator double-gate MOS structures," in *Proc. IEEE ESSDERC*, pp.169-172, 2004.

[36] T. Mizuno, N. Sugiyama, T. Tezuka, Y. Moriyama, S. Nakaharai, and S. Takagi., "(110)-Surface strained-SOI CMOS devices," *IEEE Trans. Electron Devices*, Vol.52, No.3, pp.367-374, Mar. 2005.

[37] T. Krishnamohan, D. Kim, C. D. Nguyen, C. Jungemann, Y. Nishi, and K. C. Saraswat, "High-mobility low band-to-band-tunneling strained-germanium double-gate heterostructure FETs: simulations," *IEEE Trans. Electron Devices*, Vol.53, No.5, pp. 1000-1009, May 2006.

[38] P. Palestri, N. Barin, D. Brunel, C. Busseret, A. Campera, P. A. Childs, et al., "Comparison of Modeling Approaches for the Capacitance–Voltage and Current–Voltage Characteristics of Advanced Gate Stacks," *IEEE Trans. Electron Devices*, Vol.54, No.1, pp.106-114, Jan. 2007.

[39] L. Yang, J. R. Watling, R. C. W Wilkins, M. Boriçi, J. R. Barker, A. Asenov, and S. Roy, "Si/SiGe heterostructure parameters for device simulations," *Semicond. Sci. Technol.*, Vol.19, pp.1174-1182, 2004.

[40] V. Venkataraman, C. W. Liu, and J. C. Sturm, "Alloy scattering limited transport of two-dimensional carriers in strained $Si_{1-x}Ge_x$ quantum wells," *Appl. Phys. Lett.*, Vol.63, No.20, pp.2795-2797, 1993.

[41] D. Vasileska and S. S. Ahmed, "Narrow-width SOI devices: the role of quantum-mechanical size quantization effect and unintentional doping on the device operation," *IEEE Trans. Electron Devices*, Vol.52, pp.227-236, February 2005.

[42] M. V. Fischetti, "Long-range Coulomb interactions in small Si devices. Part II. Effective electron mobility in thin-oxide structures," *J. Appl. Phys.*, Vol.89, No.2, pp.1232-1250, 2001.

[43] W.J. Gross, D. Vasileska, and D.K. Ferry, "Ultrasmall MOSFETs: the importance of the full Coulomb interaction on device characteristics," *IEEE Trans. Electron. Devices*, Vol.47, No.10, pp.1831-1837, Oct. 2000.

[44] S-I. Takagi, J. L. Hoyt, J. J. Welser, and J. F. Gibbons, "Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, Vol.80, No.3, pp.1567-1577, 1996.

[45] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials," *Rev. Mod. Phys.*, Vol.55, No.3, pp.645-705, 1983.

[46] T. Ando, A. B. Fowler, and F. Stern., "Electronic properties of two-dimensional systems," *Rev, Mod. Phys.*, Vol.54, pp.437-672, 1982.

[47] F. Gámiz, J. B. Roldán, J. A. López-Villanueva, P. Cartujo-Cassinello, and J. E. Carceller, "Surface roughness at the Si–SiO_2 interfaces in fully depleted silicon-on-insulator inversion layers," *J. Appl. Phys.*, Vol.86, No.12, pp.6854-6863, 1999.

[48] M. V. Fischetti, Z. Ren, P. M. Solomon, M. Yang, and K. Rim, "Six-band k·p calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain, and silicon thickness," *J. Appl. Phys.*, Vol.94, No.2, pp.1079-1095, 2003.

[49] S. M. Goodnick, D. K. Ferry, C. W. Wilmsen, Z. Liliental, D. Fathy, and O. L. Krivanek, "Surface roughness at the Si(100)-SiO_2 interface," *Phys. Rev. B*, Vol.32, No.12, pp.8171-8186, 1985.

[50] J. Li and T.-P. Ma, "Scattering of silicon inversion layer electrons by metal/oxide interface roughness," *J. Appl. Phys.*, Vol.62, No.10, pp.4212-4215, 1987.

[51] J. Walczak and B. Majkusiak, "The remote roughness mobility resulting from the ultrathin SiO_2 thickness nonuniformity in the DG SOI and bulk MOS transistors," *Microelectronic Engineering*, Vol.59, No.1-4, pp.417-421, 2001.

[52] F. Gámiz, A. Godoy, F. Jimenez-Molinos, P. Cartujo-Cassinello, and J. B Roldan, "Remote sur-

face roughness scattering in ultrathin-oxide MOSFETs," in *Proc. IEEE ESSDERC*, pp.403-406, 2003.

[53] A. Gold, "Electronic transport properties of a two-dimensional electron gas in a silicon quantum-well structure at low temperature," *Phys. Rev. B*, Vol.35, No.2, pp.723-733, 1987.

[54] H. Sakaki, T. Noda, K. Hirakawa, M. Tanaka, and T. Matsusue, "Interface roughness scattering in GaAs/AlAs quantum wells," *Appl. Phys. Lett.*, Vol. 51, No.23, pp.1934-1936, 1987.

[55] C-Y. Mou and T-m. Hong, "Transport in quantum wells in the presence of interface roughness," *Phys. Rev. B*, Vol.61, No.19, pp.12612-12615, 2000.

[56] K. Uchida and S. Takagi, "Carrier scattering induced by thickness fluctuation of silicon-on-insulator film in ultrathin-body metal-oxide-semiconductor field-effect transistors," *Appl Phys Let.*, Vol.82, No.17, pp.2916-2918, 2003.

[57] D. Esseni, A. Abramo, L. Selmi, and E. Sangiorgi, "Physically based modeling of low field electron mobility in ultrathin single- and double-gate SOI n-MOSFETs," *IEEE Trans. Electron. Devices*, Vol. 50, No.12, pp.2445-2455, Dec. 2003.

[58] T. Low, Li Ming-Fu, G. Samudra, Yeo Yee-Chia, Zhu Chunxiang, A. Chin, and Kwong Dim-Lee, "Modeling study of the impact of surface roughness on silicon and germanium UTB MOSFETs," *IEEE Trans. Electron. Devices*, Vol.52, No.11, pp.2430-2439, Nov. 2005.

[59] F. Monsef, P. Dollfus, S. Galdin-Retailleau, H.-J. Herzog, and T. Hackbarth, "Electron transport in Si'SiGe modulation-doped heterostructures using Monte Carlo simulation," *J. Appl. Phys.*, Vol.95, No.7, pp.3587-3593, 2004.

[60] L. Donetti, F. Gámiz, N. Rodriguez, F. Jimenez, and C. Sampedro, "Influence of acoustic phonon confinement on electron mobility in ultrathin silicon on insulator layers," *Appl. Phys. Lett.*, Vol.88, No.12, pp.122108(1-3), 2006.

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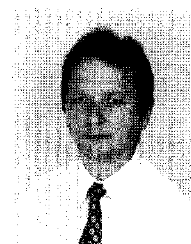

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