A Reproducible High Etch Rate ICP Process for Etching of Via-Hole Grounds in 200 μm Thick GaAs MMICs

D. S. Rawal, Vanita R. Agarwal, H. S. Sharma, B. K. Sehgal, and R. Muralidharan

***Abstract*—An inductively coupled plasma etching process to replace an existing slower rate reactive ion etching process for 60 μm diameter via-holes using Cl2/BCl3 gases has been investigated. Process pressure and platen power were varied at a constant ICP coil power to reproduce the RIE etched 200 μm deep via profile, at high etch rate. Desired etch profile was obtained at 40 mTorr pressure, 950 W coil power, 90W platen power with an etch rate ~ 4 μm/min and via etch yield >90% over a 3-inch wafer, using 24 μm thick photoresist mask. The etch uniformity and reproducibility obtained for the process were better than 4%. The metallized via-hole dc resistance measured was ~ 0.5 Ω and via inductance value measured was ~ 83 pH.**

***Index Terms*—GaAs, MMIC, via-hole, ICP, etching**

I. Introduction

The backside via-hole is one of the most critical elements for Monolithic Microwave Integrated Circuit (MMIC) technology. Electrically it provides a low inductance/resistance contact to the common grounding plane and at the same time thermally serves as a heat dissipation path for Metal Semiconductor Field Effect Transistors (MESFET) and High Electron Mobility Transistors (HEMT)[1-3]. Backside via etching is often a bottleneck of wafer production due to its crucial nature of very deep (100-200 μm) through substrate etching, after front side processing is complete. Thus, an optimized process is strongly desired to improve the wafer throughput and to reduce the cycle time. Inductively Coupled Plasma (ICP) etching has been replacing conventional reactive ion etching (RIE) for GaAs backside via etching because of several advantages. Throughput improvement utilizing significantly faster etching rate have already been reported in the literature [4,5]. Furthermore, the ICP tools provide better control of via size, repeatability and reproducebility [6].

The ICP tools produce significantly different via dimension as compared to the conventional RIE tools, if the same size mask used, due to its nature of etching process. Generally, ICP produces a vertical profile utilizing low pressure and higher ion density process while RIE produces a conical shape. The etch profile and surface morphology of via-hole grounds is important not only for the inductance consideration but also for the success of backside metallization. The smooth morphology of the etched sidewalls provides reliable and good electrical contact with low resistance.

Etching is mainly carried out in chlorine/fluorine plasma. A number of gas combinations CCl2F2, CCl2F2/CCl4, SiCl4/Cl2, BCl3/Cl2/Ar, Cl2/Ar and Cl2/BCl3 have been utilized to fabricate via-holes [6]. Each gas combination has its advantages and disadvantages. CCl2F2 is attractive because of its excellent selectivity with respect to front-side metal (Ti/Pt/Au, Cr) and lack of corrosiveness and toxicity, but the etch rate is too low and severe polymer formation occurs on the etched area as well as on the chamber walls resulting in poor process reproducibility. Cl2/BCl3 gas mixture with ICP process is being increasingly used for fabrication of via-holes at high etch rates with excellent anisotropy and smooth surface morphology.

For the implementation of ICP backside via etching

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process into any existing RIE etching production line, it is important to understand the impact of ICP process parameters on via profile, etch rate, mask selectivity, sidewall morphology and produce same RIE via etch profile to avoid any changes in via model and circuit design. A slight change in via etch profile would lead to change in via inductance value of grounded source pad. This change in source inductance could affect the circuit performance for higher frequency application. In particular, the low noise amplifier (LNA) circuits where source impedance feedback is often used as a means to achieve more stability may be more vulnerable to the subtle unwanted source inductance changes due to the change of via dimension. Reproducing RIE etch profile with ICP process would enhance the throughput signifycantly without affecting the production using existing designs. Otherwise, all the circuit designs will have to incorporate via dimensional changes and has to go through expensive mask set fabrication step.

Generally reported etch depths using ICP/RIE for via-hole etching applications in MMIC are less than 200 μm using photoresist mask [5-8]. In this study, we are reporting the etching of 60 μm diam. via-holes, up to a depth of 200 μm, in 3- inch GaAs wafer using positive photoresist mask.

The aim of this study has been to replace the existing via-hole RIE process using CCl_2F_2/CCl_4 gases, with new reproducible ICP process using non-CFC gas chemistry (Cl_2/BCl_3), for in-house MMICs production line without changing existing MMIC designs and mask sets.

II. EXPERIMENTAL

All test samples were 650 μm thick, 3- inch S.I. GaAs wafers with front side pattern. These wafers were mounted on 82 mm diameter sapphire carrier with wax, front side facing down and thinned down to 200±10 μm by standard lapping and polishing method. The substrate thickness was kept 200 μm considering factors like handling of fragile wafers and electrical losses in MMIC micro-strip interconnects on the front side. Wafers were then coated with 24 μm thick positive photo resist AZ 4620 and exposed to define via-holes with 60 μm diameter. The patterned photoresist was post baked at 120 °C for 30 minutes to introduce a sloped photoresist profile with improved adhesion. All the wafers were etched in standard ICP system, one at a time. An oxygen plasma de-scum step prior to etching was utilized in order to remove any residual photoresist in via-hole which would otherwise contribute to the roughness of the etched surface. Plasma of etcher is inductively coupled through a coil at 13.56 MHz, with independent energy control provided by 13.56 MHz RF biasing of the wafer platen. Helium gas is used to help cool backside of the wafer. The substrate temperature was set at 20 °C for all test conditions. The etch chemistry is a mixture of Cl_2/BCl_3 through mass flow controlled process gas lines. The chamber was evacuated to a base pressure of 9E-6 Torr, by a turbomoleculer pump backed by a dry mechanical pump, before initiating the etch process. The etch gases mixture was introduced through an annular region at the top of chamber lid. ICP Process parameters like pressure and platen power were varied in a narrow window, at constant ICP coil power, to reproduce the RIE etched 200μm deep via profile at a relatively very high etch rate. The etch rate, etch depth, etch profile and surface morphology of via-holes were determined by cleaving through the etched features and examining the sample under scanning electron microscope, model LEO-1430.

III. RESULTS AND DISCUSSION

Fig. 1 shows the targeted an-isotropic etch profile of a 200 μm deep via-hole obtained with the RIE process at a relatively slow etch rate ~ 1.3 μm/min. Via profile obtained was conical in shape with 60±10 μm diameter opening on front side and 180±10 μm diameter opening on backside of wafer respectively. The details of this work

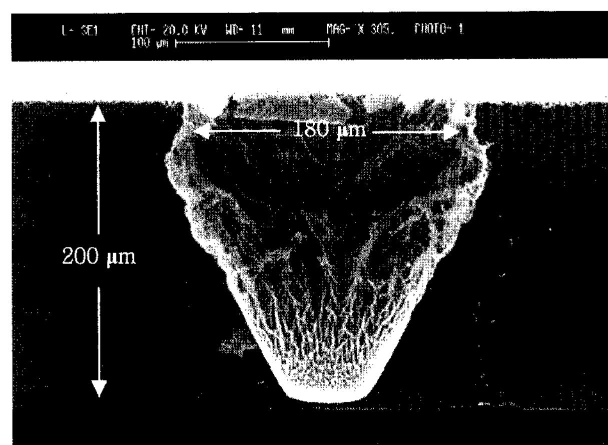

Fig. 1. 200 μm deep via etch profile obtained using standard RIE process.

are already published elsewhere [9].

All the ICP experiments were carried out at near maximum available coil power and Cl2/BCl3 flow rate ratio of 4:3 to have high plasma density [10] and increased concentration of reactive Cl species that resulted in high etch rates with better etch surface morphology. Higher than 4:3 flow rate ratio increased the etch rate but at the cost of surface morphology, whereas lower flow rate ratio decreased the etch rate significantly. Fig. 2 shows the etch rate variation with elapsed etch time for ICP process at 950 W coil power, 30 mTorr pressure and 65 W platen power. It clearly shows that the average etch rate is decreased with etch time, from 7 µm/min for 10 minute of etching to 3.9 µm/min for 45 minutes of etching on 3- inch wafer. This is due to increased depth, that reduces the effectiveness of supplying reactive species and removing etch by products. Therefore the average etch rate achieved for 100 µm etch depths is much higher than 200 µm etch depths for same diameter holes. As reported by other groups, we have also achieved an etch rate of > 6 µm/min for 100 µm depths using ICP process. However, the reduction in average etch rate with etch time is much less for the ICP process in comparison to the RIE process and etch depths of 176 µm could be achieved in just 45 minutes at 30 mTorr with controlled undercut as shown in Fig. 3. Whereas in case of RIE etch rate reduced to ~ 1.6 µm/min even at 50 mTorr pressure and etch depth of 95 µm could only be achieved in 60 minutes of etching using photoresist mask [9].

Fig. 4 shows the ICP process etch rate variation with process pressure at 950 W coil power and 80 W platen power for an etch time of 45 minutes. We have worked around 20-40 mTorr pressure as our aim was to reproduce

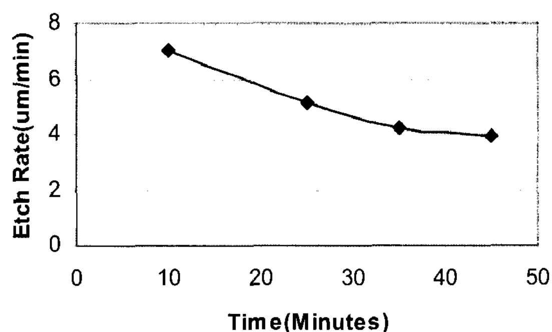

Fig. 2. ICP etch rate variation with elapsed etch time.
(Coil/Platen Power=950 W / 65 W, Pressure=30 mTorr)

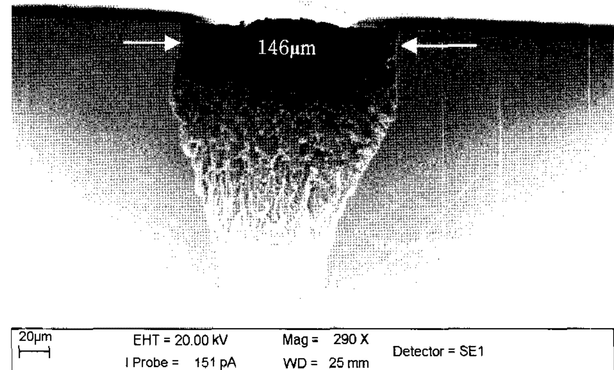

Fig. 3. ICP etched via profile obtained after 45 minutes of etching at 30mTorr.

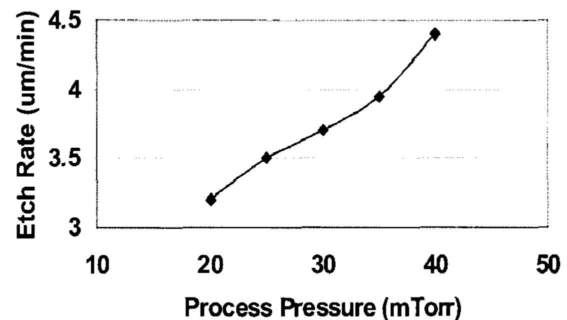

Fig. 4. Etch rate as a function of process Pressure.
(Coil Power=950W, Platen Power=80W, Etch Time=45 Min.)

the RIE etch profile with higher etch rates. It is evident from graph that the etch rate is a strong function of process pressure and is increasing with pressure due to increased density of reactive species but anisotropy is maintained mainly due to very small reduction in the ion energy incident on the substrate with 10 mTorr increase in pressure. In other words, physical component of etching is fairly constant over this narrow pressure range. Etch rate is increased to 4.4 µm/min at 40 mTorr from 3.7 µm/min at 30 mTorr, for an etch time of 45 minutes, suggesting that the process is at a reaction rate limited regime in this narrow process pressure window. Fig. 5 shows the SEM cross-section of via hole etched with 4.4 µm/min etch rate. Fig 6 shows etch rate variation as a function of platen power. Increasing platen power to 90 W at pressure 30 mTorr has resulted in reduction in etch rate to 3.6 µm/min from 3.9 µm/min at 65 W platen power for an etch time of 45 minutes contrary to normal etch rate variation with platen power at lower pressure range. R. J. Shul et al. have also reported similar trend

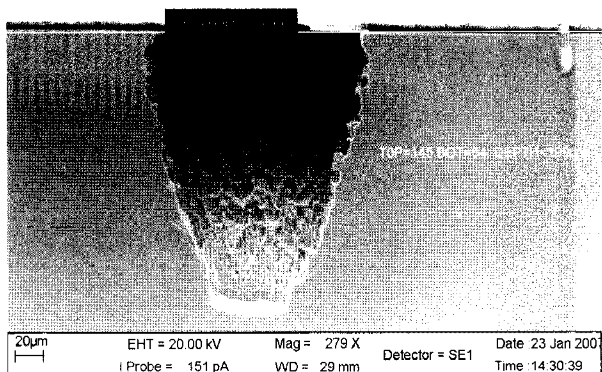

Fig. 5. SEM cross-section of via-hole etched with 4.4μm/min etch rate. (Coil Power=950W, Platen Power=80W, Etch Time=45 Min.)

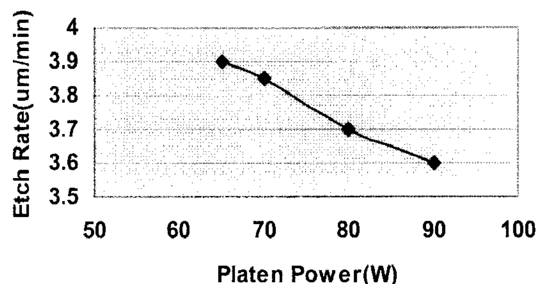

Fig. 6. Etch rate as a function of Platen power. (Coil Power=950W, Pressure =30mTorr, Etch Time=45 Min.)

with ICP process in the past [11]. This is probably due to increase in physical etching component and decrease in chemical etching component in comparatively higher pressure range at 90 W i.e. etching process is more physically driven at 90 W. This reduction in etch rate has in turn resulted into better etch sidewall morphology at 90 W, because of the higher ion bombardment that may sputter the surface evenly regardless of defects [12].

After a series of experiments it was concluded that a process pressure of 40 mTorr with platen power of 90 W are suitable for 200 μm deep, 60 μm diameter via-hole etching. This is due to the fact that etching process using these values has resulted in high etch rate with similar etched sidewall morphology as compared to the RIE process. This indicates that the ICP process would give better sidewall morphology in comparison to the RIE process at similar etch rates. Fig. 7 shows the final etch profile obtained with the ICP process at 40 mTorr pressure, 950 W coil power, 90 W of platen power for an etch time of 50 min., with via etch yield of > 90% on a

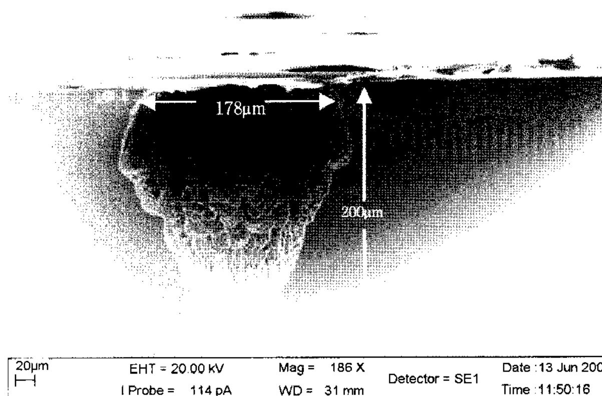

Fig. 7. ICP etched via profile at 40mTorr. (Coil Power=950W, Platen Power=90W, Etch Time=50 Min.)

full wafer. This ICP etch profile is almost similar to the RIE profile (Fig. 1) and is obtained at relatively very high etch rate of ~ 4 μm/min over a 3- inch wafer with uniformity and reproducibility better than 4%. The etch selectivity obtained with photoresist mask for this process was > 12 : 1.The etched holes were then seed metallized and gold plated to form via ground connections. Fig. 8 shows the SEM photomicrograph of gold plated hole from backside with good metal step coverage. The typical dc via-hole resistance measured was ~ 0.5 Ω and via inductance value measured was ~ 83 pH for ICP process, well within acceptable range. The typical dc via resistance and via inductance value measured for RIE process were ~ 0.5 Ω and 76 pH respectively. The slightly higher via inductance valve obtained for ICP process is mainly due to marginally better an-isotropy over 200 μm depth. Table. 1 shows the comparison of process parameters for the ICP and RIE

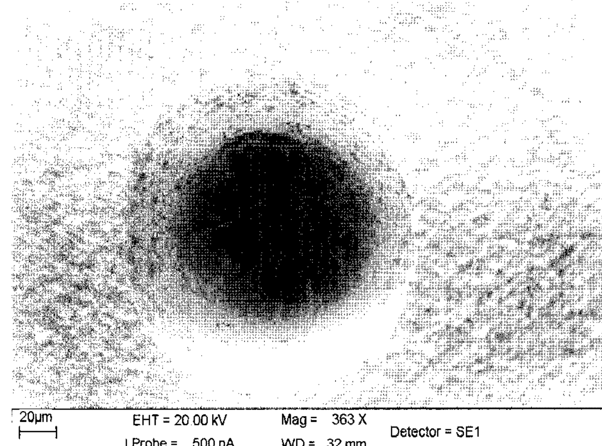

Fig. 8. SEM photomicrograph of gold plated via-hole from backside.

Table 1. RIE/ICP optimized process parameters for 60 μm diameter, 200 μm deep via-hole etching over a 3- inch wafer.

S. No.	Parameter	RIE	ICP
1.	Mask	Nickel (2000A°)	Photoresist (24μm)
2.	Gases	CCl2F2/CCl4	Cl2/BCl3
3.	Process Pressure	40mTorr	40mTorr
4.	Power	200W	950W/90W
5.	Etch Rate	~1.3μm/min.	~ 4μm/min.
6.	Selectivity	>200:1	>12:1
7.	Etch Time	180 min.	50 min.

process for etching 200 μm deep via holes on 3- inch wafer with > 90% via yield. The total etch time has been significantly reduced from 180 minutes to 50 minutes for ICP etching, with much simpler process using photo-resist mask. Finally, this high-density plasma etching process has been integrated in the production line and C-band medium power amplifiers/attenuators were fabricated with high etch rate, without changing existing MMIC designs and mask sets. These amplifiers and attenuators have performed as per the desired specifications, validating the suitability of the ICP process.

IV. Conclusions

A 200 μm deep via-hole ICP etching process has been successfully developed, to replace the existing slow etch rate RIE process on 3- inch GaAs wafers, using Cl2/BCl3 gases for the in-house MMIC production line. Desired an-isotropic etch profile for 60 μm diameter via-hole was obtained at 40 mTorr pressure, 950 W coil power, 90 W of platen power at an etch rate of ~ 4 μm/min and via etch yield of > 90% over a full wafer, with very good uniformity and reproducibility. The ICP process has resulted in high etch rate with acceptable etched sidewall morphology as compared to the RIE process. Finally, this high-density plasma etching process has been integrated in production line for fabrication of MMIC's with high throughput, without affecting the production using existing designs and mask sets.

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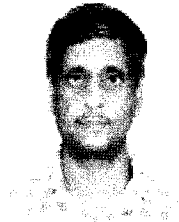

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