Enhanced f_T and f_{MAX} SiGe BiCMOS Process and Wideband Power Efficient Medium Power Amplifier

Hyun-Cheol Bae* and Seung-Hyeub Oh**

Abstract—**In this paper, a wideband power efficient 2.2 GHz - 4.9 GHz Medium Power Amplifier (MPA) has been designed and fabricated using 0.8 μm SiGe BiCMOS process technology. Passive elements such as parallel-branch spiral inductor, metal-insulator-metal (MIM) capacitor and three types of resistors are all integrated in this process. This MPA is a two stage amplifier with all matching components and bias circuits integrated on-chip. A P1dB of 17.7 dBm has been measured with a power gain of 8.7 dB at 3.4 GHz with a total current consumption of 30 mA from a 3 V supply voltage at 25 °C. The measured 3 dB bandwidth is 2.7 GHz and the maximum Power Added Efficiency (PAE) is 41%, which are very good results for a fully integrated Medium PA. The fabricated circuit occupies a die area of 1.7 mm × 0.8 mm.**

Index Terms—**SiGe, BiCMOS, MPA, inductor, capacitor**

I. INTRODUCTION

To meet the growing demand for multi-gigabit data communication systems and wide bandwidth radio communication systems, devices achieving both high speed digital operation with sophisticated functions and high frequency analog operation are the key components for ICs LSIs constructing such systems. SiGe hetero-junction bipolar transistor (HBT), strained silicon mosfet and HBTs with CMOS transistors (BiCMOS) technologies play an important role in optical transmission and wireless communication systems [1]. SiGe BiCMOS devices are used in such a wide range of applications because they are superior to conventional homojunction silicon bipolar devices in every important performance metric. In fact, SiGe with bandgap engineering enables process designers to satisfy product requirements for simultaneous high cutoff frequency (f_T), maximum oscillation frequency (f_{max}), current gain, power consumption, Early voltage (V_A), and breakdown voltage (BV_{CEO}) [2,3]. These advantages are originated from two factors; one is the smaller band gap of SiGe than that of Si, and the other is the epitaxial growth of SiGe layers that realizes the base of high doping concentration and small width.

The fabrication technology of SiGe BiCMOS RFIC, since it uses strong points of CMOS and HBT simultaneously, would not only contribute to the development of RFIC products with competitiveness, but also hold advantage for producing at low cost using silicon-based facilities. Therefore, the degree of application is expected significantly high.

In general, ultra high vacuum chemical vapor deposition (UHVCVD) process has been adopted for the SiGe BiCMOS process because of the purity-assisted improvement of device characteristics. However, low throughput and high cost of the UHVCVD becomes a barrier to be overcome at an industrial point of view, giving a chance to reduced pressure CVD (RPCVD) as an alternative.

In this paper, we developed the low cost and high performance SiGe BiCMOS process using reduced pressure chemical vapor deposition (RPCVD) process. All passive elements were integrated in the process. We presented the self-aligned SiGe HBTs having the higher f_T and f_{max} by adopting the extrinsic-base selective epitaxial growth (SEG) and selective collector implantation

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(SCI) and verified the SiGe BiCMOS devices through a fully integrated Medium Power Amplifier. It was designed and fabricated on-chip, using the SiGe BiCMOS process. All matching components and bias circuits were integrated on the chip, requiring no external tuning components.

II. Characteristics of Active and Passive Devices

The technology used in this work is a 0.8 μm SiGe BiCMOS process with 2 metal layers and conventional local oxidation of silicon (LOCOS) process to define and isolate the active regions. SiO_2 layers of 100 nm thick are formed on P-type Si <100> wafers which are used as starting substrates. In-situ heavily doped Si/SiGe/Si base layers and other Si epitaxial layers are grown in RPCVD system. The base layer is composed of the 40 nm thick cap Si layer, the 40 nm thick SiGe layer, and the 40 nm thick seed Si layer, and its total thickness was 120 nm. The Ge concentration is gradually increased from the cap layer to the seed layer, reaching to the maximum of 20 atomic percent. Boron (B) is in-situ doped in the SiGe layer, and its maximum concentration is 4×10^{19} atoms/cm^3. Heavily doped buried layers are formed by As implantation, and the definition and the isolation of active regions are achieved by the LOCOS process. Self-aligned Ti silicide on Si/SiGe/Si base is formed in a rapid thermal annealing (RTA) chamber by the two step annealings [4]. The first and second annealings are performed at 830 °C for 10 sec, and 850 °C for 30 sec, respectively.

We have four typed SiGe HBT library. And this is comprised of the different structures (1) standard, (2) SEG, (3) SCI and (4) both SEG & SCI. Fig. 1 and 2 show the cross-sectional view of the standard HBT and simplified process flow for the SiGe BiCMOS production technology, respectively. We have used the RPCVD system to grow Si/SiGe/Si base layers and other Si epitaxial layers.

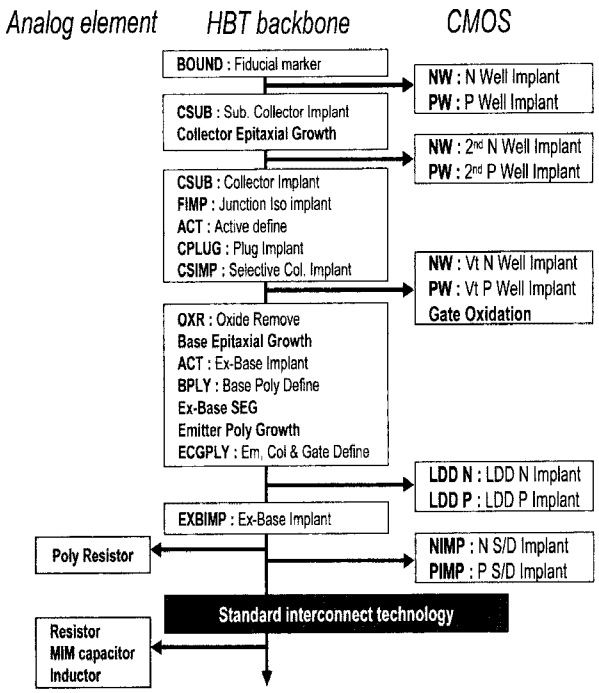

Fig. 2. Simplified process flow for the SiGe BiCMOS technology.

Based on the measured scattering parameters, each structures and RF characteristics are shown at several bias points as shown in Fig. 3. The maximum f_T and f_{max} values of standard SiGe HBT with 0.5×6 μm^2 emitter area are 46 GHz and 42 GHz, respectively. The cutoff frequency is higher at Structure-C (67 GHz) and -D (71 GHz) adopting SCI process. Since, the critical current causing the Kirk effect is shifted towards the high current. On the other hand, f_{max} is higher at Structure-B (51 GHz) and -D (51 GHz) adopting extrinsic-base SEG, because increase of base thickness leaded to decrease of base resistance. Both f_T and f_{max} is higher at Structure-D adopting both SCI and extrinsic-base SEG. For high-frequency RF/microwave operation, the structure with

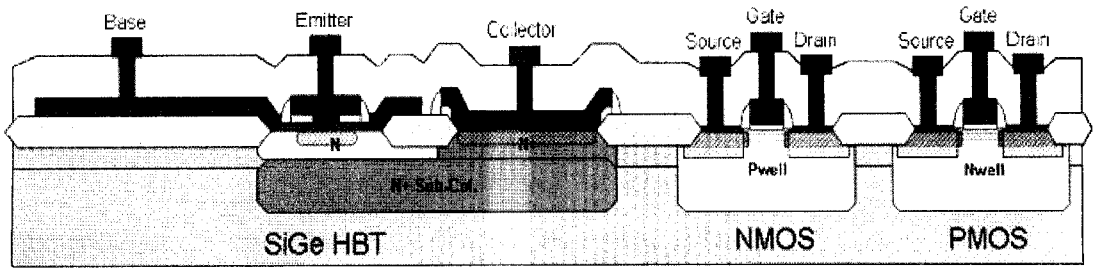

Fig. 1. Cross section of SiGe BiCMOS.

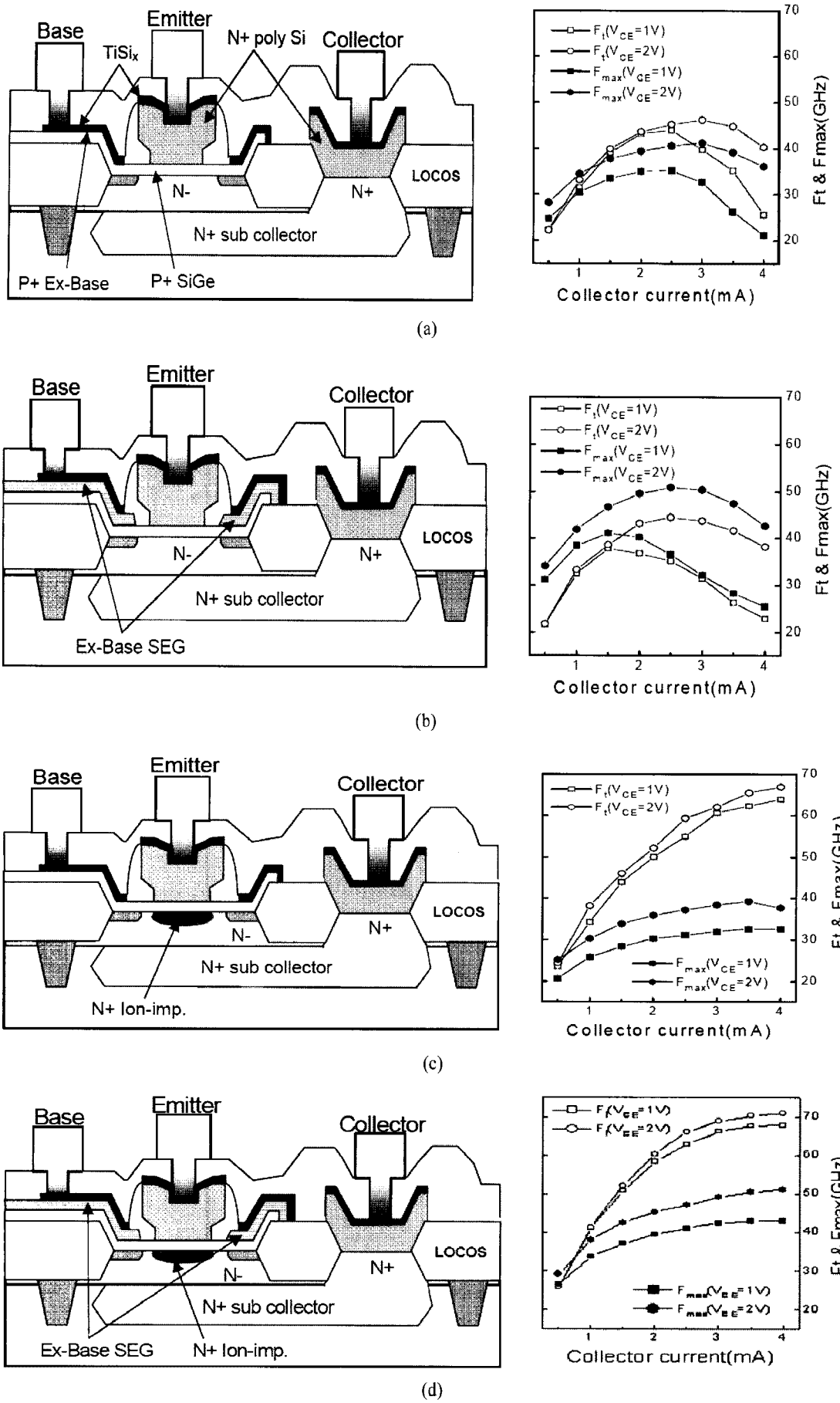

Fig. 3. Cross section and RF characteristics of (a) standard, (b) SEG, (c) SCI, (d) SEG & SCI.

high f_T and f_{max} is necessary. Therefore, the Structure-D is more effective to improve high frequency characteristics of SiGe HBT.

In addition, passive elements used for MMIC amplifier are Metal-Insulator-Metal (MIM) capacitor, parallel-branch spiral inductor, and resistors composed of metal, emitter poly-silicon, and base poly-silicon. The MIM capacitor consists of an underlying 1 μm Alumium metal layer, 75 nm thickness of isolator SiOxNy, and 2 μm Al metal with TiN over/under.

High-Q on-chip passives are required to meet the demanding requirements of RF circuits and to achieve the "system-on-a-chip" integration levels.

Generally, Q factor of the thin film inductor formed on silicon substrate can be improved by the method for reducing the resistance of the metal line itself and the parasitic capacitance. The highest percentage improvement in inductor peak Q is achieved by reducing the series resistive losses of the spiral metal lines. To decrease the spiral metallization sheet resistance, other inductors use more than five metals and over than 4 μm thick top metal. Inductors integrated in this work are parallel-branch spiral inductors with enhanced Q factor. Our top metal thickness is 2 μm. It has a little Q enhancement that the second metallization has more than 2 μm thickness. We used a SiGe BiCMOS process to fabricate these inductors. Fig. 4 shows the structures of the conventional spiral inductor and parallel-branch spiral inductor. Both are squared spiral inductors having silicon dioxide of 1 μm thick as an insulating layer.

Inductors integrated in this work are used Q factor enhanced parallel-branch spiral inductors. The inductor strip starts at the upper metal, branches off in the upper and lower metal strips with the same direction, and terminates at the opposite upper metal. Branching the inductor in parallel with the same direction, a mutual inductance is maximized and parasitic capacitances between lower metal and substrate are caused. Therefore, the Q factor of parallel-branch inductor is enhanced. Also, the frequency of peak quality factor f_{QMAX} is possible to be tuned, and the higher quality factor can be obtained.

The structure of presented parallel-branch inductor is different from fully stacked spiral inductor [5]. The inductor has 10 μm metal width and 2 μm metal space. Fig. 5, reports the f_{QMAX} of the parallel-branch inductor is

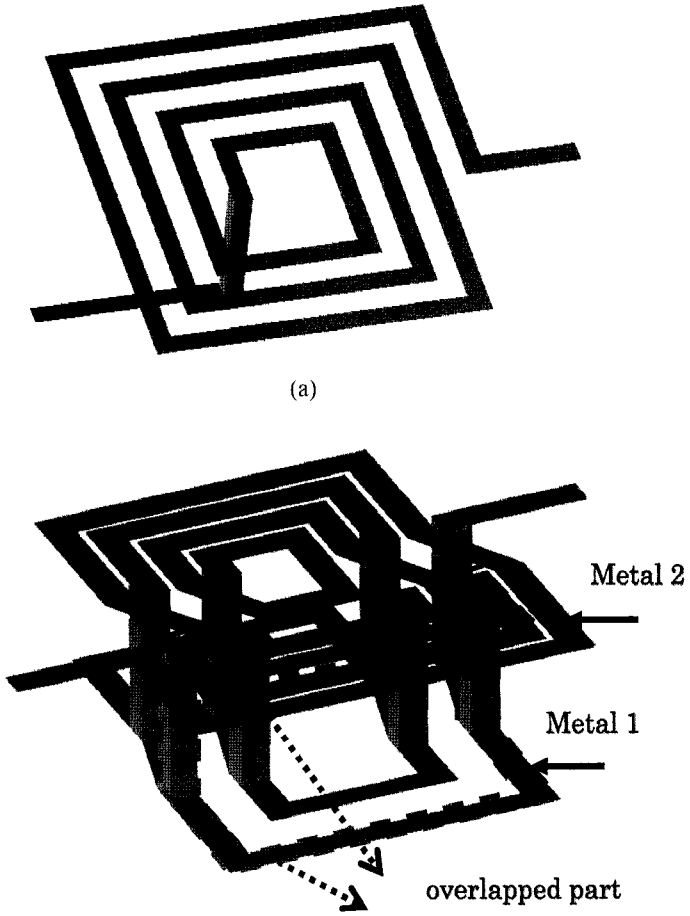

Fig. 4. Schematic diagrams of (a) the conventional and (b) the parallel-branch spiral inductor.

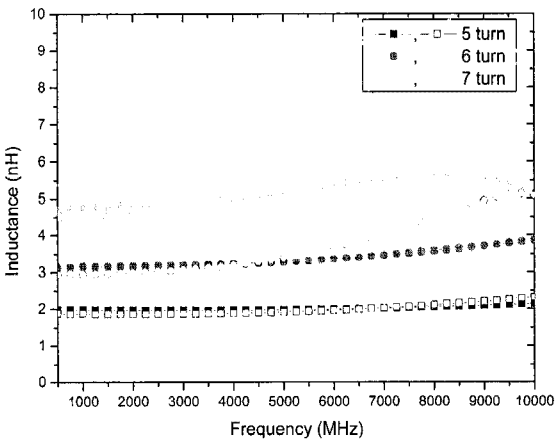

Fig. 5. Inductance variation of the conventional (solid) and the parallel branch (vacancy) inductors along the frequency.

lower than the conventional due to the parasitic capacitances by the lower metal. In Fig. 6, the quality factor is higher because the self and mutual inductance of the lower metal is added and metal resistance R_S is decreased

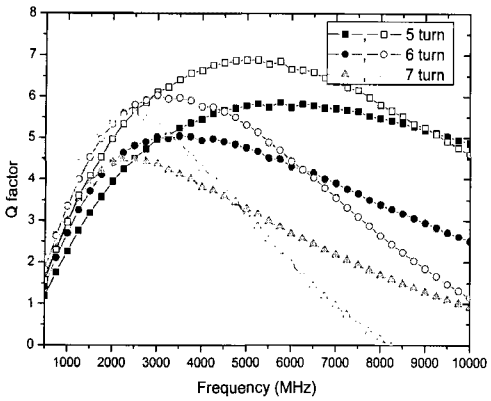

Fig. 6. Q factor versus frequency for the conventional (solid) and the parallel branch (vacancy) inductors.

by the parallel branch of the two metal strips. The presented parallel-branch inductor has 12% improved quality factor with the same area as the conventional inductor. This inductor is extracted parameters using a π-typed nine-element model [6]. The parasitic resistors and capacitors in this model have simple physically intuitive expressions.

III. Medium Power Amplifier

The MMIC amplifier is a single-ended two stage design with all matching components integrated on-chip. The LOCOS process has merits of the economical process but, is suffering RF performance limitation. Hence, the emitter areas of the driver stage and output stage transistors are optimized to provide the power gain and output power.

The first stage amplifier is designed with effective emitter area of 108 μm^2 transistor to improve the power gain. This first stage is matched to the input using a shunt inductance and the input DC-block capacitor and to the output using a inter-stage matching to the second amplifier. The second stage amplifier is matched to the output using two inductors and a capacitor. To improve the operating bandwidth of the amplifier, shunt-series peaked matching network has been used. Also, low pass output matching helps linearity of the amplifier to diminish the other harmonics. The bias currents are supplied using a resistor connected to the current-source to prevent thermal runaway in large signal operation.

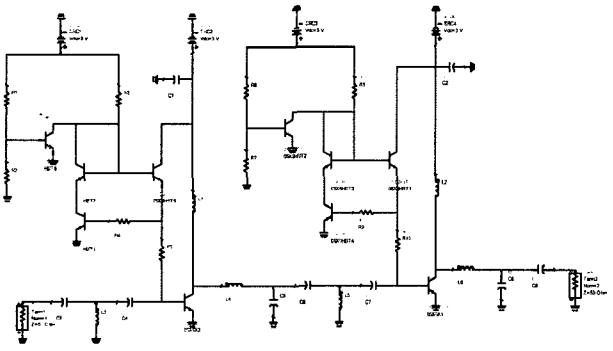

Fig. 7. Schematic of the fully integrated Medium Power Amplifier.

IV. Measurement Results

The medium power amplifier occupies 1.7 mm × 0.8 mm of die size, including the bias and probing pads. This demonstrates the size advantage of full integration. Fig. 8 shows the die photograph of the fully integrated medium power amplifier. Scattering Parameters of the amplifier in the 1.0 GHz - 6.0 GHz frequency range are shown in Fig. 9. From the data in Fig. 9, we find that the amplifier provides a small-signal power gain of 8.8 dB,

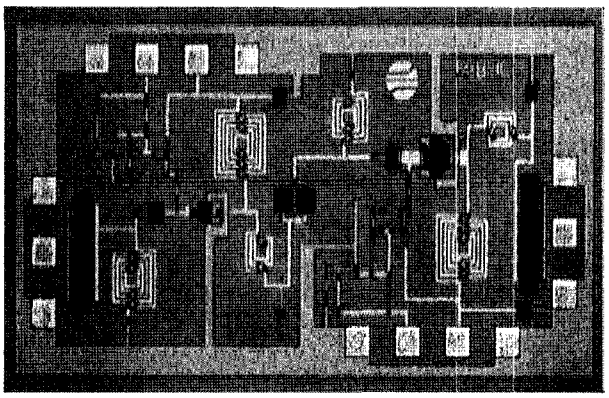

Fig. 8. Die photograph of the fully integrated Medium Power Amplifier.

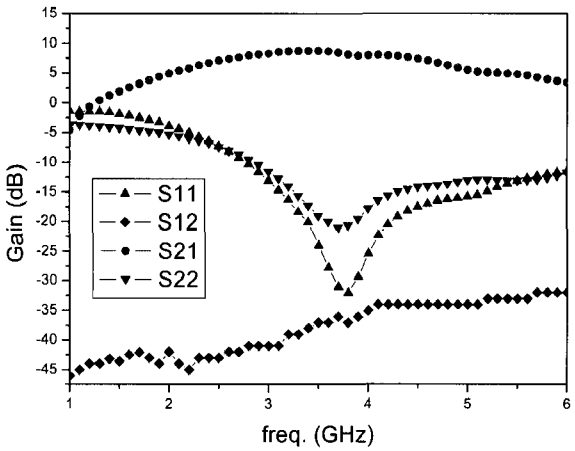

Fig. 9. Measured Small-Signal S-Parameters.

an isolation of 38 dB, and the input and output return losses are better than 15 dB at 3.4 GHz. The measured 3 dB bandwidth of the amplifier covers 2.2 GHz to 4.9 GHz. This wide bandwidth is a very good result for fully integrated medium power amplifier [7,8].

Fig. 10 presents the single-tone compression characteristics and the power gain of the amplifier at 3.4 GHz. From the data in this figure, we find that the 1 dB compressed output power and saturated output power of the amplifier into a 50 Ω load are 17.7 dBm and 19.3 dBm, respectively. The maximum PAE is 41%.

The two-tone compression characteristics of the medium power amplifier are shown in Fig. 11. Output IP3 of the amplifier has been measured at 3.4 GHz driving the input of the MPA with 10 MHz spaced two tones signals. From this figure we find that an output IP3 of 30 dBm. The fabricated medium power amplifier consumes a current of 30 mA for 3 V supply voltage.

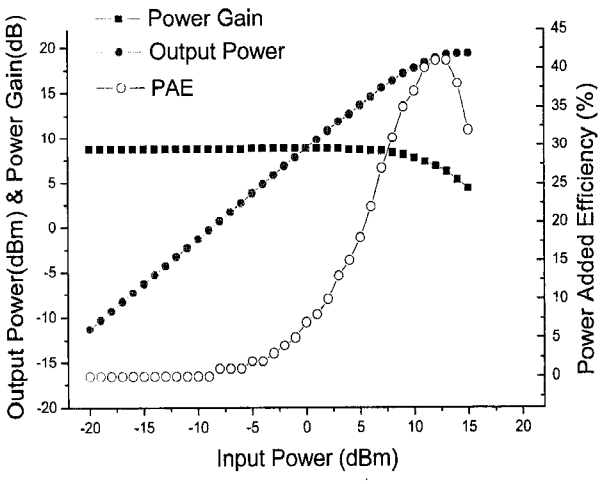

Fig. 10. Measured power gain, output power and PAE.

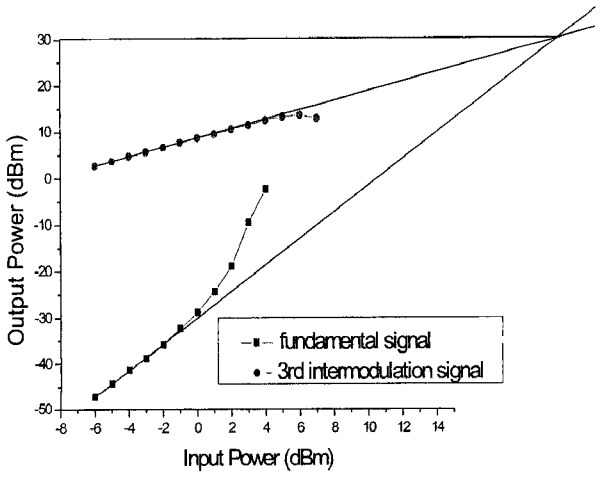

Fig. 11. Measured power intermodulation product.

V. CONCLUSIONS

We have demonstrated the effect of base and collector structures on small signal characteristics of SiGe HBTs and the fully integrated medium power amplifier for 2.2-4.9 GHz in a 0.8 μm SiGe BiCMOS technology. This single-ended 2-stage amplifier has no need for external matching circuits and has a broad operation range with adopting shunt-series peaked matching network. The measured results obtained from the fabricated medium power amplifier shows an 8.7 dB power gain, a P1dB of 17.7 dBm at 3.4 GHz with a 2.7 GHz bandwidth. This implies that a fully integrated medium power amplifier enables the realization of a single-chip transceiver for broadband wireless applications.

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