Design of a Latchup-Free ESD Power Clamp for Smart Power ICs

Jae-Young Park, Dong-Jun Kim, and Sang-Gyu Park

Abstract—**A latchup-free design based on the lateral diffused MOS (LDMOS) adopting the "Darlington" approaches was designed. The use of Darlington configuration as the trigger circuit results in the reduction of the size of the circuit when compared to the conventional inverter driven RC-triggered MOSFET ESD power clamp circuits. The proposed clamp was fabricated using a 0.35 μm 60V BCD (Bipolar CMOS DMOS) process and the performance of the proposed clamp was successfully verified by TLP (Transmission Line Pulsing) measurements.**

Index Terms—**Electrostatic discharge (ESD), darlington, power clamp, latchup, the lateral diffused MOS**

I. INTRODUCTION

ELECTROSTATIC DISCHARGE (ESD) protection has become an important task in the pursuit of the increased reliability of semiconductor ICs [1-4]. Furthermore, while the required ESD protection level is HBM 2 kV in most cases, in the Smart Power IC market the customer requirements are more demanding because Smart Power ICs are used in harsher environment than general logic IC.

In smart power technology, high-voltage MOSFETs have been used as on-chip ESD protection devices. Among them, the lateral diffused MOS (LDMOS) and the drain extended MOS (DEMOS) have been widely used as common ESD protection device because it can function both as output driver and as ESD protection device simultaneously without process modification.

There have been reports focused on analyzing and improving ESD robustness of the high-voltage MOSFETs [1-4]. However, these devices have very low snapback holding voltages, which can leads to latchup or latchup-like failures [5,6]. Because of this concern, they were seldom used in power clamp circuits.

In this paper, we propose a latchup-free power supply clamp design which uses a LDMOS in "Darlington" structure. The proposed power clamps were fabricated using a 60 V, 0.35 μm BCD process and the performance of the clamp was verified by TLP (Transmission Line Pulsing) tests.

II. LATCHUP OR LATCHUP-LIKE FAILURE IN ESD POWER CLAMP

When high voltage MOSFETs such as LDMOS (lateral double diffused MOS) are used in ESD protection clamps, they are used in "gate-grounded (gg)" configuration. However, as stated in the Introduction, these ggLDMOSs have very low snapback holding voltages. Fig. 1 shows the TLP-measured I-V characteristic of a ggLDMOS. In the TLP measurements, pulses having 100 ns duration and 10 ns rise/fall time were used. Fig. 1 shows that the ggLDMOS snaps back to only 9 V after the triggering. This strong snapback characteristic of the LDMOS is related to the turn-on behavior of the parasitic bipolar transistor and the occurrence of the Kirk effect (base push-out effect) [5,6].

When a ggLDMOS is used as I/O clamps, a low holding voltage is helpful to sustain a much higher ESD current because it leads to the smaller power dissipation. However, when these are used in power clamps, a low holding voltage poses a threat. The power clamps may

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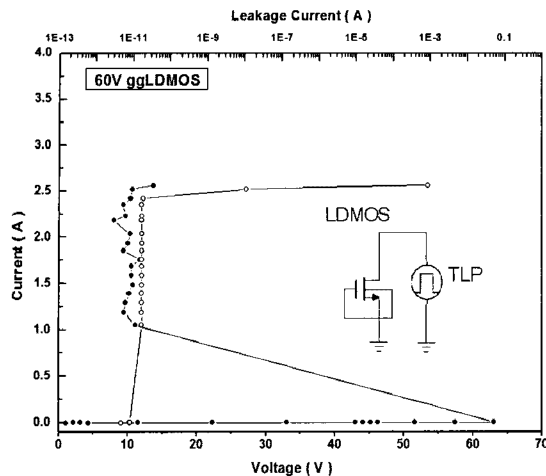

Fig. 1. TLP measured I-V characteristics of ggLDMOS fabricated in a 0.35 μm 60 V BCD process.

be triggered on by noise transients or by a glitch on the power lines during normal circuit operations. If the holding voltage of ESD power clamp devices is smaller than the power supply voltage, the power clamp may not be turned off after being accidentally turned on. This may cause very serious "latchup" or "latchup-like" failures and may lead to IC malfunction or even destruction [7].

This latchup related danger can be avoided if the power supply clamp is designed in such a way that the devices in the clamp do not enter the snapback region. No-snapback LDMOSs are one of the ways to achieve this and active research is going on in this area [8]. However, the design of a new such device usually involves process modification, which is very expensive. Therefore, in this work, we developed a circuit-level solution in which the device in the power clamp does not enter snap-back region.

III. DARLINGTON SCHEME

1. Principle of Operation

We propose the use of "Darlington scheme" to overcome the latchup or latchup-like issues in the design of power clamps for Smart Power ICs. Darlington scheme is an enhanced RC-triggered MOSFET ESD power clamp. Therefore, we briefly review the basic mechanism of RC-triggered MOSFET ESD power clamps first, and then we move on to the explanation of the proposed power clamp.

Fig. 2 shows a schematic of conventional RC-triggered MOSFET ESD power clamps. It consists of three elements: a) RC-frequency discrimination circuit, b) inverter drives circuit, and c) big MOSFET clamp [9]. Under an ESD transient event, the RC-frequency discrimination circuit detects a short ESD pulse, and drives the gate of MOSFET into the active turn-on mode, forming a low-impedance discharge path to shunt ESD current. Because of the raised gate voltage, the MOSFET operates below the triggering and does not enter into the snapback region. Therefore, it can reduce the latchup or latchup like dangers.

The draw-back of the RC-triggered power clamps is the large area requirement. In the RC-triggered MOSFET clamps, ESD current flows only through the channel region of the MOSFET because of the absence of the parasitic bipolar action associated with the snapback. Therefore, a very large MOSFET is required. Furthermore, the RC-frequency discrimination circuit and the inverter drive circuit occupy additional considerable silicon area.

To alleviate this area budgeting problem, we propose the Darlington scheme in Smart Power ICs. By using Darlington configuration as the drive circuit, the silicon area of the discrimination/drive circuit of the power clamp could be reduced by a factor of two when compared to that of the conventional RC-triggered circuits.

Fig. 3 shows the schematic of the proposed ESD power clamp circuit using the Darlington scheme. It consists of three parts, similar to the simple RC-triggered power clamp. However, the inverter drive circuit in the conventional circuit was replaced by a small LDMOS (M2) and a resistor. In the event of an ESD, M2 is turned on from the gate coupling effect, and a current flows through the resistor R1. This current raises the potential

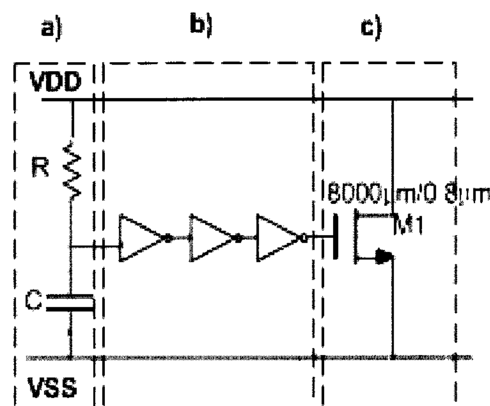

Fig. 2. Schematic of the conventional RC-triggered MOSFET ESD power clamps. (It consists of a) RC-frequency discrimination circuit, b) inverter drive circuit, c) MOSFET big clamp.)

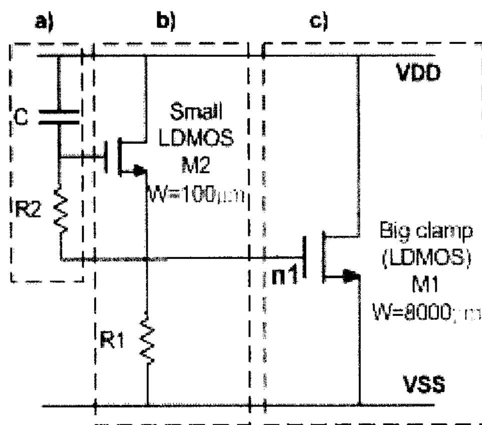

Fig. 3. Schematic of the proposed ESD power clamp circuit using Darlington scheme. (R1=R2=100kΩ, C=10pF. It consists of a) RC-frequency discrimination circuit, b) drive circuit, c) big LDMOS clamp.)

at node "n1" turning on the big LDMOS (M1). Because most of the ESD current flows through M1, M2 does not need to be large. Therefore the inverter stages like the one in Fig. 2 are not necessary between the RC network and M2. Therefore, the triggering section of the proposed circuit can be made much smaller than that of the conventional circuit.

The Darlington configuration for high voltage ESD protection circuit was originally reported by Sponton et al [10]. In Ref. [10], the parasitic capacitance between gate and drain was used as the coupling element which turns on the device upon the ESD event. However, the value of this parasitic capacitance depends on the device size and the supply voltage. Therefore, RC time constant cannot be controlled precisely independent of the ESD level requirement. Note that the device size is primarily determined by the level of ESD protection requirement. The control of the RC time constant is very important for the proper operation of the power clamp. If the constant is too large, a clamp reacts to ESD events too slowly and if it is too small the clamp can be mis-triggered even during a fast power-up. Therefore, rather than relying on the parasitic capacitance, we used a capacitor between the gate and drain so that the variation of the parasitic capacitance does not alter the total capacitance signifycantly.

2. Design and Measurement Results

The circuit of Fig. 3 has been designed using a 0.35 μm 60 V BCD Process. The widths of M1 and M2 were 8000 μm and 100 μm, respectively. The resistance R_1= R_2=100 kΩ were implemented by poly-silicon resistors and the capacitance C was implemented by a stacked (P1/M1/M2/M3) capacitor. Two values of C were used. C=10 pF corresponds to the R_2C time constant of 1 μs and C=2 pF to that of 0.2 μs.

To be effective as an ESD protection circuit, the power clamp should be turned on during an ESD event but should remain in off-state during normal circuit operation. To verify this, SPICE simulations for the triggering action have been performed. Voltage pulses with a pulse width of 100 ns and a rise time of 1ns was used to simulate the rising edge of an HBM ESD voltage. Fig. 4 shows the simulation results for R_2C=1 μs where a pulse of amplitude of 68 V is applied between VDD and VSS. It was observed that the gate voltage of M1, V(n1), rose rapidly to a level sufficient enough to turn on M1 then stayed at that level for the duration of the ESD pulse. Similar results were obtained with R_2C=0.2 μs.

To verify that the proposed clamp is kept off under normal conditions, a "VDD power-on condition" has also been simulated. A voltage ramp with a pulse height of 60 V and a rise time of 2 ms is used to simulate the rising edge of the normal VDD power-on voltage waveform. The rise time of VDD power-on transition is generally in the range of several milliseconds (ms). Fig. 5 shows that the proposed ESD power clamp is not turned-on under normal operation because V(n1) stays very close to 0 V at all time.

The performance of the designed power clamps were verified by TLP measurements of the fabricated clamps. Fig. 6 shows the TLP measured I-V characteristics. We can observe that the second breakdown current (I_{t2}) of this clamp circuit is about 4 A. Fig. 6 was obtained from

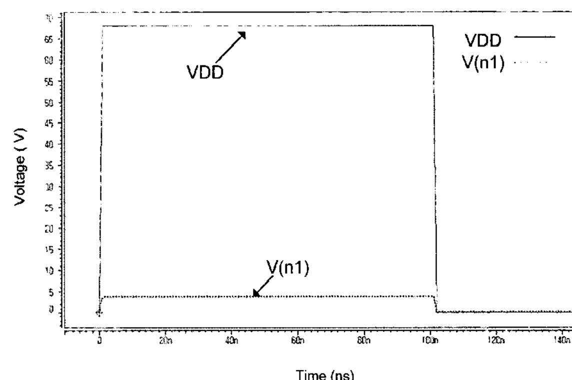

Fig. 4. The HSPICE simulated voltage waveforms for Darlington scheme ESD clamp circuit under the ESD stress condition (rise time = 1 ns, pulse width=100 ns).

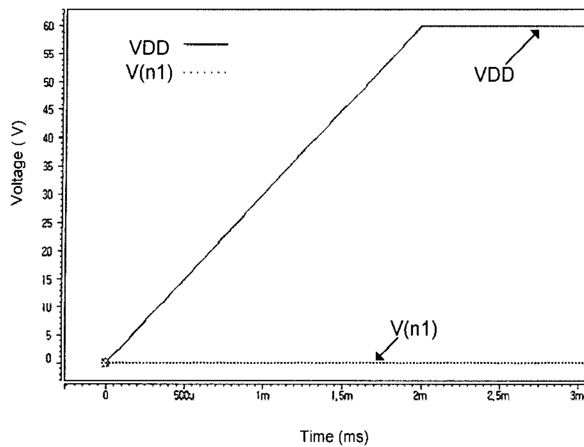

Fig. 5. The HSPICE simulated voltage waveform for normal VDD power-on condition. (rise time = 2 ms)

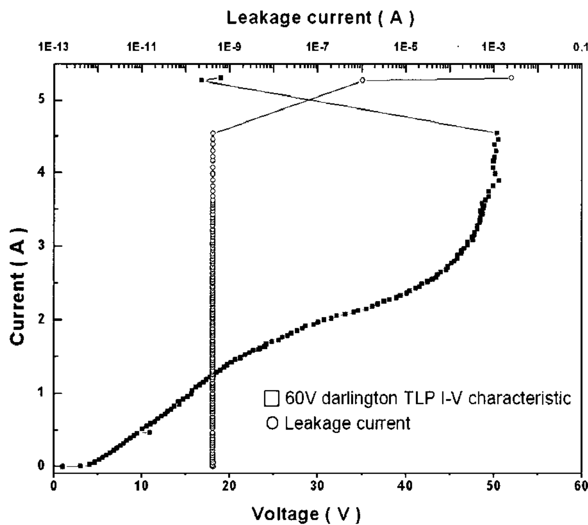

Fig. 6. TLP I-V characteristic and leakage evolution in Darlington scheme ESD power clamp.

a device of R_2C=1 μs but devices of R_2C=0.2 μs also produced similar results. The relation between the HBM blocking level and the second breakdown voltage can be expressed by [11]

$$V_{HBM} \cong 1.5k\Omega \times I_{t2}, \quad (1)$$

where 1.5 kΩ represents the HBM source resistance. From Eq. (1), we can conclude that the designed clamp can be used for ESD protection of HBM 6000 V level.

The drive circuit of the proposed clamp occupies area occupies 660 μm^2 while that of the conventional clamp does 1400 μm^2. This represents more 50% reduction of the area. The area of the big clamp was identical in both cases. In all, the proposed clamp occupies 10% smaller area than the conventional one. A micrograph of the proposed ESD protection circuit is shown in Fig. 7.

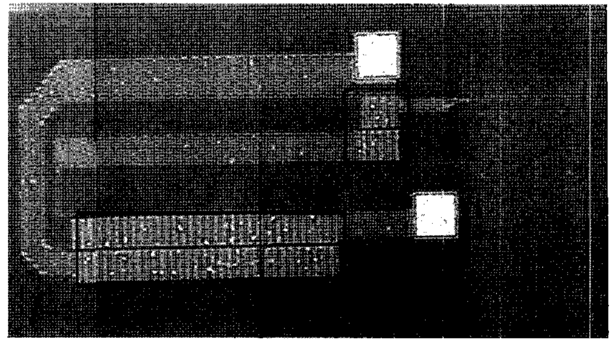

Fig. 7. The micrograph of the proposed ESD protection circuit.

IV. CONCLUSIONS

The holding voltage of the high-voltage MOSFETs in snapback condition is much smaller than the power supply voltage. This characteristic excludes the use of the devices in the ESD power clamp in the snapback mode due to the possibility of the latchup related failures. To overcome this problem, a latchup-free design using a LDMOS based on a "Darlington" approaches was proposed. The layout area of the proposed clamp was reduced by 10% when compared to the conventional RC-triggered ESD power clamp. From the measurements on the devices fabricated using a 0.35 μm BCD Process (60 V), it was observed that the proposed ESD power clamp can safely operate in Smart Power ICs.

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