An Analytical Modeling of Threshold Voltage and Subthreshold Swing on Dual Material Surrounding Gate Nanoscale MOSFETs for High Speed Wireless Communication

N. B. Balamurugan, K. Sankaranarayanan, P. Amutha, and M. Fathima John

Abstract—**A new two dimensional (2-D) analytical model for the Threshold Voltage on dual material surrounding gate (DMSG) MOSFETs is presented in this paper. The parabolic approximation technique is used to solve the 2-D Poisson equation with suitable boundary conditions. The simple and accurate analytical expression for the threshold voltage and subthreshold swing is derived. It is seen that short channel effects (SCEs) in this structure is suppressed because of the perceivable step in the surface potential which screens the drain potential. We demonstrate that the proposed model exhibits significantly reduced SCEs, thus make it a more reliable device configuration for high speed wireless communication than the conventional single material surrounding gate (SMSG) MOSFETs.**

Index Terms—**DMSG MOSFET, SCEs, threshold voltage, subthreshold swing, 2-D model**

I. INTRODUCTION

The Primary challenge for scaling complementary metal oxide semiconductor (CMOS) devices is the increased functionality per unit cost and the improved performance of devices. As device dimensions shrink to nanometer regime, Short-channel effects (SCEs) [1] impose a physical limit on their performance. In recent years, a number of non-classical MOSFETs have been proposed as the device structures to sustain the growth of the CMOS technology into nanoscale. These device structures include double gate (DG) MOSFETs, dual material gate (DMG) MOSFETs, surrounding gate (SG) MOSFETs, and dual material surrounding gate (DMSG) MOSFETs.

The difficulty with the DG MOSFETs is the control of the threshold voltage that is hardly dependent on the doping concentration and strongly affected by the thicknesses of the silicon film [2]. On other hand, DMG MOSFET provides simultaneous increase in transconductance and suppression of SCEs [3]. Its drivability and transconductance are not as good as that of the DG structure. The latest development in SG MOSFETs offers control of SCEs, improvement in the subthreshold slope, and packing densities [4]. Despite its advantages, SG MOSFETs suffer from considerable short channel behavior in the sub-100 nm regime. To overcome this, Kumar et al [5] have proposed an accurate model for the DMSG MOSFETs, where the effects of Short channel has not been dealt completely. The proposed structure exhibits the desired features of both the DMG and SG structures. This paper proposes a simple analytical model for characterizing the DIBL and threshold voltage of the DMSG MOSFETs that describe the behavior of SCEs completely with various controlling parameters. With this model, the simple and accurate analytical expression for the threshold voltage and subthreshold swing is derived. To demonstrate the efficacy of the proposed model, we

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compare the model results with the Single material Surrounding gate (SMSG) MOSFETs. This model thus provides an efficient tool for design and characterization of the novel DMSG MOSFETs.

II. Theoretical Model

A schematic view of the DMSG nanoscale MOSFET is shown in fig. 1 along with spherical coordinate system consists of a radial direction r, a vertical direction z, and an angular component θ in the plane of the radial direction. The Gate consists of two materials M_1 & M_2 with gate lengths L_1 and L_2 and two different work functions V_{b1} and V_{b2}.The relation among the surface potential, charge, and electric field are derived by solving the Poisson's equation in the silicon pillar. The influence of the charge carrier and the fixed charges on the electrostatics of the channel is assumed to be neglected. The potential distribution ϕ (r, z) in fully-depleted DMSG MOSFETs is

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi(r,z)}{\partial r}\right)+\frac{\partial^2\phi(r,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}} \quad (1)$$

Where $\phi(r,z)$ is electrostatic potential in the silicon

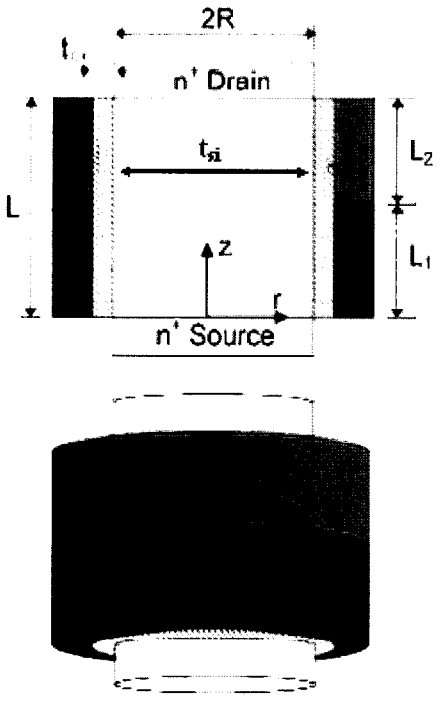

Fig. 1. Schematic view of dual material surrounding gate MOSFETs.

film, q is the electron charge, N_a is the silicon film doping concentration, and ε_{si} is the permittivity of the silicon film. Using the similar manner to Young's [6], we assume that the parabolic potential profile in the vertical direction of the channel is given by

$$\phi(r,z)=s_1(z)+s_2(z)r+s_3(z)r^2 \quad (2)$$

Where $s_1(z), s_2(z)$ and $s_3(z)$ are the functions of z. The boundary conditions required for the solution of (1) are given in the following:

(a) The surface potential $\phi_s(z)$ is a function of z only.

$$\phi(R,z)=s_1(z)=\phi_s(z) \quad (3)$$

(b) The electric field in the center of the silicon pillar is zero by symmetry.

$$\frac{\partial}{\partial r}\phi(r,z)\Big|_{r=0}=0 \quad (4)$$

(c) The electric field at the silicon /oxide interface is continuous.

$$\frac{\partial\phi(r,z)}{\partial r}\Big|_{r=R}=\frac{\varepsilon_{ox}}{\varepsilon_{si}R}\left(\frac{V_{GS}-\phi_s(z)-V_{FB}}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right) \quad (5)$$

(d) The potential at the source end is

$$\phi(0,0)=\phi_s(0)=V_{bi} \quad (6)$$

(e) The potential at the drain end is

$$\phi(L,0)=\phi_s(L)=V_{bi}+V_{ds} \quad (7)$$

Where V_{FB} is flat –band voltage, $2R$ is the diameter of the silicon pillar, t_{ox} is the silicon –oxide thickness, ε_{ox} is the permittivity of the oxide layer, t_{si} is the thickness of the silicon film, V_{GS} is the gate-source voltage, V_{bi} is the built in potential between the source and the body, V_{ds} is the drain-source voltage, and L is the channel length.

The constants $s_1(z)$, $s_2(z)$ and $s_3(z)$in (2) can be found from the boundary conditions (3) to (5), we get the value of $s_2(z)$ and $s_3(z)$ as

$$s_2(z) = 0 \tag{8}$$

$$s_3(z) = \frac{\varepsilon_{ox}}{2R^2\varepsilon_{si}} \frac{V_{GS} - V_{FB} - \phi_s(z)}{\ln\left(1+\frac{t_{ox}}{R}\right)} \tag{9}$$

Since $s_1(z), s_2(2)$ and $s_3(z)$ are known, the 2D potential distribution $\phi(r,z)$ in (2) is expressed as

$$\phi(r,z) = \phi_s(z) + r^2\left(\frac{\varepsilon_{ox}}{2R^2\varepsilon_{si}} \frac{V_{GS} - V_{FB} - \phi_s(z)}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right) \tag{10}$$

Taking the partial derivatives of (10) and using the boundary conditions, we obtain

$$\frac{\partial^2\phi_S(z)}{\partial z^2} - P^2\phi_S(z) = Q \tag{11}$$

Where

$$P^2 = \frac{2\varepsilon_{ox}}{R^2\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)} \tag{12}$$

$$Q = \frac{qN_a}{\varepsilon_{si}} - P^2(V_{GS} - V_{FB}) \tag{13}$$

In a conventional SGT MOSFET, the gate is made of only one material, but in the DM-SGT structure, we have two gates with different work functions and doping density under them.

Applying (11) to this device, we have

$$\frac{\partial^2\phi_{S1}(z)}{\partial z^2} - P^2\phi_{S1}(z) = Q_1 \quad \text{for} \quad 0 \le z \le L_1 \tag{14}$$

$$\frac{\partial^2\phi_{S2}(z)}{\partial z^2} - P^2\phi_{S2}(z) = Q_2 \quad \text{for} \quad L_1 \le z \le L_1 + L_2 \tag{15}$$

Where $\phi_{s1}(z)$ and $\phi_{s2}(z)$ are the surface potentials under the bottom and top gates, respectively. Also Q parameter corresponds to the respective regions. By solving (14) and (15), we obtain the solution for the surface potential under M_1 & M_2 as

$$\phi_{S1}(z) = A\exp(Pz) + B\exp(-Pz) - S_1 \quad \text{for} \quad 0 \le z \le L_1 \ \text{under} \ M_1 \tag{16}$$

$$\phi_{S2}(z) = C\exp(P(z - L_1)) + D\exp(-P(z - L_2)) - S_2 \quad \text{for} \quad L_1 \le z \le L_1 + L_2 \ \text{under} \ M_2 \tag{17}$$

$$\text{Where,} \ S_1 = \frac{Q_1}{P^2}, \ S_2 = \frac{Q_2}{P^2} \tag{18}$$

Using boundary conditions (6) & (7), we obtain A, B, C, D as

$$A = \frac{G\cosh(PL_2) + E - F\exp(-PL)}{2\sinh PL} \tag{19}$$

$$B = \frac{G\cosh(PL_2) + F\exp(-PL) - E}{2\sinh PL} \tag{20}$$

$$C = \frac{G}{2} + 2A\exp(PL_1) \tag{21}$$

$$D = \frac{G}{2} + 2B\exp(PL) \tag{22}$$

$$G = S_1 - S_2 \tag{23}$$

$$E = V_{bi} + V_{ds} + S_2 \tag{24}$$

$$F = V_{bi} + S_2 \tag{25}$$

The threshold voltage of a DMSG MOSFET may be defined as the gate voltage capably accomplishes the minimum surface potential to sustain the channel region. Since the subthreshold leakage current occurs at the position of the minimum surface potential in the case of short channel devices, The threshold voltage is defined as the value of V_{GS} at which the minimum surface potential $\phi_{S1,\min}$ equals $2\phi_F$. Hence, the threshold voltage is then obtained as

$$V_{th} = \frac{e + \sqrt{e^2 - 4a(c-d)}}{2a} \tag{26}$$

Where the constant coefficients are given below

$$a = \cos^2 hPL \tag{27}$$

$$b = 2V_{bi} + 3V_{ds} - 4\phi_F \sin^2 hPL \tag{28}$$

$$c = 4\phi_F^2 \sin^2 hPL - (V_{bi} + 3V_{bi}V_{ds} + V_{ds}^2) \tag{29}$$

$$d = \frac{aq^2 N_A^2}{P^4 \varepsilon_{si}} + \frac{2V_{FB} qN_A}{P^2 \varepsilon_{si}} + aV_{FB}^2 + \frac{bqN_A}{P^2 \varepsilon_{si}} + \frac{bqN_A V_{FB}}{P^2 \varepsilon_{si}} \tag{30}$$

$$e = \frac{2aqN_A}{P^2 \varepsilon_{si}} + 2V_{FB}a + b \tag{31}$$

An important parameter for a MOSFET is the subthreshold slope, which is defined as the change in gate voltage required to reduce the subthreshold current by one decade. The minimum value of the subthreshold swing (S) is then extracted from the inverse subthreshold slope versus gate voltage curve:

$$s = \ln 10 \left\{ \frac{d \ln I_D}{dV_{GS}} \right\}^{-1} \tag{32}$$

$$I_D = q.n_i.W\mu \frac{\int_0^{V_{ds}} e^{-\phi_f / V_T} d\phi_f}{\int_0^L \frac{dr}{\int_{-t_0}^{t_0} e^{\phi(r,z)/V_T} dz}} \tag{33}$$

The integral in (33) can be approximated by its value at $0.5t_0$. After mathematical manipulations we obtain closed form expression for the subthreshold swing.

$$s = \frac{\ln 10 \, V_T}{\frac{C_f.R}{2.\varepsilon_{si}} \left[\frac{L^2}{R^2} - 1 \right]} \tag{34}$$

Where, $$C_f = \frac{\varepsilon_{ox}}{R \ln\left(1 + \frac{t_{ox}}{R}\right)} \tag{35}$$

III. Results and Discussions

Fig. 2 shows the calculated values of the threshold voltage along the channel for different drain source voltages. From the figure, it may be observed that threshold voltages of the device may be shifted to lower value if V_{ds} changed from $V_{ds} = 0$ to $V_{ds} >= 0$. As shown in the figure, the threshold voltage is increased by increasing drain source voltages. The comparison of subthreshold swing values for DG, SG and DMSG MOSFETs is shown in Fig. 3. It can be observed that DMSG offers subthreshold swing values of less than 65 mV for gate length of about 50 nm. This supports scaling of the device further by making any compromise in the performance of the device. It can be optimized to the extent by choosing the required values for oxide thickness and silicon thickness.

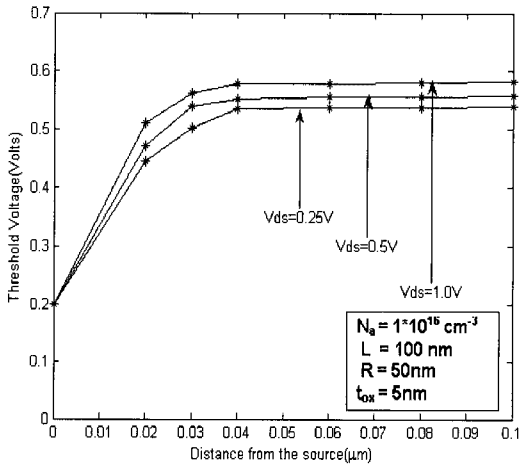

Fig. 2. Threshold voltage Vs Distance from the source of a DMSG MOSFET for different drain biases.

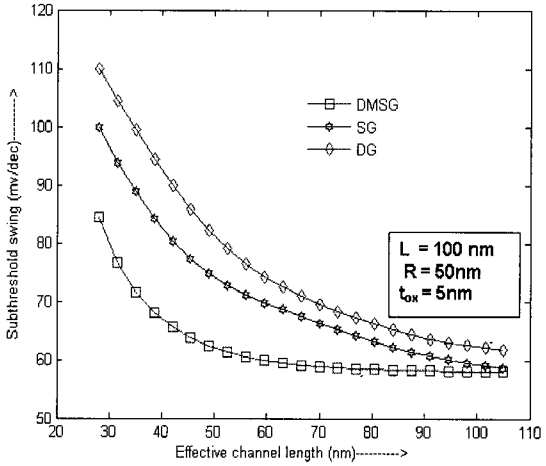

Fig. 3. Subthreshold swing values Vs Channel length for DG, SG, DMSG MOSFETs.

IV. CONCLUSIONS

We derived a new two dimensional (2-D) analytical model for the Threshold Voltage and subthreshold swing for the dual material surrounding gate (DMSG) MOSFETs. The results clearly demonstrate the excellent immunity against SCE offered by the DMSG structure with V_{th} roll-up by decreasing channel length visible down to 0.1 μm. All these features should make the proposed DMSG MOSFET a prime candidate for high speed wireless communication.

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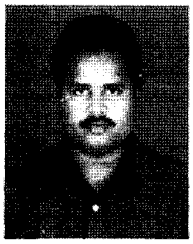

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