Surpassing Tradeoffs by Separation: Examples in Transmission Line Resonators, Phase-Locked Loops, and Analog-to-Digital Converters

Nan Sun, William F. Andress, Kyoungho Woo, and Donhee Ham

Abstract—We review three examples (an on-chip transmission line resonator [1], a phase-locked loop [2], and an analog-to-digital converter [3]) of design tradeoffs which can in fact be circumvented; the key in each case is that the parameters that seem to trade off with each other are actually separated in time or space. This paper is an attempt to present these designs in such a way that this common approach can hopefully be applied to other circuits. We note reader that this paper is not a new contribution, but a review in which we highlight the common theme from our published works [1-3]. We published a similar paper [4], which, however, used only two examples from [1] and [2]. With the newly added content from [3] in the list of our examples, the present paper offers an expanded scope.

Index Terms—Tradeoffs, transmission lines, oscillators, phase locked loops, frequency synthesizers, analog-to-digital converters, pipelined analog-to-digital converters, calibration, discrete-time filter, integrated circuits

I. INTRODUCTION

Dealing with tradeoffs is a challenge engineers must face in almost every design. A tradeoff occurs whenever one favorable parameter or performance measure must be sacrificed in favor of another. A classic example is the tradeoff between gain and bandwidth in amplifiers,

usually constrained by a constant gain-bandwidth product. In the face of such a tradeoff one increases gain at the expense of bandwidth or vice versa until hopefully both values are acceptable. In this way tradeoffs often become the ultimate limitation upon the design.

However, sometimes it is easy to perceive a tradeoff where it can in fact be nullified: two parameters that seem to trade off with each other may actually be independent or separable with clever design.

To illustrate this point let us consider Crowley's widely-used phase-locked loop (PLL) [5], which turns out to be an example precisely of this nature. In this case the apparent tradeoff is that between lock time and spectral purity: on one hand, the loop bandwidth must be maximized to minimize lock time. On the other hand, too wide a bandwidth brings more spurs and component noise (except VCO noise) into the PLL's dynamics, corrupting its output spectrum. Due to their opposite dependencies on loop bandwidth, lock time and spectral purity appear to be conflicting traits. But these two traits actually have their significance in two separate phases of the PLL operation and are therefore separated in time: spectral purity matters only during steady-state and lock time matters only during transient. Recognizing the separability of these two traits in time, Crowley employs a variable bandwidth scheme: a wider bandwidth is used during transient to accelerate phase locking, but once the PLL enters a phase-locked steady state, the bandwidth is shifted to a smaller value to attain an optimal spectrum.

Three of our own recently published designs [1-3] happen to follow the same design paradigm. Our PLL work by Woo et al [2] recognizes a separability in time between another set of PLL design parameters in an

apparent tradeoff and exploits the separability in const-ructing a fastlock PLL. Our work by Andress *et al* [1] deals with a tradeoff between series and shunt losses in a microwave on-chip transmission line. While it is a com-mon notion that reducing one type of loss without in-creasing the other is difficult, in [1] we show that if the amplitudes of waves hosted by the line are made position-dependent, as in a standing wave, the series and shunt losses can be separated in space and a high-Q transmit-ssion line can be built. Our work by Sun *et al* [3] tackles a tradeoff associated with correlation-based digital back-ground calibration in pipelined analog-to-digital conver-ters (ADCs). By realizing a separability in time between convergence accuracy and convergence time of digital-background calibration, we apply a bandwidth switching scheme just like Crowley's to relax the tradeoff.

Though Crowley's work and our own three works are all based upon entirely different designs, we found in retrospect that they share the same spirit of circumvent-ting certain tradeoffs through separation in time or space. Our objective in this paper is to illustrate this common observation, by reviewing our three works [1-3] under this unified theme. Thus rather than introducing a new contribution we wish to explicitly articulate and share the insight common to these prior works, and we hope it can be related to other designs in the future. We will first discuss the work in [1] where the principle can be illustrated simply, and then move on to the work in [2] where the principle appears in a rather complicated fashion. We will subsequently describe the work in [3]: here although the principle is illustrated simply, we will first expound on the theoretical foundation we established, which ultimately led to the application of the principle.

II. EXAMPLE 1: WAVE-ADAPTIVE TAPERED TRANSMISSION LINE

In this section we consider an on-chip transmission line in silicon, and explore a tradeoff between two types of power dissipation in the line. The tradeoff can be circumvented by exploiting the spatial separation between the two losses whenever a standing wave is formed on the line. This work was originally published in [1].

For the on-chip transmission line, the focus will be specifically on a coplanar stripline (CPS) widely used for differential operation. It consists of two metals running
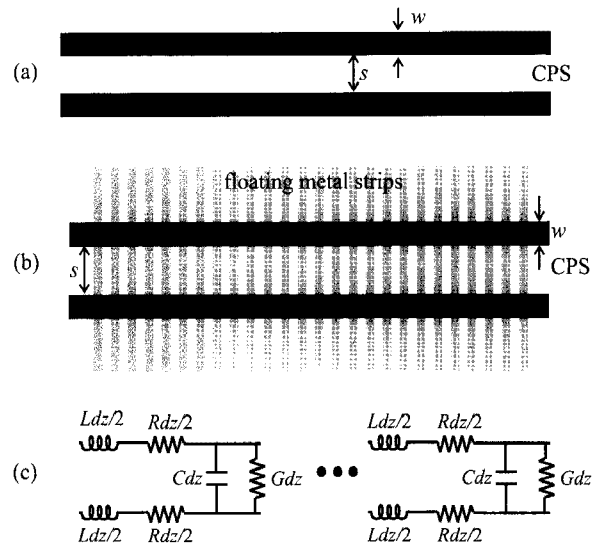

Fig. 1. (a) CPS above a silicon substrate (top view). (b) CPS with underlying metal strips above the substrate. (c) *LRCG* model.

in parallel. The CPS can directly face a silicon substrate underneath [Fig. 1(a)], or, floating metal strips periodically placed underneath the CPS [Fig. 1(b)] can shield fields from the lossy silicon substrate. In the latter case, the relatively large loss of the silicon substrate is replaced with the smaller loss of the floating metal strips.

1. Tradeoff between Series and Shunt Losses

The CPS structure can be electrically modeled using the familiar differential *LRCG* network [Fig. 1(c)], where L, C, R, and G are inductance, capacitance, series resis-tance, and shut conductance per unit length, respectively. R mainly accounts for loss *within* the CPS metals due to skin and proximity effects. The familiar skin effect is the tendency for *ac* current to become concentrated at the surface of a conductor at high frequencies, thereby reducing the effective area of current flow. The proximity effect refers to the phenomenon that when two *ac* currents flow in opposite directions, the effective area of current flow is further squeezed toward the proximate regions of the two conductors. G, on the other hand, reflects loss *outside* of the CPS metals, for instance, losses coming from the substrate in the CPS of Fig. 1(a) and losses coming largely from the underlying periodic metal strips of Fig. 1(b).

R couples to current waves as G couples to voltage waves to introduce respective series and shunt losses. Smaller R corresponds to less series loss; smaller G

corresponds to less shunt loss. Simultaneous minimization of R and G is desired in the design of the CPS by properly selecting its two design parameters, the metal width, w, and the separation, s, where w and s are with reference to Fig. 1. The simultaneous minimization, however, is difficult. Increasing w decreases R due to a reduced skin effect but increases G due to increased interaction between EM fields and lossy media outside the CPS metals (substrate or underlying metal strips). Likewise, increasing s mitigates proximity effects hence decreasing R, but this increases G again due to increased interaction between fields and lossy media outside the CPS metals. Clearly one cannot come up with a CPS structure where both R and G are simultaneously minimized. This is a widely recognized tradeoff between R and G, from which one might easily conclude that the series loss caused by R and the shunt loss caused by G cannot be simultaneously minimized.

2. Circumventing the Tradeoff via Line Tapering

A more careful inspection, however, reveals that such a conclusion is a hasty one. The series loss caused by R is also a function of the current wave amplitude, and the shunt loss caused by G is also a function of the voltage wave amplitude. If the line hosts a sinusoidal traveling wave where the voltage and current amplitudes are the same throughout the line, it is indeed true that the R-G tradeoff directly translates to the tradeoff between the series and shunt losses. However, if the CPS hosts a sinusoidal standing wave where the voltage and current amplitudes are position-dependent and moreover the voltage and current standing waveforms are offset from each other by a quarter wavelength in space, a completely different scenario emerges and the R-G tradeoff can be elegantly circumvented so as not to cause the tradeoff between the series and shunt losses, in order to minimize overall loss [1].

To see this, consider a CPS of length l terminated by an open on one end and a short on the other, as in Fig. 2. Reflections of waves at both ends and their superpositions lead to standing waves. In the resulting fundamental standing-wave mode, the CPS would span a quarter wavelength ($l=\lambda/4$), with the voltage maximum & current zero at the open end ($z=0$) and the current maximum & voltage zero at the short end ($z=l$): see Fig. 2. Since R couples to
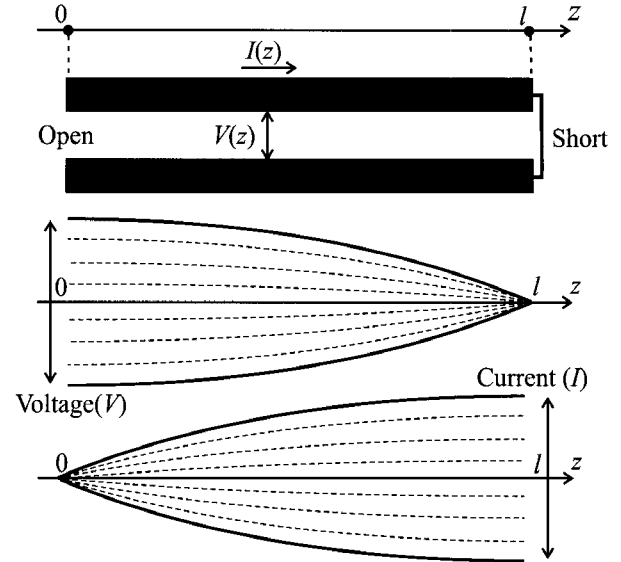

Fig. 2. A CPS with a short and an open termination at each end and the $\lambda/4$ voltage and current standing waves it hosts.

current waves, series losses are localized toward the short end ($z=l$). Likewise, since G couples to voltage waves, shunt losses are localized toward the open end ($z=0$). In other words, the series loss and shunt loss are rather separated in space. When the two types of dissipation do not overlap significantly in space, the R-G tradeoff is quite irrelevant. Near $z=0$, G may be minimized by choosing proper w and s to reduce loss while the unavoidable increase in R (due to the R-G tradeoff) is not detrimental because of the negligible current amplitude in this vicinity. Similarly toward $z=l$, R may be minimized to reduce loss while the inevitable increase in G is not harmful due to the locally negligible voltage. This continuous variation of R and G along z by varying w and s to minimize loss yields a tapered transmission line.

The CPS tapering while holding the characteristic impedance Z_0 constant throughout the line to prevent reflections can be done using a contour of characteristic impedance in w-s space obtained from EM simulations Fig. 3(a). As one simultaneously moves apart (increasing s) and widens (increasing w) the CPS following this contour, Z_0 remains constant while R decreases and G increases (R-G tradeoff). The $\lambda/4$ CPS can be tapered along this contour as shown in Fig. 3(b). The voltage maximum and current zero at $z=0$ yields minimum local loss with low G and high R. The current maximum and voltage minimum at $z=l$ yields minimum local loss with low R despite high G. In [1] we experimentally confirmed the benefit of this technique: a lower-loss (higher-Q) tapered
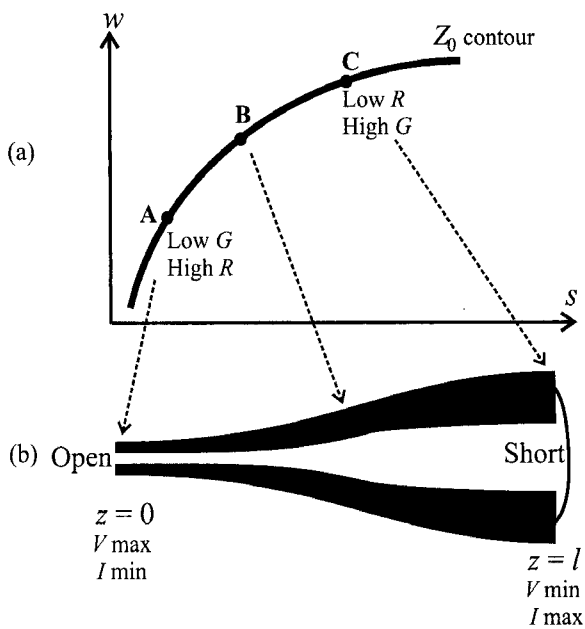
Fig. 3. (a) Z_0 contour in w-s space. (b) Tapered line.

Fig. 4. Hybrid PLL operation.

structure, when used as a resonator of a standing wave oscillator, lowers the oscillator's phase noise by up to 10 dB.

The separability between lock time and optimum spectrum in two distinct phases of the PLL operation lends itself to Crowley's technique of varying the PLL bandwidth in time. Analogously, the separability between the series and shunt losses in two distinct points of a transmission line hosting a standing wave lends itself to our technique of varying the line structure in space.

III. EXAMPLE 2: PLL FREQUENCY SYNTHESIZER COMBINING FRACTIONAL- & INTEGER-N MODES

Crowley's fast-lock variable-bandwidth PLL [5] has been used almost exclusively within a fixed frequency division mode, *i.e.*, the bandwidth switching has been executed while maintaining the same frequency division mode at either integer- or fractional-N. In [2], we generalized Crowley's scheme, introducing a single-loop fast-lock PLL frequency synthesizer that changes not only bandwidth but also frequency division mode between transient and steady states. More concretely, the PLL operates in a narrow-bandwidth, integer-N mode during steady state (phase lock), but in a wide-bandwidth, fractional-N mode (with no fractional spur reduction circuit such as phase interpolators or high-order $\Sigma\Delta$ modulators) during transient. See Fig. 4. This hybrid PLL frequency
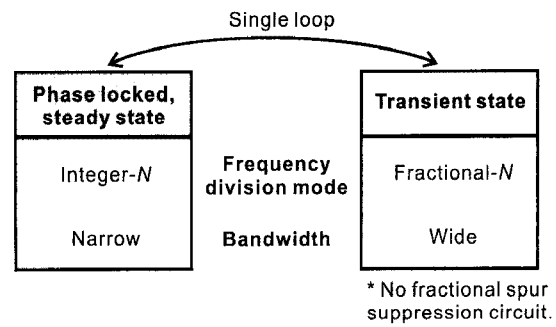
synthesizer is another example in which an apparent tradeoff is circumvented via separation in time, which we will elucidate in what follows.

1. Tradeoff & its Circumvention

Consider a scenario where an integer-N PLL frequency synthesizer is preferred to a fractional-N one, due to the design simplicity of the former. In the latter, phase interpolators or high-order $\Sigma\Delta$ modulators are needed to reduce fractional spurs. Since quantization noise of such fractional spur reduction circuits can corrupt the PLL spectrum via loop nonlinearities, significant design efforts are required to minimize loop nonlinearities in the fractional-N PLL. In contrast, integer-N PLLs are much simpler to design due to the absence of fractional spurs.

The design simplicity of integer-N PLLs, however, comes at the price of slow locking. To produce the same set of output frequencies in a given application, an integer-N PLL uses a lower reference frequency than a fractional-N PLL. The reference frequency is directly proportional to the maximum usable bandwidth in any PLL, and hence, the integer-N PLL cannot accommodate as large a bandwidth as the fractional-N PLL. The result is the slower speed of the integer-N PLL.

So an apparent tradeoff would be encountered in an attempt to achieve both the speed of the fractional-N PLL and design simplicity of the integer-N PLL. In [2] we recognized, however, that the two traits involved in the tradeoff, speed and fractional spurs (the latter is tied with the design complexity as mentioned), matter in two separate phases of the PLL operation, the exploitation of which led to the hybrid PLL. During transient, the speed is what matters and hence we use a fractional-N mode that can accommodate a larger bandwidth. During steady state, the PLL is shifted to integer-N since the continued

use of the fractional-N in the steady state would require the fractional-spur reduction circuit. The use of the fractional-N mode only during transient does not require such a fractional spur reduction circuit, for spurs matter only during steady state, and hence we do not implement any such fractional spur reduction circuit, leading to the design simplicity. In this way we came up with the hybrid PLL that opportunistically switches between the two frequency division modes of differing bandwidths to circumvent the apparent tradeoff, adopting each of their good behaviors while discarding their bad behaviors.

The hybrid PLL may be viewed as an integer-N PLL made faster than the normal integer-N PLL by borrowing the speed of the fractional-N PLL during transient. Integer-N PLLs have inherently worse phase noise than fractional-N PLLs. Therefore, in a situation where the phase noise is to be made as small as possible, the hybrid PLL would not be an optimal design choice (as phase noise is a concern in steady state) and the aforementioned tradeoff would not enter the design considerations. However, when an integer-N PLL can meet target phase noise specifications in certain applications (GSM, Bluetooth, and WLAN, for instance) [2], the hybrid PLL can be a valuable design choice. The hybrid PLL example has again illustrated how an apparent tradeoff can be surpassed via separation. Although the main point of this paper has now been delivered, below we will briefly describe the hybrid PLL's architecture and operation for the sake of completeness.

2. Architecture & Operation

Fig. 5 shows the architecture of the hybrid PLL. When the PLL enters a transient state, the two static divide-by-M blocks are disabled and screened out by the two multiplexers, and the crystal oscillator signal $x(t)$ [frequency: f_0] and the prescaler output, $d_1(t)$, are fed to the PFD. This is a standard fractional-N PLL configuration but with no fractional spur reduction circuit. The standard prescaler-accumulator combination inside the dashed box provides a fractional division ratio of $N_d=N+k/M$ through $d_1(t)$. The reference frequency is f_0.

When the PLL attains a phase lock, both divide-by-M blocks are enabled and their outputs, $x_1(t)$ and $d_2(t)$, are fed to the PFD through the two multiplexers. This reconfigured loop is an integer-N PLL: the reference
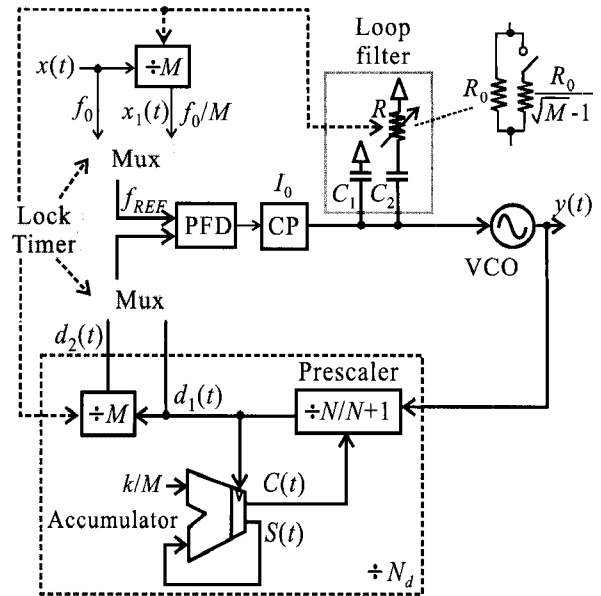

Fig. 5. Overall architecture of the hybrid PLL frequency synthesizer.

frequency is f_0/M; the integer frequency division ratio of $N_d=NM+k$ is provided through $d_2(t)$ by the rather unfamiliar combination of the accumulator, divide-by-M, and prescaler inside the dashed box. The resulting set of output frequencies are the same as in the fractional-N mode.

The simple switching between the two modes is enabled by the absence of fractional spur reduction circuits, and that the overall hybrid PLL of Fig. 5 is almost the normal integer-N PLL, with only 3 additional, simple digital components (shaded areas).

Execution of the mode switching in sync with bandwidth switching is at the heart of the hybrid PLL operation. In conventional Crowley's variable-bandwidth PLLs, the charge pump current I_0 and the loop filter resistance R are changed together to shift the loop bandwidth while maintaining the same phase margin in the loop gain transfer function [5]. In our hybrid PLL, the frequency division ratio N_d naturally changes upon bandwidth switching due to the simultaneous mode switching, and this can serve as an additional parameter in altering the loop bandwidth. This feature permits exploration of a larger design space for bandwidth switching, e.g., when the bandwidth is to be changed by a large amount, this new protocol can lessen the burden of the large I_0-change, as the N_d-change can also contribute. An especially interesting scheme is to not change I_0 at all, but to solely rely on the change of N_d for altering the loop bandwidth (R has to be always changed). This represents a more digital fashion

of bandwidth switching, a polar opposite of the conventional bandwidth shifting where I_0 must be altered.

Our experimental work in [2] firmly confirms the benefit of our hybrid PLL. There are many implementation details, for which we can refer the readers to [2].

IV. EXAMPLE 3: DIGITAL ACCELERATION OF CORRELATION-BASED DIGITAL BACKGROUND CALIBRATION IN PIPELINED ADCS

Correlation-based digital background calibration is being actively studied as a means to mitigate component mismatch errors in pipelined ADCs [6-13]. Currently, a marked drawback of this background calibration method is its slow convergence. The central task in the correlation-based background calibration is the extraction of component mismatch information from correlated data sequences. It is this extraction process that determines the convergence time.

The mismatch information extraction problem has so far been dealt with mostly in time domain [6-13], but it may be alternatively viewed as low pass filtering in frequency domain. In our work by Sun et al [3], we took this elementary notion to the next step, constructing an explicit frequency domain picture of the extraction process. This allowed us to transform the mismatch information extraction problem into a digital filter design problem. In this new framework, we were able to recognize the time separability between convergence speed and convergence accuracy that apparently trade off with each other, and subsequently to apply the Crowley-type variable bandwidth scheme (this is done in an entirely digital

fashion) to surpass the tradeoff, accelerating the convergence speed by a factor of 18.

In this section, we will describe this bandwidth switching scheme to accelerate convergence, after providing the frequency-domain view of correlation-based digital background calibration.

1. Frequency Domain Analysis of Correlation-Based Background Calibration

Fig. 6 is a general model for the correlation-based digital background calibration of capacitor[1] mismatch errors in pipelined ADCs. Detailed implementations may vary, but the model of Fig. 6 captures the essence. In Fig. 6, the real ADC is separated to an ideal ADC with no capacitor mismatch, and the explicit capacitor mismatch, Δ. To understand Δ concretely, think of typical 1-bit or 1.5-bit-per-stage pipelined ADCs. In any given stage, the mismatch between a sampling capacitor C_1 and a feedback capacitor C_2 may be represented by $\Delta=|C_1/C_2-1|$, and we can think that the model of Fig. 6 is being applied to each stage. Alternatively, we can think of Δ as what collectively represents the overall capacitor mismatch.

The calibration procedure in Fig. 6 is as follows. First, the capacitor mismatch Δ is correlated with a causal pseudo-random signal $X[n]$ (+1 or -1 with equal probability for $n \geq 0$; 0 for $n < 0$) and this correlation is added to the real ADC input, $V_{in}[n]$. This sum is passed through the ideal ADC. We denote the pre-calibrated digital output of the ADC as $D_{out}[n]$. As noted in Fig. 6, $D_{out}[n]=V_{in}[n]+X[n]\Delta+e[n]$, where $e[n]$ is quantization noise. Now, $D_{out}[n]$ is correlated with the same digital
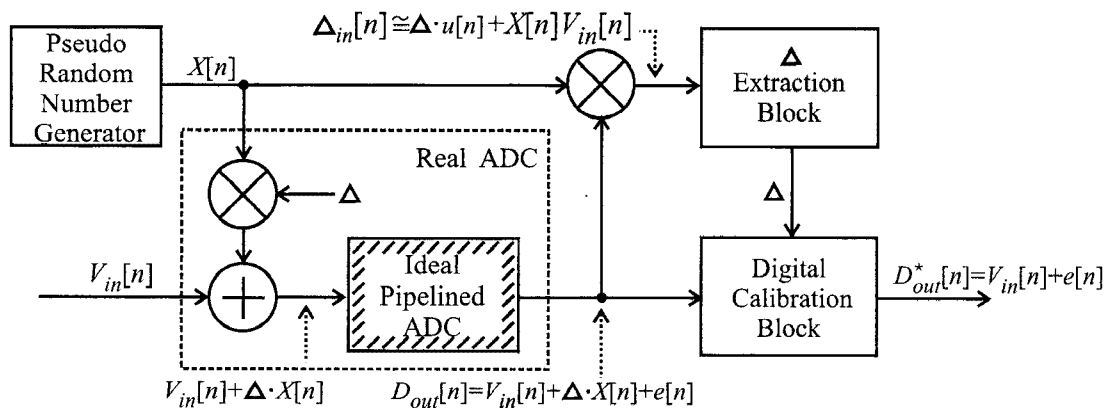

Fig. 6. Correlation-based digital background calibration.

---

[1] We will present our technique in the context of capacitor mismatch errors. Its extension to other nonidealities is straightforward.

pseudo-random signal $X[n]$. Since $X^2[n]=u[n]$ ($u[n]$ is the unit-step function; due to causality), we attain $\Delta \cdot u[n] + X[n]V_{in}[n]+X[n]e[n]$ as the outcome of the second correlation. We will denote this signal as $\Delta_{in}[n]$:

$$\begin{aligned} \Delta_{in}[n] &\equiv \Delta \cdot u[n] + X[n]V_{in}[n] + X[n]e[n] \\ &\cong \Delta \cdot u[n] + X[n]V_{in}[n] \end{aligned} \tag{1}$$

Here we have neglected $X[n]e[n]$, for $V_{in}[n] \gg e[n]$ in any reasonably high resolution application [6].[2] $\Delta_{in}[n]$ in (1) bears the capacitor mismatch information, Δ, which, however, is obscured by the additive term, $X[n]V_{in}[n]$. The key step in the entire background calibration is to extract Δ from $\Delta_{in}[n]$, by removing the additive term. Once Δ is extracted, it can be used in a standard digital block to correct capacitor mismatch errors in $D_{out}[n]$, yielding the desired digital output, $D^*_{out}[n]= V_{in}[n]+e[n]$.

In this model, extracting Δ within a given accuracy from $\Delta_{in}[n]$ of (1) requires a certain number of samples (the index 'N' needs to run over a certain set of integers), which defines convergence time. The convergence time depends crucially on the specific extraction algorithm used. Currently, the sequential iterative method [6,7] or certain signal averaging method [8-13] is used, but in our work of [3], we use a different method, which is the key to our fast convergence solution, as we will see shortly. To see how the iterative algorithm or the currently used averaging differs from our fast-convergence solution, let us first obtain a frequency domain picture of $\Delta_{in}[n]$ of (1). The Fourier transform of the first term of (1), $\Delta \cdot u[n]$, is:

$$\mathscr{F}\{\Delta \cdot u[n]\} = \Delta\left[\frac{1}{1-e^{j\omega}} + \sum_{k=-\infty}^{\infty} \pi\delta(\omega + 2\pi k)\right] \tag{2}$$

As for the second term $X[n]V_{in}[n] \equiv Y[n]$ of (1), since it is a random process, we calculate its power spectral density (PSD) to obtain its frequency domain representation. To this end, let us first denote the autocorrelation function of $X[n]$, $V_{in}[n]$ and $Y[n]$ as $R_{XX}[m]$, $R_{VV}[m]$, and $R_{YY}[m]$, respectively. Since $X[n]$ and $V_{in}[n]$ are independent

random processes, $R_{YY}[m]= R_{XX}[m]R_{VV}[m]$. Suppose $X[n]$ is a pseudo-random signal with period T: after time T, the same pattern of $X[n]$ is repeated. If T is large enough, $R_{XX}[m]$ may be modeled as:

$$\begin{aligned} R_{XX}[m] &= E\big[X[n]\cdot X[n+m]\big] \\ &\cong \frac{1}{2}\sum_{n=-\infty}^{\infty}\delta[m-nT] \end{aligned} \tag{3}$$

where $\delta[n]$ is the discrete-time delta function. This model is approximately valid, as the correlation of $X[n]$ and $X[n+m]$ is approximately[3] zero if m is not an integer multiple of T, and it is exactly one half[4] if m is an integer multiple of T and the two sequences overlap perfectly.

Let us now denote the PSD of $X[n]$, $V_{in}[n]$, and $Y[n]$ as $\Phi_{XX}(e^{j\omega})$, $\Phi_{VV}(e^{j\omega})$, and $\Phi_{YY}(e^{j\omega})$. Using Wiener-Khinchin theorem and (3), we obtain:

$$\begin{aligned} \Phi_{XX}(e^{j\omega}) &= \mathscr{F}\{R_{XX}[m]\} \\ &\cong \frac{\pi}{T}\sum_{k=-\infty}^{\infty}\delta\left(\omega-\frac{2\pi k}{T}\right) \end{aligned} \tag{4}$$

and, subsequently,

$$\begin{aligned} \Phi_{YY}(e^{j\omega}) &= \mathscr{F}\{R_{XX}[m]\cdot R_{VV}[m]\} \\ &\cong \frac{1}{2\pi}\int_{-\pi}^{\pi}\Phi_{XX}(e^{j\theta})\Phi_{VV}(e^{j(\omega-\theta)})d\theta \\ &= \frac{1}{2T}\sum_{k=-\frac{T}{2}}^{\frac{T}{2}}\Phi_{VV}\left(e^{j\left(\omega-\frac{2\pi k}{T}\right)}\right) \end{aligned} \tag{5}$$

The frequency domain illustrations of these results are in Fig. 7. $\Phi_{VV}(e^{j\omega})$ and $\Phi_{XX}(e^{j\omega})$ are in Fig. 7(a) and Fig. 7(b), respectively. Equation (5) indicates that $\Phi_{YY}(e^{j\omega})$ is the sum of repeatedly shifted replicas of $(1/2T)\cdot\Phi_{VV}(e^{j\omega})$, which are shown in Fig. 7(c). From this figure, we can predict that $\Phi_{YY}(e^{j\omega})$ will assume a constant value regardless of ω, as shown in Fig. 7(d). We now confirm this prediction by carrying out the summation of (5). In any practical correlation-based digital background calibration, T is large enough so that $2\pi/T$ is much smaller than the input signal bandwidth. Therefore, $\Phi_{YY}(e^{j\omega})$ of (5) may be rewritten as

---

[2] For a given ADC input, $e[n]$ depends on the value of $X[n]$, and hence $e[n]$ and $X[n]$ could be correlated [13]. If the correlation were strong, the omission of $X[n]e[n]$ should be reexamined, but in practical situations where $V_{in}[n]$ is a random signal, the correlation should be negligibly weak.

[3] The approximate nature originates from the "pseudo"-randomness.
[4] One half instead of one is the result of causality, i.e., $X[n]=0$ for $n<0$.
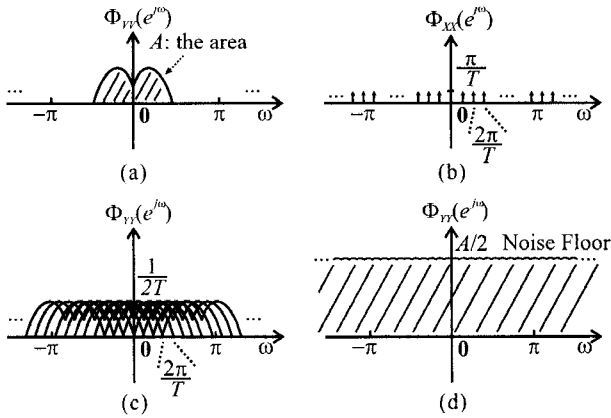
Fig. 7. PSDs of $\Phi_{VV}(e^{j\omega})$, $\Phi_{XX}(e^{j\omega})$, and $\Phi_{YY}(e^{j\omega})$.

Fig. 8. Frequency-domain representation of $\Delta_{in}[n]$ of (1). Log scale.

$$\Phi_{YY}\left(e^{j\omega}\right)=\frac{1}{2}\int_{\omega-\pi}^{\omega+\pi}\Phi_{VV}\left(e^{j\theta}\right)d\theta$$

$$\cong\frac{1}{2}\int_{-\pi}^{\pi}\Phi_{VV}\left(e^{j\theta}\right)d\theta \tag{6}$$

$$=\frac{1}{2}\left[\text{Energy of input }V_{in}\left[n\right]\right]$$

where we have resorted to the fact that $\Phi_{VV}(e^{j\omega})$ has a period of 2π in obtaining the second line.

The analysis above leads to a few meaningful interpretations of the second term $Y[n]=X[n]V_{in}[n]$ of $\Delta_{in}[n]$ in (1), for any practical, large-enough value of T:

1) $\Phi_{YY}(e^{j\omega})$ is not a function of frequency, that is, $Y[n]=X[n]V_{in}[n]$ is a discrete-time white noise. See Fig. 7(d).

2) $\Phi_{YY}(e^{j\omega})$ is half the input signal energy. Therefore, an input signal $V_{in}[n]$ with larger energy leads to a higher white noise floor in Fig. 7(d), making it harder to extract Δ from $\Delta_{in}[n]$ of (1): a longer convergence time is required to average out the larger noise. This also explains why foreground calibration is much faster than background calibration. In foreground calibration, $V_{in}[n]=0$, and hence the noise floor is zero, so we need much less time for convergence.

3) The noise floor level $\Phi_{YY}(e^{j\omega})$ has no dependence on T. Increasing pseudo-random signal period T will *not* help reduce noise floor.

Fig. 8 shows the overall frequency domain picture of $\Delta_{in}[n]$, by combining the white noise $\sqrt{\Phi_n(e^{j\omega})}$ and the mismatch information signal $\mathcal{F}\{\Delta \cdot u[n]\}$ of (2). The mismatch information signal amplitude is equal to the noise amplitude at ω_0. Since the noise, directly affected by $V_{in}[n]$, is rather strong compared to the mismatch infor-
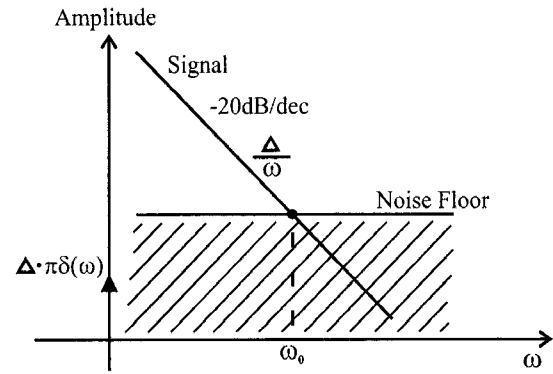
mation signal, ω_0 is quite small. Therefore, in the vicinity of ω_0, $\omega \ll 1$ and we can model $\mathcal{F}\{\Delta \cdot u[n]\}$ of (2) as a -20 dB/dec line, for $\Delta/(1-e^{j\omega})\cong-\Delta/(j\omega)$.

From the analysis above and Fig. 8, we see the function of Δ-extraction block of Fig. 6 is to extract Δ out of the noise floor in frequency domain. We have just transformed the problem of designing a faster Δ-extraction block into a filter design problem. As mentioned earlier, convergence time is determined by the Δ-extraction block. Therefore, attaining faster convergence within a given calibration accuracy is to design a discrete-time LPF with a bandwidth high enough to settle fast (for convergence time) but low enough to reject much of the white noise (for accuracy). Building on this filter design notion, we in the next subsection will explain how our fast convergence solution works.

But before moving on, we would like to further shed light on the correctness of the filter picture, by proving that the sequential iterative method for Δ-extraction used in [6,7] is equivalent to the 1st-order IIR LPF. The iterative method can be generally modeled as:

$$\Delta^*\left[n+1\right]=\Delta^*\left[n\right]+\varepsilon\left(\Delta_{in}\left[n\right]-\Delta^*\left[n\right]\right) \tag{7}$$

Here $\Delta^*[n]$ denotes the estimated capacitor mismatch after the N-th iteration and ε denotes the iteration step size. By plugging $\Delta_{in}[n]$ of (1) into the equation above, we obtain

$$\Delta^*\left[n+1\right]=\Delta^*\left[n\right]+\varepsilon\left(\Delta-\Delta^*\left[n\right]\right)+\varepsilon X\left[n\right]V_{in}\left[n\right] \tag{8}$$

$\Delta-\Delta^*[n]$ can be regarded as the correction term of every iteration, which makes the next iterative value $\Delta^*[n+1]$ closer

to the real capacitor mismatch Δ. If $\Delta^*[n]<\Delta$, $\Delta-\Delta^*[n]>0$, and a larger $\Delta^*[n+1]$ results in the next iteration. Similarly, this algorithm works for $\Delta^*[n]>\Delta$. Consequently, starting from an initial value $\Delta[0]=0$, $\Delta^*[n]$ will gradually converge to Δ. By setting ε to be sufficiently small, $\varepsilon X[n]V_{in}[n]$ will eventually appear as a small random perturbation.

The time-domain picture above can be re-examined in frequency domain. If we consider $\Delta_{in}[n]$ and $\Delta^*[n+1]$ as the input and output of Δ-extraction block, by applying Z-transform to (7), we obtain:

$$\frac{\Delta^*(z)}{\Delta_{in}(z)} = \frac{\varepsilon}{z-1+\varepsilon} \tag{9}$$

The iterative Δ-extraction process is no more than a 1st-order IIR LPF with passband bandwidth ε. The iterative algorithm lets $\Delta_{in}[n]$, which contains Δ and the noise term, go through the 1st-order IIR LPF to extract Δ by filtering out the noise.

The analysis above further supports our picture that the design of the Δ-extraction block is essentially a filter design problem. From now on, we will treat the Δ-extraction block exclusively as a discrete-time LPF, and will move on to discuss how we design the LPF to achieve fast convergence.

2. Fast Convergence Technique

Based on the frequency domain picture of $\Delta_{in}[n]$ in Fig. 8, we clearly see the trade-off in deciding the LPF bandwidth. If the bandwidth is small, the convergence will be accurate rejecting more noise, but it will take long for calibration to converge. If the bandwidth is large, convergence will be fast, but more noise is filtered in, undermining calibration accuracy. Convergence time trades off with calibration accuracy via the bandwidth. In light of this observation, it is easy to appreciate the disadvantage of the 1st-order LPF (both the iterative algorithm [6,7] and the averager [8-13]): the bandwidth is fixed and the tradeoff is directly faced. To satisfy a required accuracy, the LPF bandwidth is set small enough, resulting in a long convergence time. Such design constraint becomes more troublesome in high resolution applications where calibration accuracy requirement is stringent.

Our fast convergence technique is enabled by relaxing the tradeoff between convergence time and accuracy.

This is achieved by incorporating the Crowley-type bandwidth switching scheme in the discrete-time IIR LPF: we use a larger bandwidth during the initial calibration transient and a smaller bandwidth near and during the final convergence (steady-state). This variable bandwidth technique is based on the notion that convergence speed matters only during transient, while convergence accuracy matters only during steady state. During the initial calibration phase, in order to achieve faster convergence, a larger bandwidth is used. Although more noise is filtered in due to the larger bandwidth, during this early phase of calibration, accuracy is no concern. As convergence is approached, bandwidth is switched to a smaller value to reduce steady-state convergence errors. By using this adaptive bandwidth scheme, we circumvent the tradeoff, substantially reducing convergence time for a given accuracy. In MATLAB behavioral simulations of a 13-bit pipelined ADC consisting of 12 1.5-bit stages, the convergence speed was increased by a factor of 18 by our technique, attesting to its validity. We refer readers to [3] for details of the simulation results.

The variable bandwidth scheme can be implemented in an all-digital fashion at low cost in discrete-time filters by altering multiplication coefficients, as shown in Fig. 9 for a 3rd-order LPF example.[5] The rest extra cost is simple combinational logic gates and a counter to determine
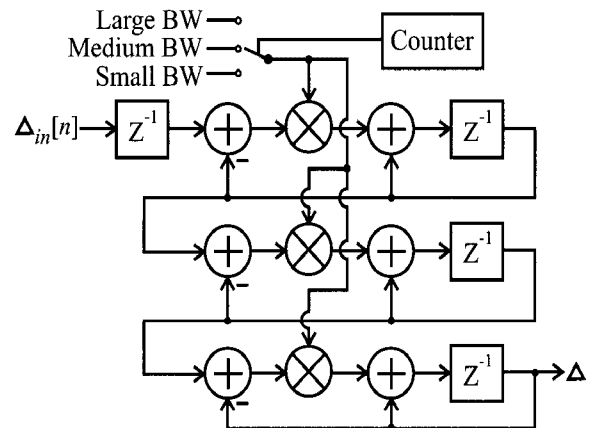

Fig. 9. 3rd-order discrete-time IIR LPF with a variable bandwidth scheme.

---

[5] We show an example of a 3rd-order filter, for increasing the filter order is another way of relaxing the tradeoff between the convergence speed and the convergence accuracy: a higher order increases the convergence speed for a given accuracy. This important technique is also the outcome of the frequency-domain analysis of the correlation-based digital background calibration, but we did not go over this, as it is irrelevant to the theme of this paper. We refer interested readers to [3] for details of this technique.

bandwidth switching times.

V. CONCLUSIONS

We have discussed several published design examples in which tradeoffs can be surpassed if the relevant traits are somehow separated in time or space. We hope that the perspective presented in this paper can be applied to other designs.

REFERENCES

[1] W. Andress and D. Ham, "Standing wave oscillators utilizing wave-adaptive tapered transmission lines," *IEEE J. Solid-State Circ.*, Vol.40, No.3, pp.638-651, March 2005.

[2] K. Woo, Y. Liu, E. Nam, and D. Ham, "Fast-lock hybrid PLL combining fractional-N & integer-N modes of differing bandwidths," *IEEE J. Solid-State Circ.*, Vol.43, No.2, pp.379-389, February 2008.

[3] N. Sun and D. Ham, "Digital acceleration of correlation-based digital background calibration in pipelined ADCs," *Technical Report*, Harvard University, August 2008. This report is available at http://www.seas.harvard.edu/~donhee/digia.pdf.

[4] W. Andress, K. Woo, and D. Ham, "Surpassing tradeoffs by separation: examples in frequency generation circuits," *SiRF*, January 2008.

[5] Crowley, "Phase locked loop with variable gain and bandwidth," US Patent 4,156,855, May 29th, 1979.

[6] J. Li and U. Moon, "A background calibration techniques for multi-stage pipelined ADCs with digital redundancy," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, Vol.50, No.9, pp.531-538, Sept. 2003.

[7] M. Taherzadeh-Sani and A. A. Hamoui, "Digital background calibration of capacitor-mismatch errors in pipelined ADCs," *IEEE Trans. Circuits Syst. II, Brief Papers*, Vol.53, No.9, pp.966-970, Sept. 2006.

[8] R. Jewett, K. Poulton, K. Hsieh, and J. Doernberg, "A 12-b 128M samples/s ADC with 0.05LSB DNL," *Proc Int. Solid-State Circuits Conf.*, pp.138-139, Feb. 1997.

[9] J. Ming and S. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," *IEEE J. Solid-Sate Circuits*, Vol.36,

No.9, pp.1489-1497, Oct. 2001.

[10] I. Galton, "Digital cancellation of D/A converter noise in pipelined A/D converters," *IEEE Trans. Circuits Syst. II*, Vol.47, pp.185-196, Mar. 2000.

[11] E. Siragusa and I. Galton, "A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, Vol.39, pp.2126-2138, Dec. 2004. ,

[12] K. El-Sankary and M. Sawan, "A digital blind background capacitor mismatch calibration for pipelined ADC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, Vol.51, No.10, pp.507-510, Oct. 2004.

[13] A. Panigada and I. Galton, "Digital background correction of harmonic distortion in pipelined ADCs," *IEEE Trans. Circuits Syst. I, Regular Papers*, Vol.53, No.9, pp.1885-1895, Sept. 2006.

Nan Sun received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2006. He is currently working toward the Ph.D. degree in electrical engineering at Harvard University where his major research interests lie in RF, analog and mixed-signal integrated circuit design, and also in silicon bio-molecular sensors.

He ranked first in EE Dept. at Tsinghua University, and graduated with highest honor and outstanding thesis award. He was the recipient of Samsung Outstanding Student Award in 2003, Hewlett Packard Outstanding Student Award in 2006, and Analog Device Outstanding Student Designer Award in 2007. He was also the recipient of Harvard Teaching Fellow Award in 2008.

William F. Andress received the B.S. degree (highest honors) in electrical engineering and computer science from Harvard University, Cambridge, MA, in 2004, and has begun working toward the Ph.D. degree in electrical engineering and applied physics, also at Harvard. His research interests include RF integrated circuits and ultrafast electronics in conjunction with stochastic resonance. Mr. Andress was awarded the Thomas T. Hoopes Prize for best senior thesis and is a recipient of the Analog Devices Outstanding Student Designer Award.

Kyoungho Woo received the B.S. degree from Seoul National University, Seoul, Korea, in 1999, and the M.S. degree from Stanford University, Stanford, CA, in 2004, all in electrical engineering. He is currently working toward the Ph.D. degree in electrical engineering at Harvard University.

In 2003, he was with the timing-design group at the Sun Microsystems, Sunnyvale, CA, where he developed a timing analysis code for the Ultraspac III microprocessor. He is also with an analog design team at the Cavium Networks, Marlborough, MA, as a part-time employee where he is developing a multi-standard high-speed serial links transmitter. His current research interest lies in analog and mixed-signal integrated circuit design, especially in PLL frequency synthesizers and high-speed serial links.

He has been the graduate fellow of the Korea Foundation for Advanced Studies since 2002, and is the recipient of the Analog Devices Outstanding Student Designer Award in 2006.

Donhee Ham is John L. Loeb Associate Professor of the Natural Sciences and Associate Professor of Electrical Engineering at Harvard University, where he is with the School of Engineering and Applied Sciences (Programs: Electrical Engineering, Applied Physics).

He received the B.S. degree in physics from Seoul National University, Korea, in 1996, where he graduated summa cum laude with the Valedictorian Prize as well as the Presidential Prize, ranked top 1st across the Natural Science College, and also with the Physics Gold Medal (sole winner). Following 1.5 years of mandatory military service in the Republic of Korea Army, he proceeded to California Institute of Technology, where he received the M.S. degree in physics in 1999 working on general relativity and gravitational astrophysics, and Ph.D. degree in electrical engineering in 2002 winning the Charles Wilts Doctoral Thesis Prize, Best thesis award in Electrical Engineering. His doctoral work examined statistical physics of electrical circuits. He was the recipient of the IBM Doctoral Fellowship, Li Ming Scholarship, IBM Faculty Partnership Award, IBM Research Design Challenge Award, and the fellow of the Korea Foundation of Advanced Studies. He shared Harvard's Hoopes prize with William Franklin Andress. He was recognized by *MIT Technology Review* as among the world's top 35 young innovators in 2008 (TR35), for his group's work on CMOS RF biomolecular sensor utilizing nuclear magnetic resonance to pursue early disease detection.

Donhee Ham's work experiences include Caltech-MIT Laser Interferometer Gravitational Wave Observatory (LIGO), IBM T. J. Watson Research Center, IEEE conference technical program committees including the *IEEE International Solid-State Circuits Conference (ISSCC)* and *the IEEE Asian Solid-State Circuits Conference (ASSCC)*, advisory board for *the IEEE International Symposium on Circuits and Systems (ISCAS)*, international advisory board for the Institute for Nanodevice and Biosystems, and various US, Korea, and Japan industry, government, & academic technical advisory positions on subjects including ultrafast electronics, science & technology at the nanoscale, and the interface between biotechnology and microelectronics. He is serving as a guest editor for *the IEEE Journal of Solid-State Circuits, (JSSC)* and is a co-editor of *CMOS Biotechnology* with Springer (2007).

Ham's current research focus is on (1) RF/microwave, analog & mixed-signal ICs, (2) ultrafast 1-dimensional electron transport, (3) soliton electronics, (4) applications of CMOS ICs in biotechnology, and (5) non-equilibrium statistical physics of electrical circuits.