A Continuously Tunable LC-VCO PLL with Bandwidth Linearization Techniques for PCI Express Gen2 Applications

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Abstract—**This paper describes bandwidth linearization techniques in phase-locked loop (PLL) design for common-clock serial link applications. Utilizing a continuously tunable single-input dual-path LC VCO and a constant-gain phase detector, a proposed architecture is well suited to implementing PLLs that must be compliant with standards that specify minimum and maximum allowable bandwidths such as PCI Express Gen2 or FB-DIMM applications. A prototype 4.75 to 6.1-GHz PLL is implemented in 90-nm CMOS. Measurement results show that the PLL bandwidth and random jitter (RJ) variations are well regulated and that the use of a differentially controlled dual-path VCO is important for deterministic jitter (DJ) performance.**

Index Terms—**PLL, tunable LC-VCO, PCI Express Gen2, bandwidth linearization**

I. Introduction

As advanced silicon technology drives the demand for high speed I/O links, serial link area and power constraints along with performance requirements have become increasingly strict. Since the PCI Express (PCIe) specification was finalized in 2002, it has been rapidly adopted as the next generation interconnect between microprocessors and peripheral components [1]. Compared with PCI or PCI-X, PCIe is based on a point-to-point serial link topology as illustrated in Fig. 1. While PCI provides up to a per-bit 1-Gb/s data rate with a a 64-bit bus at a 133-MHz clock rate, PCIe provides a 2.5-Gb/s data rates with a single-bit serial connection and can provide higher data rate simply by merging each lane at the same time. PCI Express Gen2 (PCIe2) is a second generation of PCIe with a data rate of 5 Gb/s. In contrast to network communication links which are usually included in low-volume and high-cost systems, PC communication links are built for high-volume and low-cost systems where low-quality reference clock sources are often used. Hence, unlike other communication links, the jitter transfer function of the reference clock needs to be carefully considered in phase-locked loop (PLL) design [1,2]. The key requirements of the PLL for PCIe2 are summarized in Table 1. Since PCIe2 operates at twice the data rate of PCIe, the jitter budget is tighter, demanding random jitter (RJ) of less than 1.4 ps. The PLL bandwidth is specified by the standard, for example, it must be within a range of 8-16 MHz in the case where up 3-dB peaking is allowed in jitter transfer function. As the loop para

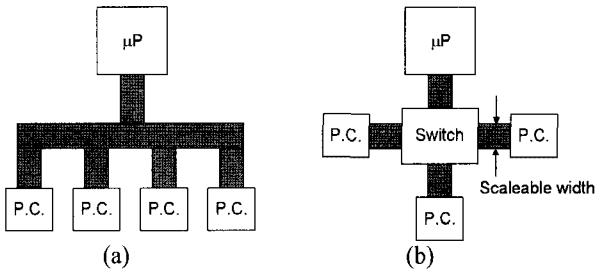

Fig. 1. Interconnect between microprocessor and peripheral components: (a) PCI or PCI-X, and (b) PCI Express.

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Table 1. PLL key requirements for PCIe2.

Data rate	5Gb/s
Unit interval (UI)	200ps +/- 300ppm
Jitter Generation (RJ)	
TX	1.4ps$_{rms}$
RX	1.4ps$_{rms}$
REFCLK	3.1ps$_{rms}$
Jitter Transfer*	
Max. bandwidth	16MHz with 3dB peaking
Min. bandwidth	8MHz with 3dB peaking
	5MHz with 1dB peaking

*For 2.5Gb/s PCIe, 3 – 22MHz with 3dB peaking is required.

meters of the on-chip PLL vary a lot over process and temperature, a means of achieving uniform bandwidth to meet PCIe2 specifications is needed. In this work, we present a PLL architecture that can be compliant with standards that specify minimum and maximum allowable PLL bandwidths by utilizing a continuously tunable single-input dual-path LC VCO and a constant-gain phase detector.

This paper is organized as follows. In section II, PLL design considerations for common-clock serial links are addressed. Then, the proposed PLL architecture with uniform bandwidth control and circuit implementation are presented in section III and section IV, respectively. Section V presents the measurement results, followed by conclusions in section VI.

II. PLL Design for Common-Clock Serial Links

1. Jitter Transfer of Reference Source

Fig. 2 shows jitter contribution of the reference source in two typical clock-and-data recovery systems (CDRs) which are often employed in serial link systems [2]: (a) an embedded clock system having a PLL-based CDR; and (b) a common-clock system where the CDR is based on a semidigital delay-locked loop (DLL) with phase interpolation (PI) [3]. The PLL-based CDR does not need a reference clock, hence the transmitter jitter tracking by the CDR can be simply represented by a high-pass filter, 1 - $H_2(s)$ as illustrated in Fig. 2(a). The PI-based CDR, on the other hand, needs the reference clock for the PLL to generate a multiphase clock in the receiver. Since the same reference clock is used for both the transmitter and

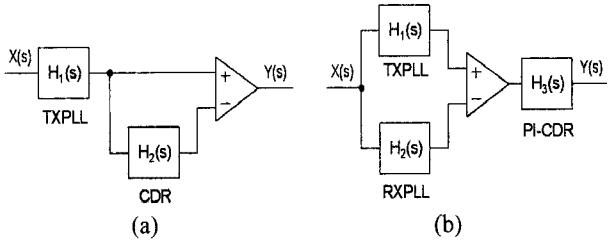


Fig. 2. Jitter transfer of reference source: (a) data-clocked system, and (b) common-clock system.

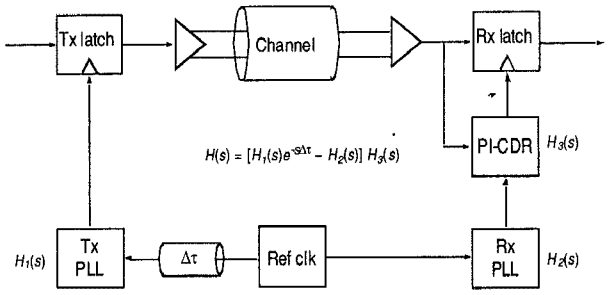


Fig. 3. Common-clock serial link system.

the receiver, there will be partial correlation in the relative phase variation between the transmitter and receiver PLLs. In these types of serial links, it is possible to leverage this partially correlated jitter characteristic to mitigate the detrimental effects of reference clock jitter. Generally, specific jitter transfer characteristics must be satisfied in the transmitter PLL design, which can be accomplished by controlling PLL bandwidths between minimum and maximum ranges.

The common-clock serial link architecture shown in Fig. 3 offers certain performance advantages over source-synchronous serial link architectures, while enabling a lower cost link system solution than embedded clock systems. Therefore, the common clock link system has been rapidly adopted for short distance links, including computer centric I/O links (PCIe) and memory I/O links (FB-DIMM). In this work, the common-clock serial link system is also assumed in determining the objectives for the PLL design.

2. Bandwidth Variation

Maintaining constant bandwidth over process and temperature variations is challenging in fully integrated PLL designs. Since one option under the PCIe2 specification requires less than 1-dB jitter peaking, an overdamped loop should be considered. The PLL bandwidth is mainly determined by a phase detector gain, loop filter (LPF) characteristics, a division ratio, and a VCO gain. Since

the VCO gain affects both noise and bandwidth most significantly, the VCO design is critical to achieving performance targets. A ring VCO enables low cost design and offers wide tuning range, but it suffers from poor phase noise performance. The phase noise of the ring VCO can be suppressed substantially with a wideband PLL, but the increased noise bandwidth results in worse RJ performance than a PLL having an LC VCO. The high-Q LC VCO, however, suffers from a narrow tuning range. The trade-off between noise performance and tuning range can be overcome by having multiple varactors [4-5] or by adopting a dual-path control [6-13].

Fig. 4 shows an LC VCO with a digitally programmable varactor array. By having multiple coarse-tuning varactors with sufficient frequency overlap and a fine-tuning varactor to set precise VCO frequency within the band selected by digital coarse tune controls, a relatively wide tuning range can be achieved without degrading phase noise performance. It is clear from the tuning curves shown in Fig. 4, however, that a drawback of this approach is VCO gain variability: as the VCO fine-tuning voltage moves from a point near center of its transfer characteristic to a point near edge of its transfer characteristic in any band, the VCO gain drops significantly. While center frequency shift due to process variation can be calibrated during system initialization, center frequency drift due to temperature and supply changes must be accommodated by the PLL during normal operating mode. As indicated by the circles on the tuning curve example of Fig. 4, VCO gain can drop dramatically at the target operating frequency as die temperature changes from 25 to 100 °C. Note further that because changing bands will result in an abrupt frequency change during normal operation, the PLL must tolerate temperature and supply changes while remaining in the band chosen at calibration. Large VCO gain variation is harmful to PLL performance unless additional compensation circuits are implemented for VCO gain linearization.

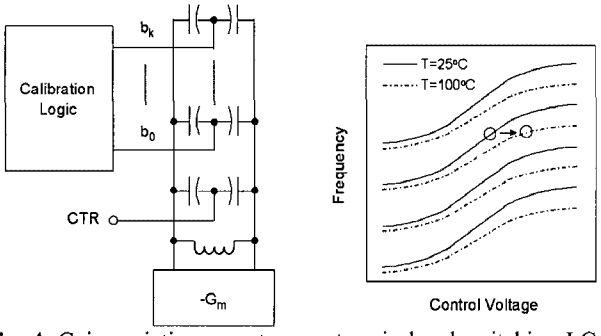


Fig. 4. Gain variation over temperature in band-switching LC VCO.

An alternative to the coarse band-switch VCO is a dual-path VCO that replaces calibration logic and coarse tuning varactors with a large analog varactor and associated new analog control while maintaining a fine-tuning path similar to that used on the band-switch design. In this design, a high-gain analog coarse-tuning path tunes the VCO frequency over the entire tuning range while a parallel low-gain fine-tuning path sets the small-signal VCO gain. In practice, however, the dual-path VCO offers several design challenges. Firstly, the high gain of the analog coarse tuning path is more vulnerable to noise than the digital band-switch path of the previous design; noise coupling to the analog coarse control node can strongly modulate the VCO output. Furthermore, since the gain of the analog coarse-tuning path is much higher than that of the fine-tuning path, any coupling due to supply noise or substrate noise can affect the VCO noise performance. Secondly, the dual-path control often requires a PLL topology change such as the introduction of an additional voltage node from the loop filter [6-9] or an additional phase detector (or charge pump) [10-12]. Lastly, for stability reason, the coarse-tuning control loop must have much narrower bandwidth than the PLL bandwidth, increasing the area of the stabilizing capacitor in the coarse-tuning path.

III. ARCHITECTURE

1. Uniform Bandwidth Control

The PLL bandwidth is mainly determined by phase detector gain, LPF characteristics, division ratio, and VCO gain. One approach to minimizing phase detector gain variation is having the charge pump bias current generated by the on-chip resistor and the bandgap reference voltage. As illustrated in Fig. 5, the phase detector gain, which is set by the product of the charge pump current and the resistor in the LPF (the impedance of the LPF is mostly set by the resistor), will remain constant over temperature and process variations, since the charge pump current variation is inversely proportional to the resistor variation. The capacitor variation in the LPF will affect the phase margin of the feedback loop, but its impact on loop dynamics is relatively less significant. In

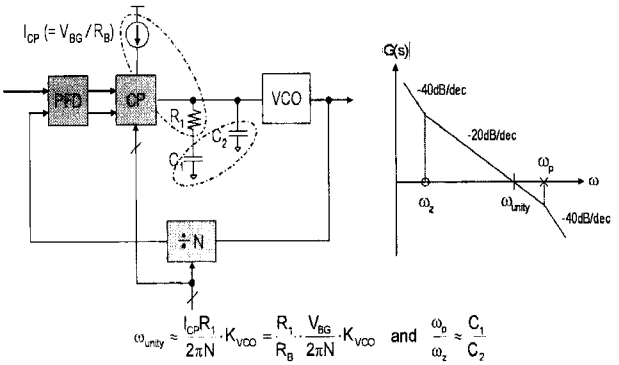


Fig. 5. Uniform bandwidth control.

particular, the shunt capacitor and the series capacitor act to compensate for each other to a certain degree with respect to the phase margin; if the capacitance increases, the shunt capacitor reduces the phase margin, but the series capacitor increases the phase margin. Since the division ratio is set by explicit control signals, these controls can be used to set the charge pump current so that it compensates for division ratio changes in the overdamped PLL. If these approaches are applied, VCO gain variation is the primary remaining factor affecting overall PLL bandwidth variation.

2. Single-Input Dual-Path LC VCO

Fig. 6 shows the block diagram of the proposed PLL. Instead of having a digitally programmable varactor array, a single coarse-tuning varactor controlled by an analog control voltage is used. Unlike prior arts in which dual-path controlled LC VCOs are used [6,10], the proposed PLL not only uses a coarse-tuning varactor with a coarse-tuning linear amplifier after the LPF [13] but also further increases the open-loop gain at dc [11], linearizing the gain of the VCO and the charge pump. Furthermore, the LC VCO has the inputs of the coarse- and fine-tuning linear amplifiers controlled by same voltage in the loop filter, namely a single-input dual-path control. Hence, the architecture does not require PLL topology modification and is also comparable to conventional PLLs using ring VCOs, while maintaining wide tuning range and superior noise performance.

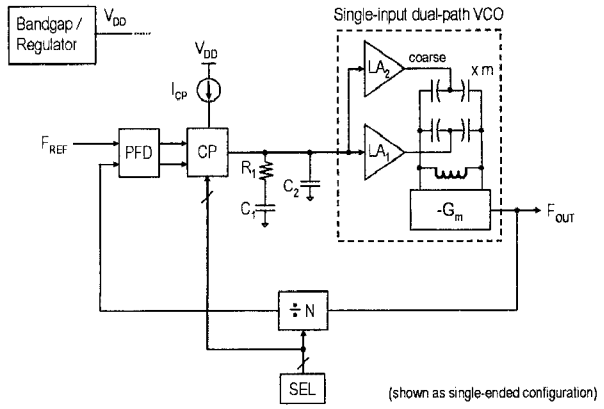


Fig. 6. Proposed PLL architecture.

In VCO design, the linear amplifier in the coarse-tuning path is designed to have higher gain than the linear amplifier in the fine-tuning path. Fig. 7 illustrates the relationship between the coarse-tuning range and the fine-tuning range. In Fig. 7, the solid line represents the tuning curve of the larger coarse-tuning varactor and the dotted line represents the tuning curve of the smaller fine-tuning varactor. When the gain of the coarse-tuning linear amplifier k is greater than 1, the actual voltage range in the LPF (or, equivalently, at the output of the charge pump) will be narrower than the output voltage range of the coarse-tuning linear amplifier by a factor k. In Fig. 7, the voltage range $\pm V_F$ or $\pm V_c/k$ represents the input voltage range of both coarse-tuning and fine-tuning linear amplifiers and the output voltage range of the fine-tuning linear amplifier, while the voltage range $\pm V_c$ represents the output voltage range of the coarse-tuning linear amplifier only.

The proposed architecture thus acts to center the fine-tuning operating range of the VCO in a very linear part of the tuning curve, effectively minimizing VCO gain

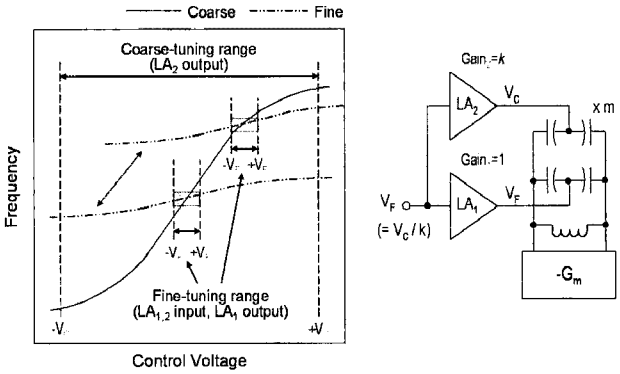


Fig. 7. Tuning range of single-input dual-path LC-VCO.

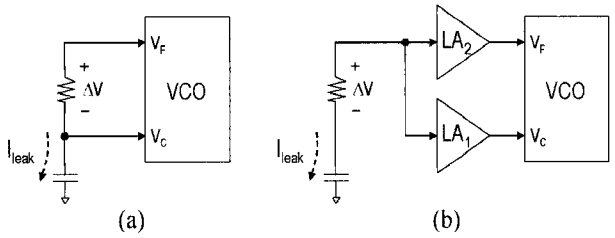


Fig. 8. Leakage current effect: (a) dual-input dual-path VCO, and (b) single-input dual-path VCO.

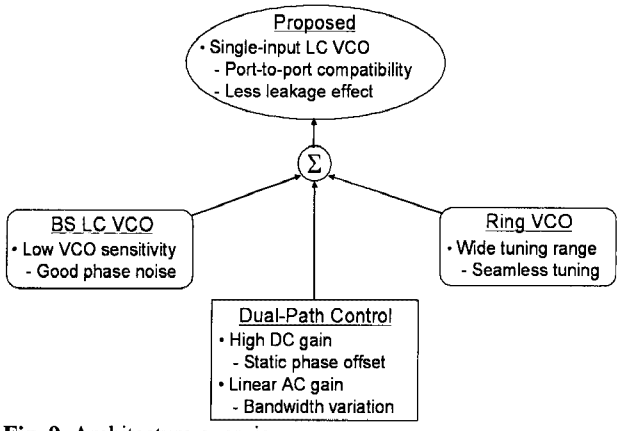


Fig. 9. Architecture overview.

variation, the primary remaining source of overall PLL bandwidth variation. Reduced voltage range in the LPF also has the additional benefit of relaxing the charge pump design requirements as it minimizes current mismatch between UP/DN mirrors, resulting in a further benefit of improved static phase error performance. The single-input VCO also provides more immunity to leakage current effects. As illustrated in Fig. 8, the leakage current in the on-chip LPF does not induce an offset voltage between the coarse-tuning path and the fine-tuning path in the proposed architecture. The advantages of the proposed architecture are reviewed in Fig. 9. Note that the dual-path architecture's use of a high gain coarse-tuning path raises potential deterministic jitter (DJ) exposures that must be addressed in the PLL implementation for the approach to be successful.

3. Loop Dynamics

Fig. 10(a) shows the linear model of the proposed PLL, where K_{PD}, K_{VCO}, $F(s)$, M, and N represent phase detector gain, VCO gain, the loop filter transfer function, coarse-tuning gain factor, and division ratio, respectively. The coarse-tuning gain factor M is the ratio of the coarse-tuning path gain to the fine-tuning path gain, which includes the linear amplifier gain ratio as well as the varactor size ratio. Open-loop gain of the proposed PLL can be written as follows:

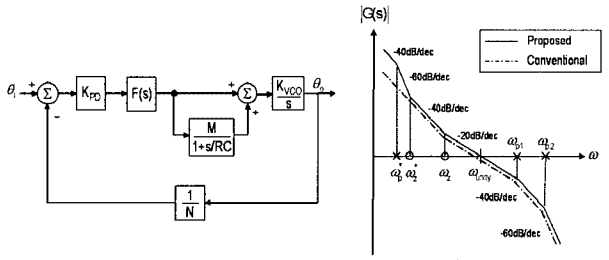
$$G(s) = \frac{K_{PD}}{N} \cdot F(s) \cdot \left(1 + \frac{M}{1+sRC}\right) \cdot \frac{K_{VCO}}{s} = G_0(s) \cdot \left(\frac{M+1+sRC}{1+sRC}\right) \quad (1)$$

where the open-loop gain of a conventional PLL $G_o(s)$ is given by

$$G_0(s) = \frac{K_{PD}}{N} \cdot \frac{K_{VCO}}{s} \cdot F(s) \quad (2)$$

Compared to conventional Type-II PLLs, the proposed PLL has an additional pole and a zero located at s = $1/RC$ and $(M+1)/RC$, respectively. Fig. 10(b) shows the Bode plot of the open-loop gain for the proposed PLL and the conventional PLL. Note that a high coarse-tuning gain factor M can degrade the phase margin even with narrow coarse-tuning bandwidth. Hence, it is important to keep the additional pole and zero at much lower frequencies than the unity-gain frequency for jitter peaking requirements.

Fig. 11 shows the transient behavioral simulation results of the proposed PLL. Closed-loop behavioral simulation was done using the *CppSim* tool [14]. In this simulation, the PLL bandwidth is normalized to 1. In Fig. 11(a), different coarse-tuning gain factors are chosen, but the bandwidth of the coarse-tuning path is fixed to 0.1. The first plot shows a PLL control voltage waveform with a coarse-tuning gain factor of zero. In this case, loop dynamics of the proposed PLL is same as that of the conventional PLL. The second plot shows that the coarse-tuning gain factor of 1 has negligible effect to stability with the coarse-tuning bandwidth of 0.1. In the case of the coarse-tuning gain factor of 10, shown in the third plot, there is a slight overshoot in the transient waveform. It shows that increased coarse-tuning gain factor degrades phase margin, as predicted in the previous analysis. With extremely high coarse-tuning gain factor, shown in the fourth plot, the PLL can be unstable. In Fig. 11(b), the coarse-tuning gain factor is fixed to 10, and the bandwidth of the coarse-tuning path is varied from 0.01 to 10. As shown in the third and fourth plots, widening the bandwidth of the coarse-tuning path can degrade phase margin significantly.



(a) (b)

Fig. 10. Loop dynamics: (a) linear model, and (b) open-loop gain comparison.

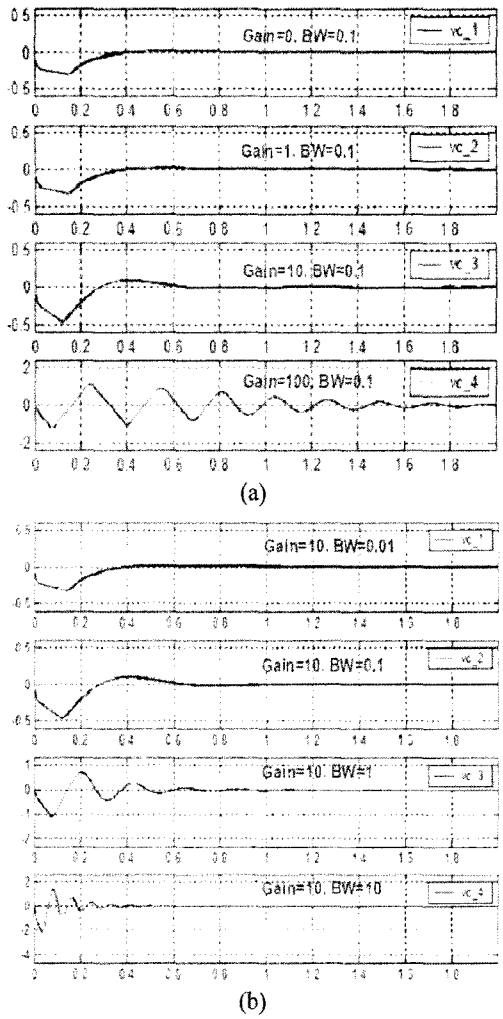


Fig. 11. PLL behavioral simulations: (a) with different coarse-tuning dc gains, and (b) with different coarse-tuning bandwidths.

IV. CIRCUIT IMPLEMENTATION

A prototype PLL was designed with front-end division ratios of 8/10/16/20. To achieve a low-power programmable 8/10/16/20 divider, a 4/5 dual-modulus divider was employed in the middle of the divider chain. The charge pump current is digitally programmable and controlled in an adaptive way such that different division ratios set the appropriate charge pump current value to maintain constant PLL bandwidth. A fully on-chip bandgap reference circuit and supply voltage regulator are included in the design to enable good power supply rejection. A key drawback of the dual-path VCO is that it includes a high-gain coarse-tuning path which can degrade PLL DJ performance. To address this concern and to broadly enhance immunity to supply and substrate noise coupling, a VCO using differentially-controlled varactors along with a differential linear amplifier was designed and used in this implementation [15].

Fig. 12 shows the schematic of the linear amplifier used in the coarse-tuning path and the fine-tuning path. The linear amplifier in the coarse-tuning path is designed with much lower bias current and has much narrower bandwidth than that in the fine-tuning path. The linear amplifier is implemented as a simple differential amplifier with source degeneration to minimize the noise contribution from active devices and to achieve linear gain. Compared with the linear amplifier in the fine-tuning path, the linear amplifier in the coarse-tuning path has three times higher dc gain, and, due to additional RC filtering, much narrower bandwidth; this extra filtering also helps to reduce DJ sensitivity of the PLL at the coarse input. The thermal noise contribution from the series resistor will be suppressed by the PLL open-loop gain since the linear amplifier is placed after the loop filter, as illustrated in Fig. 12. Hence, a high-value resistor can be implemented to reduce the capacitor size. A key layout consideration is minimizing substrate noise coupling to the output of the linear amplifier.

Fig. 13 shows the simplified schematic of the fully differential charge pump. The charge pump output current is digitally programmable (not shown in Fig. 13). The

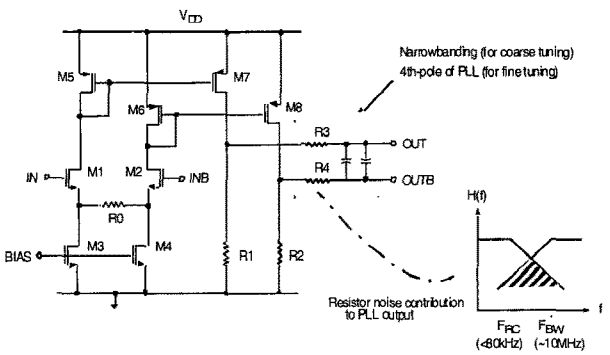


Fig. 12. Linear amplifier and noise consideration.

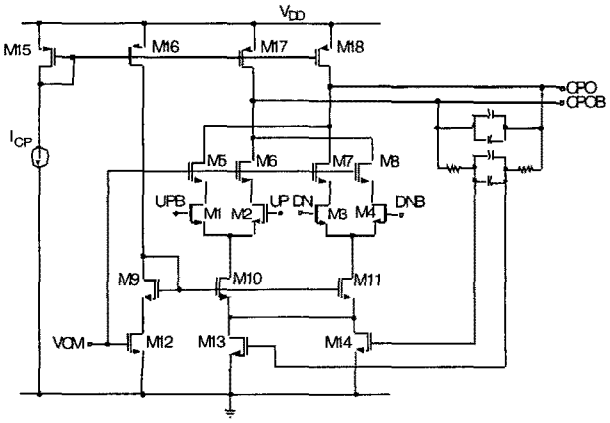


Fig. 13. Charge pump and LPF with CMFB.

transistors M5-M8 provide cascoded output stages to minimize charge coupling between switching devices M1-M4 and the LPF. Common-mode feedback (CMFB) is implemented using linear-mode transistors M13 and M14. The common-mode reference voltage is applied not only to the gate of M12 for setting the common-mode voltage but also to the gates of M5-M8 for cascode biasing. For the PLL, instead of using the direct charge pump output signals to provide CMFB information, the voltage across the capacitor in the loop filter is used, thus avoiding the high-frequency voltage ripple caused by the resistors in the loop filter [16].

V. Experimental Results

The prototype PLL fabricated in 90-nm CMOS is shown in Fig. 14. Another PLL with a dual-path VCO using a conventional varactor and a linear amplifier having a single-ended output is also implemented to enable a power supply rejection comparison. The active die area is 0.68 x 0.52 mm^2. The PLL excluding output buffers consumes 20 mW from a 1.2 V supply.

Fig. 15 shows the measured VCO output spectrum at 5 GHz. The measured spurious tones are less than -56 dBc, which results in a negligible periodic jitter (PJ) contribution (<0.01 UI) to the overall DJ. Fig. 16 shows the measured VCO output phase noises over process variation. To show that the PLL bandwidth variation is well regulated in the proposed PLL, several PLLs in different process-corner parts are tested. The striped wafer where each stripe has controlled channel length and threshold voltage variations provides up to 6-sigma process corners. The metal variation including inductor variation is not controlled in the wafer. At nominal conditions, the phase noise at 1 MHz offset frequency from the carrier is -108 dBc/Hz, and the measured bandwidth is approximately 8 MHz. The phase noise characteristics as shown in Fig. 16 do not exhibit noise peaking, indicating that all the PLLs have over-damped loop dynamics over process. Fig. 17 shows RJ variation over process and temperature,

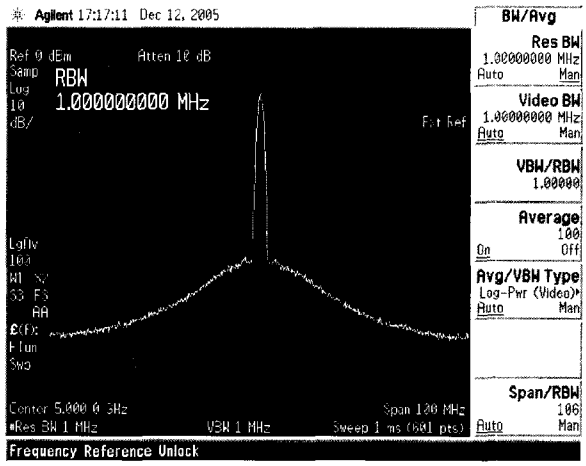


Fig. 15. Measured VCO output spectrum at 5 GHz.

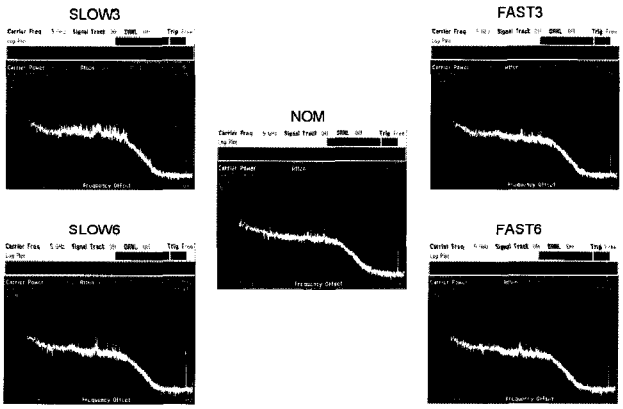


Fig. 16. Measured output phase noises over process variation. (e.g. SLOW3 = process corner with -3σ, FAST6 = process corner with +6σ)

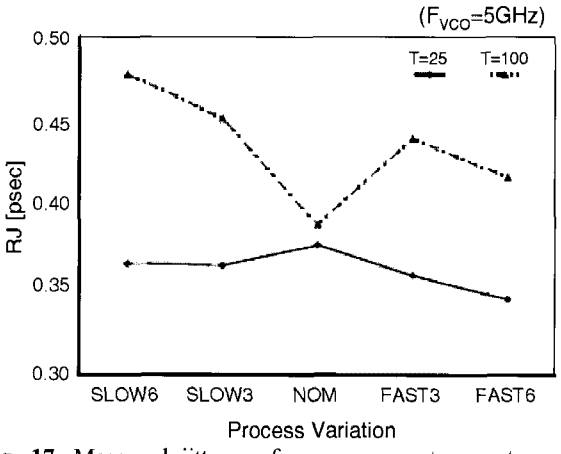


Fig. 17. Measured jitter performance over temperature and process variations.

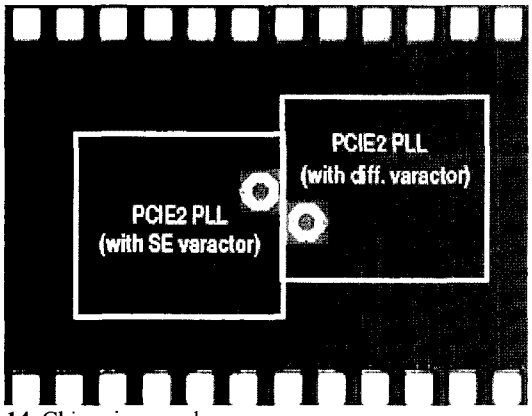


Fig. 14. Chip micrograph.

where a noise integration bandwidth of 3 MHz to 1 GHz is used. RJ performance varies from 0.34 ps-rms to 0.48 ps-rms over process and temperature variations, while the PLL bandwidth was measured to be within a range of 8-12 MHz, showing that bandwidth variation is well controlled.

Fig. 18 shows the measured tuning curve of the dual-path VCO. The tuning range of 4.75 to 6.1 GHz is achieved with VCO gain of 450 MHz/V and +/-0.2-V differential input control voltage range. Since the typical input voltage range for the fine tuning curve is less than +/-0.2 V due to the high coarse tuning gain factor, highly linear fine-tuning VCO gain can be achieved.

As mentioned previously, a high-gain coarse tuning node exists in the dual-path VCO. The sensitive analog node within the VCO can therefore contribute to DJ due to supply and substrate noise coupling. In an experiment designed to assess the DJ impact of this sensitivity, supply noise with 100-mV_{pp} amplitude at various frequencies was applied to the PLL. Since the PLL has an

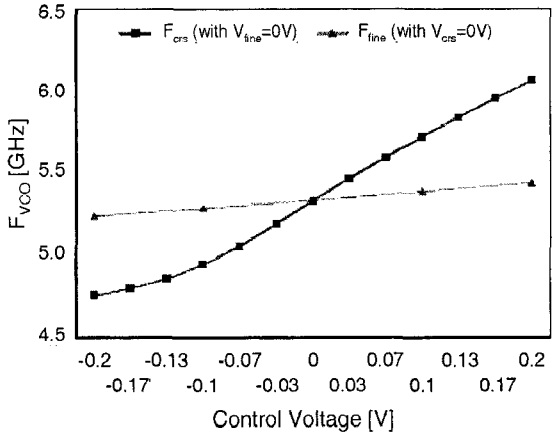


Fig. 18. Measured VCO coarse- and fine-tuning curves.

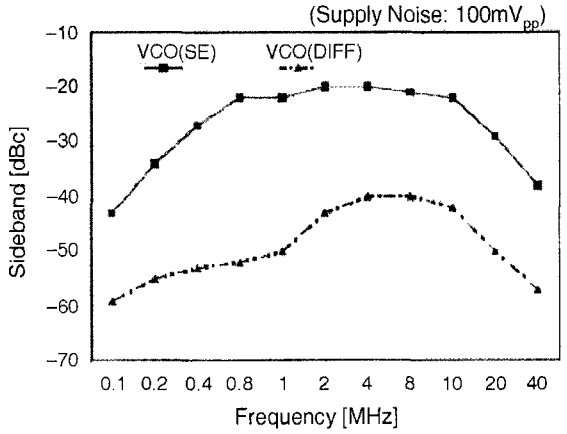


Fig. 19. Measured supply noise sensitivity comparison: single-ended VCO vs. differentially-controlled VCO.

Table 2. Summary of measured performance.

Technology	90nm CMOS
Supply voltage	1.2V
Power consumption	20mW
Frequency range	4.75 – 6.1GHz
Bandwidth	8 – 12MHz
Phase noise @1MHz	−108dBc/Hz
Spurious tones	< −56dBc/Hz
Random jitter*	0.34 – 0.48ps_{rms}
Area**	0.52 x 0.68mm^2

*Noise integration bandwidth: 3MHz to 1GHz

**Including supply voltage regulator and bandgap

on-chip regulator which provides about 20-dB power supply rejection, actual supply noise amplitude for the internal PLL supply can be estimated at 10 mV_{pp}. Fig. 19 shows the measured supply noise sensitivity which is represented by sideband magnitudes. Noise suppression within PLL bandwidth is observed in the plot, indicating that overall DJ performance is dominated by the VCO-induced noise. Fig. 19 also shows the performance comparison with the PLL having the single-ended varactor and the single-ended output linear amplifier. The measured results clearly show that the differentially controlled VCO offers superior power supply rejection.

A summary of the measured results is given in Table 2.

VI. CONCLUSIONS

The PLL using a single-input dual-path VCO with uniform bandwidth control is implemented in 90-nm CMOS. The prototype 5GHz continuously tunable PLL exhibits RJ variation of 0.34 to 0.48 ps-rms and bandwidth variation of just 8-12 MHz over process and temperature. These results demonstrate that the proposed PLL is a promising approach for the common clock serial link applications which require specific jitter transfer characteristics. This work also addresses noise and coupling issues in dual-path VCO design. It is shown that using the differential control scheme is important in dual-path VCO design to achieve good DJ performance.

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REFERENCES

[1] *PCI Express Base Specification 2.0, Revision 0.7*, PCI-SIG, 2005.

[2] M. Li, A. Martwick, G. Talbot, and J. Wilstrup, "Transfer functions for the reference clock jitter in a serial link: Theory and applications," in *Proc. International Test Conference (ITC)*, pp.1158-1167, Oct. 2004.

[3] S. Sidiropoulous and M. Horowitz, "A semidigital dual delay-locked loop," *IEEE J. of Solid-State Circuits*, Vol.32, pp.1683-1692, Nov. 1997.

[4] T.-H. Lin and W. Kaiser, "A 900-MHz 2.5-mA CMOS frequency synthesizer with an automatic SC tuning loop," *IEEE Journal of Solid-State Circuits*, Vol.36, pp.424-431, Mar. 2001.

[5] W. Wilson, U.-K. Moon, K. Lakshmikumar, and L. Dai, "A CMOS self-calibrating frequency synthesizer," *IEEE Journal of Solid-State Circuits*, Vol.35, pp. 1436-1444, Oct. 2000.

[6] A. Loke, et al., "A versatile 90-nm CMOS charge-pump PLL for SerDes transmitter clocking," *IEEE J. of Solid-State Circuits*, Vol.41, pp.1894-1907, Aug. 2006.

[7] Y. Moon, Y. Park, N. Kim, G. Ahn, H. Shin, and D.-K. Jeong, "A quad 0.6-3.2Gb/s/channel interference-free CMOS transceiver for backplane serial link," *IEEE Journal of Solid-State Circuits*, Vol.39, pp.795-803, May 2004.

[8] S. Williams, H. Thompson, M. Hufford, and E. Naviasky, "An improved CMOS ring oscillator PLL with less than 4ps RMS accumulated jitter" in *Proc. IEEE CICC*, pp.151-154, Sept. 2004.

[9] S. Gierkink, D. Li, R. Frye, and V. Boccuzzi, "A 3.5 GHz integer-N PLL with dual on-chip loop filters and VCO tune ports for fast low-IF/zero-IF LO switching in an 802.11 transceiver," in *Proc. IEEE CICC*, pp. 629-632, Sept. 2004.

[10] F. Herzel, G. Fischer, and H. Gustat, "An integrated CMOS RF synthesizer for 802.11a wireless LAN," *IEEE J. of Solid-State Circuits*, Vol.38, pp. 1767-1770, Oct. 2003.

[11] H. Noguchi, T. Tateyama, M. Okamoto, H. Uchida, M. Kimuar, and K. Takashi, "A 9.9G-10.8 Gb/s rate-adaptive clock and data recovery with no external reference clock for WDM optical fiber transmission," in *IEEE ISSCC Dig. Tech. Papers*, pp.252-253, Feb. 2002.

[12] Y. Koo, et al., "A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems," *IEEE Journal of Solid-State Circuits*, Vol.37, pp.536-542, May 2002.

[13] R. Nonis, N. Da Dalt, P. Palestri, and L. Selmi, "Modeling, design, and characterization of a new low jitter analog dual tuning LC-VCO PLL architecture," *IEEE Journal of Solid-State Circuits*, Vol.40, pp.1303-1309, June 2005.

[14] M. Perrott, *CppSim behavioral simulator*, http://www-mtl.mit.edu/researchgroups/perrottgroup/tools.html.

[15] B. Soltanian, H. Ainspan, W. Rhee, D. Friedman, and P. Kinget, "An ultra compact differentially tuned 6 GHz CMOS LC VCO with dynamic common-mode feedback," in *Proc. IEEE CICC*, pp.671-674, Sept. 2006.

[16] W. Rhee et al., "A 10-Gb/s CMOS clock and data recovery circuit using a secondary delay-locked loop," in *Proc. Custom Integrated Circuits Conf.*, pp.81-84, Sept. 2003.

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