A Combined Clock and Data Recovery Circuit with Adaptive Cancellation of Data-Dependent Jitter

Jin-Hee Lee*, Suhwan Kim, and Deog-Kyoon Jeong****

***Abstract*—A combined clock and data recovery (CDR) circuit with adaptive cancellation of data-dependent jitter (DDJ) is constructed in all-digital architecture which is amenable to deep submicron technology. The DDJ canceller uses an adaptive FIR filter to compen-sate for any unknown channel characteristic. The proposed CDR decreases jitter in the recovered clock since the DDJ canceller significantly cancels out incoming jitter caused by inter-symbol interference.**

***Index Terms*—Data-dependent jitter, adaptive DDJ canceller, CDR**

I. INTRODUCTION

Recent increase in data rates of serial link transceivers over band-limited channels required rigorous studies into the effect of jitter in clock and data recovery (CDR) circuits for accurate recovery of transmitted sequence. Traditionally, channel equalization has been widely used to enlarge the data eye at the receiver front-end, such as continuous-time equalization [1], decision feedback equalization (DFE) [2-3], or feed-forward equalization [3-4]. However, since a channel equalizer expands the height of the data eye rather than widening the timing opening, significant timing jitter still persists after equalization. New methods aimed at improving the link performance in the presence of data-dependent jitter (DDJ) caused by inter-symbol interference (ISI) have been introduced recently [5-6] and they attempt to reduce jitter by edge equalization.

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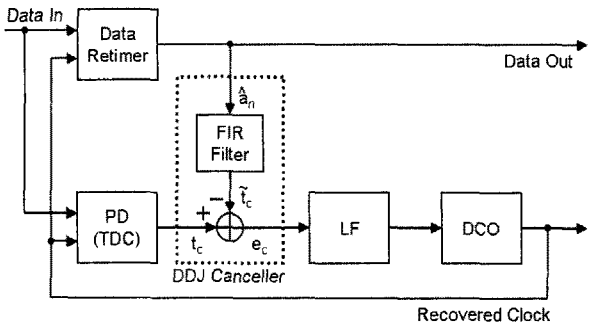

Fig. 1. Block diagram of combined CDR with DDJ canceller.

Although CDRs with edge equalizers show improved performance, they have a constrained adaptation policy [5] or cannot adapt to an unknown channel [6]. We propose a combined CDR with an adaptive DDJ canceller inside the loop as shown in Fig. 1, which provides coefficient adaptation to an unknown channel characteristic. Unlike the feedback architecture of edge equalization [6], this work incorporates a feed-forward architecture in a DDJ cancellation path. The feed-forward architecture brings DDJ cancellation to the discrete-time domain and relaxes the timing requirement for DDJ estimation. Therefore, a conventional digital FIR filter can be used for the DDJ canceller and a conventional time-to-digital converter (TDC) for the phase detector (PD). These basic building blocks of the proposed CDR can be readily realized as high-speed digital circuits. The digital implementation of the proposed CDR with synthesizable circuits is amenable to deep submicron technology.

II. CANCELLATION OF DATA-DEPENDENT JITTER

Timing jitter consists of random jitter (RJ) and deterministic jitter (DJ). DJ can be further classified into three sub-categories: bounded uncorrelated jitter (BUJ), data-dependent jitter (DDJ), and periodic jitter (PJ) [7]. DDJ

originates from the ISI of a channel. In other words, the preceding data sequence influences the crossing time of the current transition edge.

For example, when a random data sequence is transmitted over a first-order channel, the crossing time t_c of the received signal can be represented by the time constant τ of the channel [8]. For a rising edge with a_{-1}=0 and a_0=1, the half-level crossing time becomes

$$t_{c,rise} = \tau \ln\left[2 - 2\sum_{n=-\infty}^{-2} a_n\left(\alpha^{-n-1} - \alpha^{-n}\right)\right] = \tau \ln 2 + \tau \ln\left[1 - (1-\alpha)\sum_{n=-\infty}^{-2} a_n \alpha^{-n-1}\right] \quad (1)$$

where T is the unit interval of a symbol, α is defined as $e^{-T/\tau}$, and a_n is the symbol that is transmitted -n cycles earlier than the current one. To remove the logarithm in the second term, we need to find the linear approximation to the second term. Let ε be a positive number less than 1/2. When x varies between 0 and ε, the function ln(1-x) can be approximated by a straight line fitting as follows:

$$\ln(1-x) \cong \frac{\ln(1-\varepsilon)}{\varepsilon} x, \quad (0 \le x \le \varepsilon). \quad (2)$$

Since $0 < \alpha < 1/2$ in practical cases with an open eye diagram of a received signal, the accumulative term inside the second logarithmic term in (1) has the maximum of α with all-one sequence before a_{-1} and the minimum of 0 with all-zero sequence. Thus,

$$0 \le (1-\alpha)\sum_{n=-\infty}^{-2} a_n \alpha^{-n-1} \le \alpha. \quad (3)$$

Using (2) and (3), the crossing time in (1) can be expressed by the following linear function:

$$t_{c,rise} \cong \tau \ln 2 + \tau \frac{\ln(1-\alpha)}{\alpha}(1-\alpha)\sum_{n=-\infty}^{-2} a_n \alpha^{-n-1} = t_{c0} + \sum_{n=-\infty}^{-2} t_c^{(n)} a_n \quad (4)$$

where t_{c0} is the ideal crossing time without DDJ, and $t_c^{(n)}$ represents the amount of crossing time deviation caused by a_n. The linear relationship between the trans-mitted sequence a_n and the crossing time t_c makes it possible to estimate DDJ using an FIR filter, as illust-rated in Fig. 1. Thus, the estimated DDJ is expressed by the linear function [6]

$$\tilde{t}_c = \sum_{n=-N-1}^{-2} w_n \hat{a}_n \quad (5)$$

where N is the number of taps employed in the DDJ canceller, w_n are the tap coefficients, and $\hat{a}_n$ are the estimated symbols. As an LMS algorithm is used to adapt the DDJ canceller to the input jitter characteristics, the tap coefficient w_n approaches the n-th amount of crossing time error $t_c^{(n)}$ as follows:

$$w_n \cong t_c^{(n)} = \tau(1-\alpha)\alpha^{-n-2}\ln(1-\alpha). \quad (6)$$

This equation is examined by the simulation with a first-order channel with α of 0.44 and a 16-tap adaptive DDJ canceller. Calculated and simulated coefficients are plotted in Fig. 2. Almost identical coefficients suggest that the proposed DDJ canceller can be adapted by an LMS algorithm to any channel characteristics approximated as the first order. The mean-squared error (MSE) criterion of the LMS algorithm operates reliably in the presence of other jitter sources such as RJ and PJ, which are introduced by the transmitter, channel, sampler, and the digitally controlled oscillator (DCO). In this work, a signed LMS algorithm is employed to reduce the hardware complexity of the coefficient update circuit.

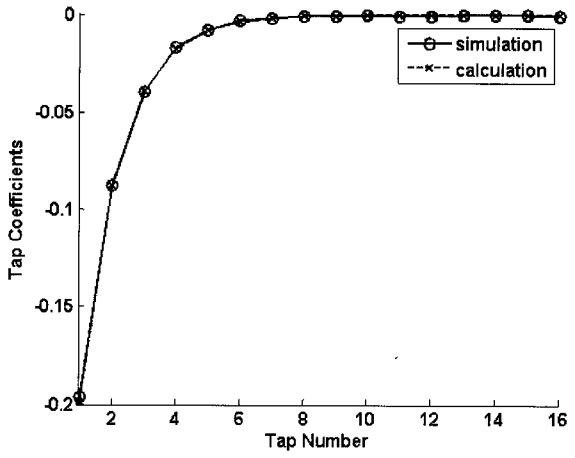

Fig. 2. Comparison of calculated coefficients with a linear approximation and LMS adaption, for a first-order channel.

III. A COMBINED CDR CIRCUIT

Since DDJ is almost linearly dependent on the data sequence as explained above, an FIR filter, as shown in Fig. 1, can be employed for DDJ cancellation. Although the previous work also adopts the FIR filter for DDJ equalization, the DDJ equalizer consists of an analog FIR filter and a precise edge shifter [6]. The most serious drawback of the previous work is lack of coefficient adaptation policy. Ad hoc adjustment cannot be applied to an equalizer for an unknown channel. Besides, the DDJ equalizer is separated from the CDR circuit. The DDJ equalizer provides clean edges to the CDR and the CDR provides the recovered clock to the DDJ equalizer. The separated DDJ equalizer requires the feedback structure for DDJ equalization.

Instead of an edge shifter and an analog FIR filter, the proposed DDJ canceller utilizes a TDC and a digital FIR filter. Since the DDJ canceller is integrated into the all-digital CDR, an LMS algorithm can be easily implemented using the DDJ cancelled error signal in a digital value. The coefficient adaptation enables the proposed DDJ canceller to be used for any unknown channel.

Fig. 3 describes the detailed structure of the DDJ canceller [9]. The input to the FIR filter is a retimed symbol ân and the output is an estimated DDJ. When the estimated DDJ is subtracted from the detected phase error, a DDJ-free phase information ec is obtained and utilized in the proposed CDR loop. Therefore, the combined CDR with DDJ canceller can recover clock with less jitter, offering a lower bit error rate for an ISI-corrupted incoming data stream.

Unlike a conventional FIR filter, the DDJ canceller shown in Fig. 3 operates only when there is a data transition. The estimated symbol ân and the previously detected symbol $\hat{a}_{n-1}$ with opposite polarity indicate the transition in the received sequence. Besides, the present estimated symbol ân, indicating the direction of the edge, simply inverts the stored symbols using XOR gates to reduce the required hardware by half. Since the phase shift of the rising edge caused by the preceding data pattern is equal to that of the falling edge by the preceding data pattern with the opposite polarity, inverting symbols in the delay line eliminates the identical FIR filter for the alternative edge. Thus, the output is an estimated DDJ for both rising and falling edges.

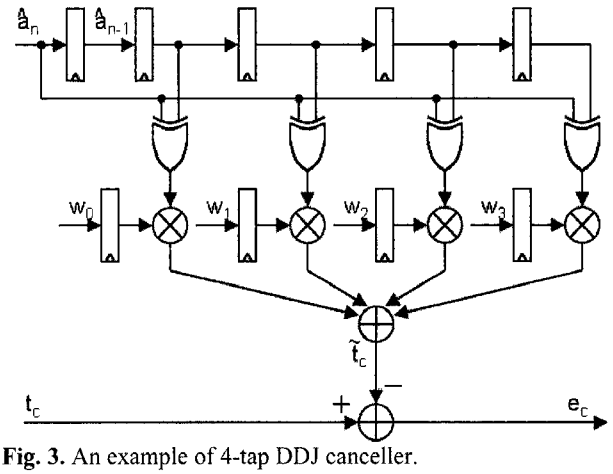

Fig. 3. An example of 4-tap DDJ canceller.

Since a conventional LMS algorithm increases the hardware usage, a signed LMS algorithm is adopted to adjust tap coefficients as follows:

$$w_{k,n+1} = w_{k,n} + \mu \cdot \mathrm{sgn}(e_{c,n}) \cdot (\hat{a}_n \oplus \hat{a}_{n-k-2}), \qquad (7)$$

where $w_{k,n}$ is the k-th tap coefficient at the current time instant n and μ is the gain constant for adaptation. The sign function on the error e_c removes a multiplier in the coefficient update circuit because the result of the binary XOR operation is already one bit. Hence, only a shifter and an adder are used for the update circuit.

In contrast to an analog implementation, a fully digital implementation of an FIR filter is suitable for logic synthesis using EDA tools. To increase the throughput of the digital filter, which restricts the operating speed of the entire CDR, parallel signal processing can be utilized [10]. Speed limitations can be overcome by interleaving a few small FIR filters.

The PD is implemented with a conventional TDC as shown in Fig. 4. The TDC estimates a phase error t_c in a discrete value which represents an edge position in the detection range. When the edge is placed in the middle of detection range, the TDC translates the phase error to zero. The early and late edges have positive and negative values, respectively.

The loop filter (LF) consists of proportional and integral paths [11]. The integral path tracks frequency information by accumulating phase information and the proportional path keeps track of phase errors for loop stability. The transfer function of the loop filter is

$$H_{LF}(z) = K_P + \frac{K_I}{1 - z^{-1}}, \qquad (8)$$

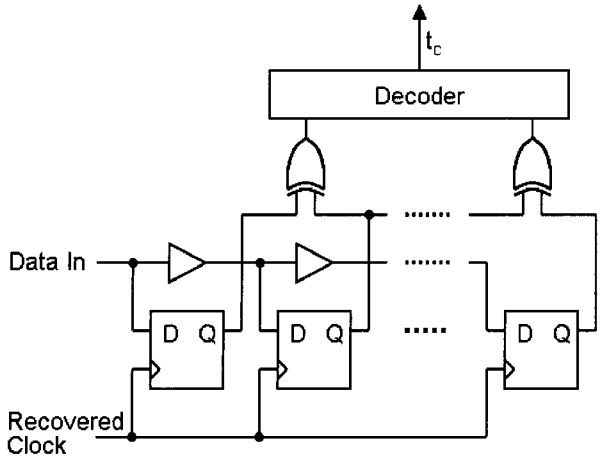

Fig. 4. Circuit diagram of the TDC.

where K_P and K_I are the proportional and integral gains, respectively.

As illustrated in Fig. 1, the phase error is filtered by the DDJ canceller and the cleaned-up timing information is averaged in the loop filter to steer the DCO. Then, the recovered clock generated by the DCO is fed back to sample the input signal in the TDC and the data re-timer. Since the rising edge of the recovered clock is aligned with the edge of the data eye, the re-timer must use the falling edge to sample the data in the middle of a data eye. In contrast to a conventional CDR, the proposed circuit incorporates the DDJ canceller inside the loop to reduce ISI-corrupted jitter and all of the functions are operated in digital domain. Thus, basic building blocks in the proposed CDR could be implemented in high-speed digital circuits, which enable fast migrations of all-digital architectures.

Since the DDJ canceller only reduces the phase error as shown in Fig. 5, the same analysis method of a charge-pump phase-locked loop (PLL) can also be applied to the proposed CDR. For a given bandwidth and phase margin, gains for the loop filter can be obtained from the parameters of the equivalent charge-pump PLL using a bilinear z-transform [11]. However, delays incurred in digital circuits should be considered in the analysis. The added loop latency aggravates the phase margin of the proposed CDR.

Considering the loop latency, two loop filter gains are expressed as

$$K_P = \frac{T^2 \Delta t_{TDC}}{\Delta t_{DCO}} \frac{\omega_{UGBW}^{\ 2}}{\sqrt{\omega_{UGBW}^{\ 2} + \omega_Z^{\ 2}}} \left[\frac{1}{T} - \frac{\omega_{UGBW}}{2 \cdot \tan(\mathrm{PM}')} \right]$$
$$K_I = \frac{T^2 \Delta t_{TDC}}{\Delta t_{DCO} \cdot \tan(\mathrm{PM}')} \frac{\omega_{UGBW}^{\ 3}}{\sqrt{\omega_{UGBW}^{\ 2} + \omega_Z^{\ 2}}} \quad (9)$$

where T is the clock period and Δt_{DCO} and Δt_{TDC} are the resolutions of the DCO and the TDC, respectively. PM′, ω_{UGBW}, and ω_Z are the phase margin with zero latency, the targeted unit gain bandwidth, and the zero frequency of the CDR, respectively. The zero frequency is calculated as

$$\omega_Z = \frac{\omega_{UGBW}}{\tan(\mathrm{PM}')}, \quad (10)$$

Since PM′ is the ideal phase margin of the CDR without loop latency, it is calculated from the desired, actual phase margin PM as follows:

$$\mathrm{PM}' = \mathrm{PM} + n_d T \omega_{UGBW}, \quad (11)$$

where n_d is the loop latency of the proposed CDR denoted by the number of cycles in discrete-time domain. Although the additional delay caused by the DDJ canceller degrades stability, the proposed CDR shows better overall performance thanks to the more dominant effect of reduced input jitter against the slower response to the phase error.

Timing recovery and adaptive filtering occur at the same time in the proposed CDR. Therefore, the two loop dynamics may interact while in operation. However, goals of the CDR loop and the LMS adaptation in the DDJ canceller are the same. An LMS algorithm minimizes the mean squared error which is the DDJ-cancelled phase error e_c and the CDR loop also reduces the average phase error. To prevent possible detrimental interaction leading to instability, the adaptation loop runs significantly slower than the CDR loop. The time constant of the coefficient adaptation, which is inversely proportional to the gain constant μ [12], can be controlled to several hundreds greater than that of the CDR loop. The bandwidth separation enables each loop to converge in an orderly fashion: the CDR loop converges first and then the coefficient update loop.

IV. Simulation Results

To demonstrate the operation of the proposed CDR, simulations are performed with a 20-m RG-58 cable model and 0.13-μm CMOS library. A 2^{23}-1 pseudo-random bit sequence (PRBS) is used as data sequence

and transmitted at a rate of 2.5 Gb/s. An eye diagram of the transmitted signal at the end of the cable and the statistical probability density function (pdf) of the DDJ are plotted in Fig. 5. Only 0.28 UI of the data eye is open due to severe ISI. Random jitter of 0.01 UI_{rms} is injected into the output of the transmitter and the DCO in the receiver. The resolution of the DCO is initially set to 0.005 UI. A typical resolution of 0.1 UI is used for the TDC and the differential nonlinearity (DNL) of the TDC is included as ±0.25 LSB while the TDC covers the detection range of 0.9 UI. The loop latency of the whole CDR loop is assumed as three cycles.

As shown in Fig. 5, the pdf of the cleaned-up edge position is changed according to the number of taps employed in the DDJ canceller. More taps engaged in the DDJ canceller move more edges to the center. Hence, the residual jitter is decreased. Since the DDJ canceller produces fractional numbers, the pdf of the DDJ cancelled edges shows no noticeable quantization although the TDC outputs extremely quantized numbers.

Fig. 6 shows the relation between the amount of residual jitter after DDJ cancellation and the number of taps employed in the DDJ canceller as well as the resolution of the TDC. The residual jitter is significantly reduced as the number of taps is increased. Using the TDC with 0.1-UI resolution, the amount of residual rms jitter is reduced from 0.159 UI_{rms} with no DDJ canceller to 0.067 UI_{rms} with a 4-tap filter. While the precision of the TDC also influences the performance of the DDJ canceller, as shown in Fig. 6, the residual jitter is increased only modestly as the resolution drops from 0.047 UI to 0.18 UI for all the number of taps considered. However, the impact on hardware complexity is significant. As we decrease the resolution of the TDC from 0.047 UI, 0.1 UI, 0.18 UI, to 0.3 UI, the number of DFFs used in the TDC is signifycantly decreased from 20, 10, 6, to 4, respectively. Moreover, a fine-resolution TDC raises many issues on implementation, such as uneven rising and falling transition time and unbalanced route [13].

In contrast to the feedback architecture [6], the input signal to the TDC in the feed-forward architecture includes a large amount of jitter since the actual edge is not shifted. Although the DDJ canceller eliminates input jitter significantly, the amount of residual jitter cannot be lower than the bound set by the quantization error introduced by the TDC. For example, if the TDC resolution is 0.1 UI, its quantization error is equivalent to 0.029 UI_{rms}. Thus, the residual jitter cannot go below 0.029 UI_{rms}. However, the negative effect of the limited TDC resolution is

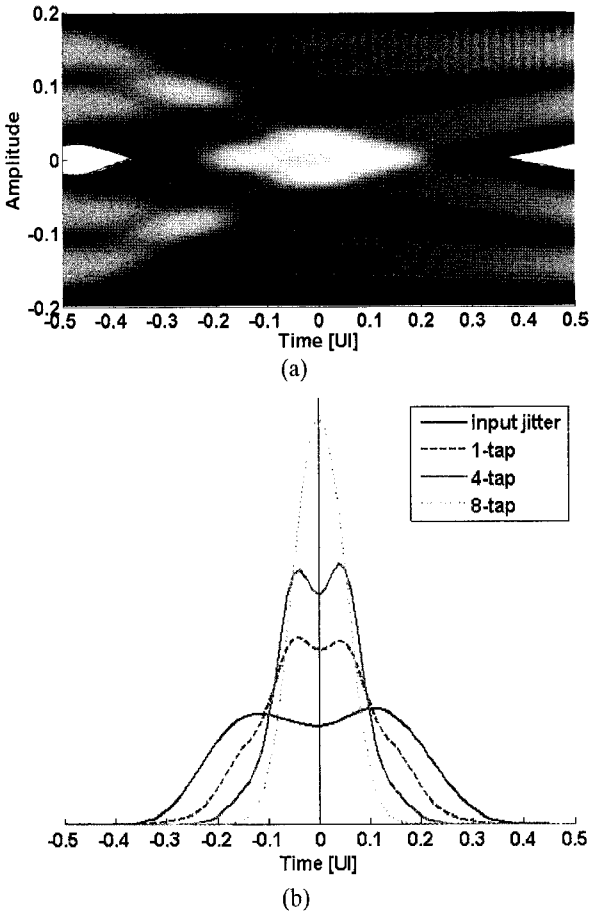

Fig. 5. (a) Simulated eye diagram of a signal over a 20m RG-58 cable model at a data-rate of 2.5 Gb/s. (b) Statistical pdfs of input jitter and DDJ cancelled phase errors with increasing numbers of taps.

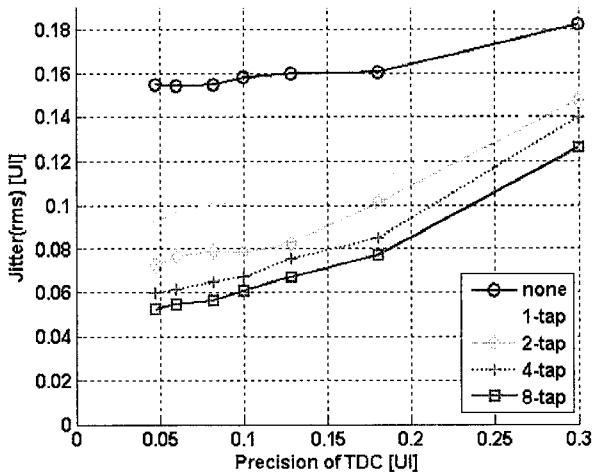

Fig. 6. Amount of residual input jitter vs. resolution of TDC, with DCO resolution of 0.005 UI, for a random jitter of 0.01 UI_{rms} injected at the transmitter and DCO.

significantly reduced since the random jitter in the DDJ canceller output is later filtered by the digital loop filter.

Fig. 7 shows the simulation results of the entire CDR loop with the 4-tap DDJ canceller with 0.1-UI TDC resolution under the previously stated condition. The loop filter gains, 3.0 for K_P and 0.063 for K_I, are chosen for a loop bandwidth of 25 MHz and a phase margin of 60°. To prevent detrimental interaction between the CDR loop and the coefficient adaptation loop, the coefficient update loop runs significantly slower than the CDR loop. Coefficient update loop time constant is about 1500 UIs when μ is 0.00005. Fig. 7 shows the convergence behavior of the proposed CDR, starting from the initial state. Note that the tap coefficients begin to change after the convergence of the CDR loop (CDR lock) at 400 UIs. Before the CDR lock, tap coefficients drift but remain close to zero. By 4400 UIs, the tap coefficients converge to their expected values of the estimated channel response (coefficient lock). Although the CDR loop and the coefficient update of the DDJ canceller may interact to disturb the convergence of each loop, large difference between time constants of the CDR loop and the coefficient adaptation guarantees the robust operation of the proposed CDR. As the tap coefficients converge, the rms jitter of the recovered clock is reduced from 0.061 UI_{rms} to 0.033 UI_{rms}.

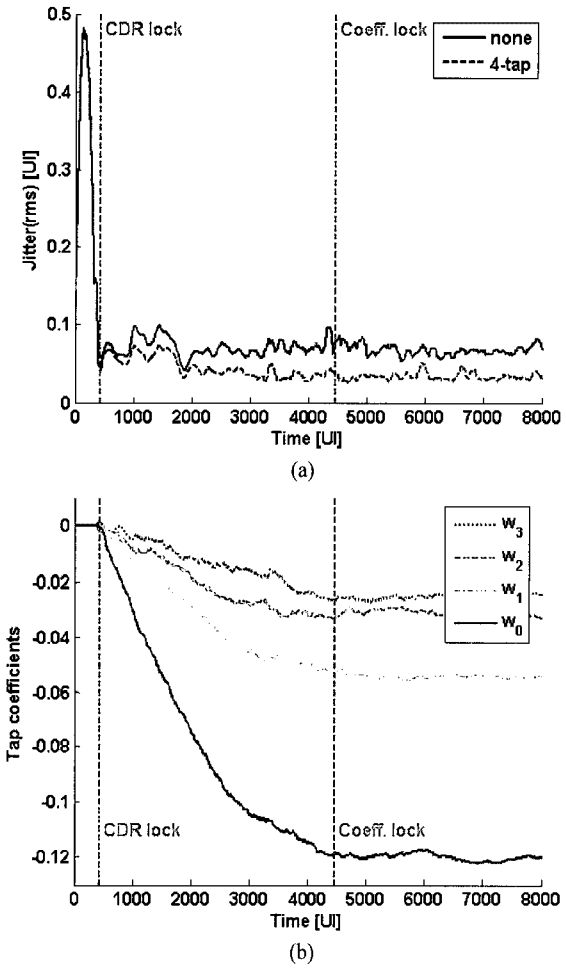

Fig. 7. Convergence behavior of conventional and proposed CDRs: (a) rms jitter of the recovered clock and (b) tap coefficients in the DDJ canceller.

V. CONCLUSIONS

An all-digital CDR circuit with adaptive cancellation of DDJ for unknown channel characteristics has been proposed and simulated with various architectural parameters. The DDJ canceller is integrated into the CDR loop with the feed-forward architecture. Thus, all building blocks except for the DCO can be implemented in synthesizable digital circuits. In addition, it relaxes the timing constraints on the digital circuits and mitigates the required resolution of the TDC. The proposed CDR is more amenable to implementation in deep submicron technology than the conventional CDR. Simulation results of the combined CDR with a 4-tap DDJ canceller and a TDC with a 0.1-UI resolution using a 20-m RG-58 cable model at the data rate of 2.5 Gb/s show that the rms jitter of the recovered clock is reduced from 0.061 UI_{rms}, for the conventional CDR, to 0.033 UI_{rms} while the rms jitter at the output of the DDJ canceller is decreased from 0.159 UI_{rms} to 0.067 UI_{rms}.

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REFERENCES

[1] J.-S. Choi, M.-S. Hwang, and D.-K. Jeong, "A 0.18-μm CMOS 3.5-Gb/s continuous-time adaptive cable equalizer using enhanced low-frequency gain control method," *IEEE J. Solid-State Circuits*, Vol.39, pp. 419-425, Mar. 2004.

[2] V. Stojanovic, et al., "Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery," *IEEE J. Solid-State Circuits*, Vol.40, pp.1012-1026, Apr. 2005.

[3] M. Sorna, et al., "A 6.4 Gb/s CMOS SerDes core with feed-forward and decision-feedback equalization," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2005, pp.62-63.

[4] J. Kim, J. Yang, S. Byun, H. Jun, J. Park, C. Conroy, and B. Kim, "A four-channel 3.125-Gb/s/ch CMOS serial-link transceiver with a mixed-mode adaptive equalizer," *IEEE J. Solid-State Circuits*, Vol.40, pp.462-471, Feb. 2005.

[5] K.-L. J. Wong, E-H. Chen, and C.-K. Ken Yang, "Modified LMS adaptation algorithm for a discrete-time edge equalizer of serial I/O," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2006, pp.387-390.

[6] J. F. Buckwalter and A. Hajimiri, "Analysis and equalization of data-dependent jitter," *IEEE J. Solid-State Circuits*, Vol.41, No.3, pp.607-620, Mar. 2006.

[7] A. Kuo, T. Farahmand, N. Ou, S. Tabatabaei, and A. Ivanov, "Jitter models and measurement methods for high-speed serial interconnects," in *Proc. IEEE Int. Test Conf.*, 2004, pp.1295-1302.

[8] J. F. Buckwalter, B. Analui, and A. Hajimiri, "Predicting data-dependent jitter," *IEEE Trans. Circuits and Systems II: Express Briefs*, Vol.51, pp.453-457, Sep. 2004.

[9] J. F. Buckwalter, M. Meghelli, D. J. Friedman, and A. Hajimiri, "Phase and amplitude pre-emphasis techniques for low power serial links," *IEEE J. Solid-State Circuits*, Vol.41, No.6, pp.1391-1399, June 2006.

[10] D. A. Parker and K. K. Parhi, "Area-efficient parallel FIR digital filter implementations," in *Proc. IEEE Int. Application Specific Systems, Architectures and Processors*, 1996, pp.93-111.

[11] V. Kratyuk, P. K. Hanumolu, U.-K. Moon, and K. Mayaram, "A design procedure for all-digital phase-locked loops based on a charge-pump phase-locked-loop analogy," *IEEE Trans. Circuits and Systems II: Express Briefs*, Vol.54, pp.159-163, Mar. 2007.

[12] B. Widrow and S. D. Stearns, *Adaptive signal processing*, Prentice Hall, 1985.

[13] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara, "1.3V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *IEEE Trans. Circuits and Systems II: Express Briefs*, Vol.53, pp.220-224, Mar. 2006.

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