A Multiphase Compensation Method with Dynamic Element Matching Technique in Σ-Δ Fractional-*N* Frequency Synthesizers

Zuow-Zun Chen and Tai-Cheng Lee

***Abstract*—A multiphase compensation method with mismatch linearization technique, is presented and demonstrated in a Σ-Δ fractional-N frequency synthesizer. An on-chip delay-locked loop (DLL) and a proposed delay line structure are constructed to provide multiphase compensation on Σ-Δ quantizetion noise. In the delay line structure, dynamic element matching (DEM) techniques are employed for mismatch linearization. The proposed Σ-Δ fractional-N frequency synthesizer is fabricated in a 0.18-μm CMOS technology with 2.14-GHz output frequency and 4-Hz resolution. The die size is 0.92 mm × 1.15 mm, and it consumes 27.2 mW. In-band phase noise of -82 dBc/Hz at 10 kHz offset and out-of-band phase noise of -103 dBc/Hz at 1 MHz offset are measured with a loop bandwidth of 200 kHz. The settling time is shorter than 25 μs.**

***Index Terms*—CMOS RF, delta-sigma modulator, frac-tional-*N* frequency synthesizers, phase-locked-loop (PLL), frequency dividers, phase noise, quantization noise suppression, WCDMA**

I. INTRODUCTION

PLL-based frequency synthesizers are widely used in communication systems. Fractional-*N* frequency synthesizers are used rather than integer-*N* frequency synthesizers because of the relaxed tradeoffs between frequency resolution and loop bandwidth. In high-frequency resolution applications, integer-*N* frequency synthesizers lack for large loop bandwidth which limits the settling speed and in-band VCO phase noise performance. On the contrary, fractional-*N* frequency synthesizers are able to resolve these problems, by allowing fractional divisions, high-frequency reference clock and high resolution. Therefore, larger loop bandwidth frequency synthesizers can be employed.

Fig. 1 shows the diagram of a conventional Σ-Δ fractional-*N* frequency synthesizer [1-3]. The fractional division is often based on a Σ-Δ modulator and multi-modulus dividers. The Σ-Δ modulator produces a sequence of integer numbers whose mean is equal to the fractional number. The sequential integer numbers control the division of the divider so that the desired fractional ratio is obtained. The deviation between the integer number and the fractional number is called quantization noise which has a high-pass feature in frequency domain [4], and often dominates at high offset frequencies. By reducing the loop bandwidth, high-pass quantization noise can be suppressed, but this conflicts the advantage in using fractional-*N* synthesizers, which is to increase loop bandwidth. There are several methods to compensate the quantization noise, such methods include DAC compen-

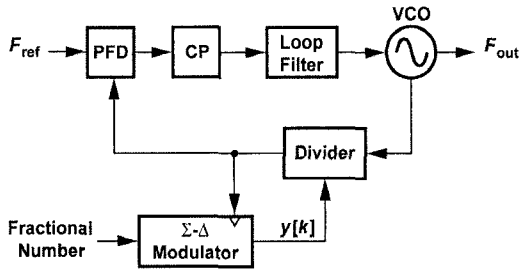

Fig. 1. A conventional Σ-Δ fractional-N frequency synthesizer.

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sation [5,6], multiphase compensation [7-9], PFD/DAC compensation [10], and compensation based on 1/1.5 dividers [11].

Most of the reported multiphase compensation methods are based on ring VCO [7,8] or delay-locked loop [12] and a Σ-Δ modulator or counter. The main purpose of these designs is to reduce the quantization noise by generating multiphase fractional divisions. However, nonideal effect such as multiphase mismatch or gain error causes serious problems like in-band noise and spurious tones.

In this work, to suppress the quantization noise, a multiphase compensation method based on delay-locked loop and a proposed delay line structure are implemented for the advance of no pulse amplitude problem that occurs in DAC compensation methods [5,6,10]. In the proposed delay line structure, dynamic element matching techniques [13,14] are introduced to improve frequency synthesizer phase noise due to the timing mismatch in the delay line units. A 200-kHz bandwidth Σ-Δ fractional-*N* frequency synthesizer operating at the frequency of 2.14 GHz with a 35-MHz input reference clock is built for demonstration.

This paper is organized as follows. Section II presents the system architecture of a multiphase compensation Σ-Δ fractional-*N* frequency synthesizer. Details of circuit implementations are described in Section III. The experimental results are given in Section IV, and in Section V, we conclude the remarks.

II. SYSTEM ARCHITECTURE

Fig. 2 depicts the architecture of the proposed Σ-Δ fractional-*N* frequency synthesizer. The delay-locked loop and delay line 1 are employed for multiphase compensation that suppresses the quantization noise. Rather than generating all the multiphase signals in advance [7-9], the proposed delay line 1 structure generates specific phased signal only when it is needed.

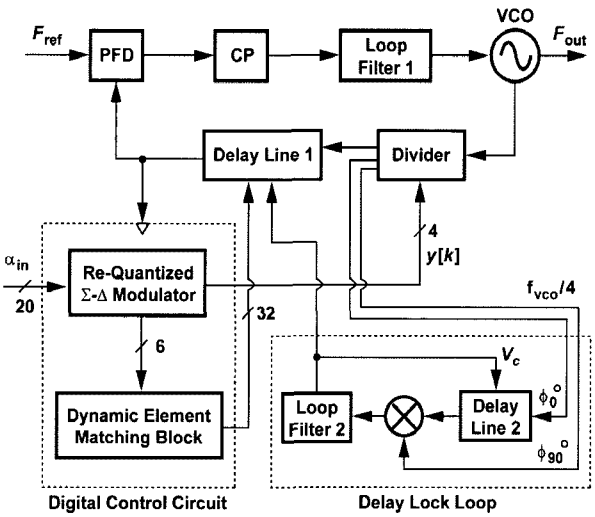


Fig. 2. Proposed frequency synthesizer architecture.

The digital control circuit contains two main building blocks. The first one is a re-quantized Σ-Δ modulator [6], which contains two Σ-Δ modulators and is employed to resolve the nonideal effect of delay time gain error in delay units and simultaneously generates the specific fractional division. The second one is the dynamic element matching block, which contains DEM algorithms for mismatch linearization. Details of the proposed frequency synthesizer will be discussed in the followings.

1. Delay-Locked Loop and Delay Lines

The proposed fractional-*N* frequency synthesizer employs a third-order Σ-Δ modulator. Therefore, second-order quantization noise will be induced to the frequency synthesizer through the operation of divider [15]. In order to extend the loop bandwidth to 200-kHz, a reduction of 18 dB in quantization noise will be required to attain the same noise level as a 70-kHz bandwidth frequency synthesizer at 10-MHz frequency offset [6]. In multiphase compensation frequency synthesizers, to reduce the quantization noise of 18 dB, a least delay time of $T_{vco}/8$ is required. Some methods such like ring VCO [7,8] or delay-locked loop [12] has been employed to realize this small delay interval. In this work, a delay-locked loop is employed to generate the $T_{vco}/8$ delay time.

Shown in Fig. 3 is the proposed delay-locked loop. The high-frequency signal of VCO output is first divided by four to achieve the two quadrature signals ϕ_0° and ϕ_{90}°, which has 90-degree phase difference. With quarter-rate operation frequency, the power consumption of the delay-locked loop could be highly reduced. The ϕ_0° signal then enters the delay line 2 and compares its phase with ϕ_{90}° at the phase frequency detector. The purpose of the 90-degree phase difference is to reduce the needed numbers of delay units. For example, if the two input signals of delay-locked loop are in-phased, 32 delay units are needed to maintain a delay time of $T_{vco}/8$ in each delay units. However, only 8 delay units are required for a pair of 90-degree phase difference input signals.

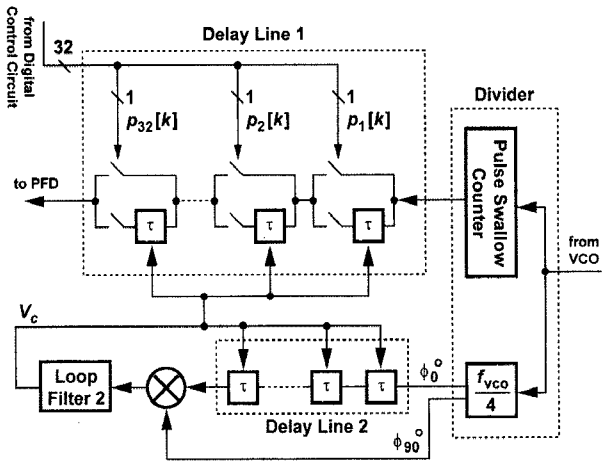


Fig. 3. Proposed delay-locked loop structure.

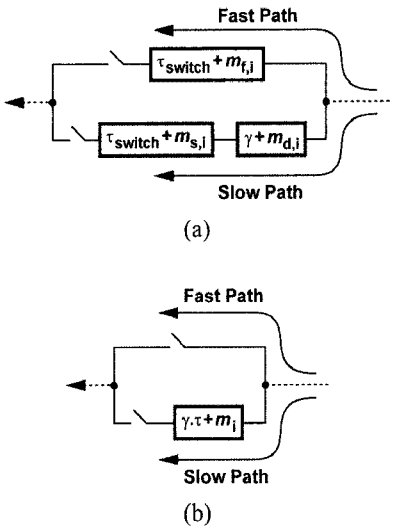


Fig. 4. Nonideal model of subcircuits in delay line 1. (a) Mismatch in slow path and fast path. (b) Mismatch considered only in delay unit.

While the delay-locked loop is under locked condition, each delay unit in delay line 2 has a delay time τ equal to $T_{vco}/8$. With replica delay units, this delay time is mapped to the delay units in delay line 1 by voltage control signal V_c. The structure of delay line 1 is depicted in Fig. 3. Delay line 1 can be divided into 32 subcircuits, where each of them contains two switches and a delay unit. Shown in Fig. 3, input signals passes through each subcircuit either by the fast path or slow path controlled by the signal $p_i[k]$. If $p_i[k]$ equals to 1, the input signal passes the i^{th} subcircuit through slow path. On the other hand, if $p_i[k]$ equals 0, the input signal passes the i^{th} subcircuit through fast path. Thus the multiphase signals can be generated through this topology specifically by the control signals $p_i[k]$ that is produced from digital control circuit.

Ideally, the delay time of a subcircuit will increase with an additional time τ while switching from fast path to slow path. However, nonideal effect such as mismatches and propagation delays in switches or delay units should be considered. Fig. 4(a) shows a nonideal model of a subcircuit in delay line 1. τ_{switch} represents the propagation delay of the switches. $m_{f,i}$ and $m_{s,i}$ are the mismatch factors of the two switches. Further, τ represents the ideal delay time of a delay unit equal to those in delay-locked loop, and $m_{d,i}$ represents the mismatch factor in the delay unit. Though various mismatch and parasitic propagations exists in real circuits, only the delay time difference between slow path and fast path is considered. That is, the additional delay time while switching from fast path to slow path

$$\begin{aligned}\tau_i` &= (\tau_{switch}+m_{s,i}+\gamma+m_{d,i})-(\tau_{switch}+m_{f,i}), \\ &= \tau+(m_{d,i}+m_{s,i}-m_{f,i})\end{aligned} \tag{1}$$

where $\tau_i`$ represents the delay time difference of a nonideal subcircuit. From (1), a mismatch term contributed by nonideal effects in addition to the ideal delay time can be observed. Now, (1) can be rewritten as

$$\tau_i` = \gamma \cdot \tau + m_i, \tag{2}$$

where the two delay time difference in (1) and (2) are the same, but the effect of delay mismatches are now represented by means of a gain error factor γ and a new mismatch factor m_i. The values of γ and m_i can be derived by assuming the sum of $m_i`$ of all subcircuits equals to zero. Thus, the sum of $\tau_i`$ of all 32 subcircuits in delay line 1 can be obtain as

$$\sum_{i=1}^{32} \tau_i` = 32 \cdot \gamma \cdot \tau \cdot \tag{3}$$

And the gain error factor γ can be derived as

$$\gamma = \frac{\sum_{i=1}^{N} \tau_i`}{32 \cdot \tau} \cdot \tag{4}$$

By substituting (4) into (2) the mismatch factor m_i within each subcircuit can be obtain as

$$m_i = \tau_i` - \left(\frac{\sum_{i=1}^{N} \tau_i`}{32 \cdot \tau}\right) \cdot \tau \cdot \tag{5}$$

Note that the gain error and mismatch factor in (4) and (5) can also be related to the parameters in (1). Fig. 4(b) shows the simplified mismatch model of a subcircuit. The effects of various mismatch sources in the subcircuit are now equivalently comprehended inside the delay unit. This simplification leads to an equivalent model of the nonideal effect by means of gain error and mismatches. Analysis of nonideal effects on frequency synthesizer phase noise performance will be further derived in the following sections.

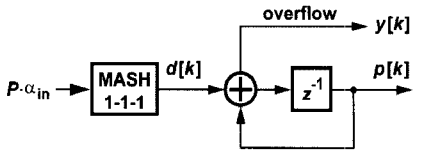
2. Re-Quantization Σ-Δ Modulator

In the proposed frequency synthesizer, to derive both accurate fractional division and low quantization noise, a re-quantization Σ-Δ modulator is implemented to control divider and delay line 1. The reason to use re-quantized Σ-Δ modulator technique rather than the more general technique, multiphase fractional division [7-9], is that the former can achieve high pass noise shaped characteristic on delay unit gain error, while in the latter one, delay unit gain error acts like random noise in the frequency synthesizer that causes in-band noise and spurious tones at the synthesizer output. The effect of delay unit gain error on the synthesizer output utilizing either technique is discussed below.

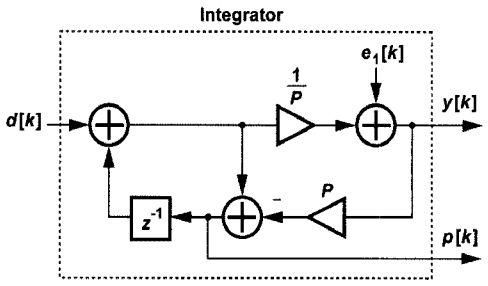
A. Multiphase Fractional Division Technique

In general, multiphase fractional division modulators are constructed with a single Σ-Δ modulator followed by an integrator, as shown in Fig. 5(a). The carry out signal *y[k]* controls the divider to produce a division value $N+y[k]$. Note that the operation of the integrator is equivalent to a first-order error-feedback Σ-Δ modulator [16], indicated in Fig. 5(b), where $e_1[k]$ represents the quantization error of the error-feedback modulator. Further, the reason for the multiplication factors $1/P$ and P is because the overflow signal occurs each time the integrator exceeds P, which is defined as T_{VCO}/τ. Now, the relation-ship between MASH 1-1-1 modulator signal *d[k]* and *y[k]*, can be described as

$$y[k]=\frac{1}{P}\cdot d[k]+\left(e_1[k]-e_1[k-1]\right) \qquad (6)$$
$$=\frac{1}{P}\cdot\left(P\cdot\alpha_{in}+Q_3[k]\right)+\left(e_1[k]-e_1[k-1]\right)$$



(a)



(b)

Fig. 5. (a) Architecture of a multiphase fractional division modulator. (b) Linear model of the integrator.

where $Q_3[k]$ is the output quantization noise of the third-order MASH 1-1-1 modulator which has a third-order noise shaped characteristic. In (6), a fractional division α_{in} plus an error term controls the division of divider. The error term in *y[k]* causes a phase deviation at the output of the divider and is derived as

$$\Phi_n[k]=\frac{2\pi}{P\cdot N_{nom}}\cdot\sum_{i=0}^{k}\left[Q_3[i]+P\cdot\left(e_1[i]-e_1[i-1]\right)\right], \qquad (7)$$

where N_{nom} represents the nominal division value of divider [15]. Furthermore, in Fig. 5(a) the signal *p[k]* decides the number of subcircuits in delay line 1 to operate by its slow path. Thus if the delay units are ideal, a total additional delay time $\tau p[k]$, is contributed by delay line 1. The total additional delay time can be equivalently converted into an additional phase expression

$$\Phi_{delay\ line\ 1}[k]=\frac{2\pi}{T_{VCO}\cdot N_{nom}}\cdot\gamma\cdot\tau\cdot p[k], \qquad (8)$$
$$=\frac{2\pi}{P\cdot N_{nom}}\gamma\cdot\left(-P\cdot e_1[k]\right)$$

where *p[k]* equals $-P\cdot e_1[k]$, as shown in Fig. 5(b). By summing (7) and (8), a total phase deviation contributed by divider and delay line 1 is obtained as

$$\Phi_n[k]=\frac{2\pi}{P\cdot N_{nom}}\cdot\left\{\sum_{i=0}^{k}\left[Q_3[i]+P\cdot\left(e_1[i]-e_1[i-1]\right)\right]\right. \qquad (9)$$
$$\left.+\gamma\cdot\left(-P\cdot e_1[k]\right)\right\}$$
$$=\frac{2\pi}{P\cdot N_{nom}}\cdot\left\{\sum_{i=0}^{k}\left(Q_3[i]\right)+(1-\gamma)\cdot P\cdot e_1[k]\right\}$$

Now the power spectral density of the phase deviation can be written as

$$S_{\Phi_n}(f)=\left(\frac{2\pi}{P\cdot N_{nom}}\right)^2\cdot\left[\left(\frac{1}{2sin(\pi fT)}\right)^2\cdot S_{Q_3}(f)\cdot +(1-\gamma)^2\cdot P^2\cdot S_{e_1}(f)\right] \quad (10)$$

Ideally, quantization error is uniformly distributed between *0* and *1*, and is modeled as an additive white noise source so that their power spectrum is flat with magni-tude 1/12 [15]. Thus, (10) can be rewritten as

$$S_{\Phi_n}(f)=\left(\frac{2\pi}{P\cdot N_{nom}}\right)^2\cdot\frac{1}{12}\cdot\left[(2sin(\pi fT))^4+(1-\gamma)^2\cdot P^2\right] \quad (11)$$

The power spectrum of phase deviation contains two noise components. One is caused by the quantization noise with a shaping factor $sin(\pi fT)^4$. As shown in (11), compared to the frequency synthesizers with no multiphase compensation, a $(1/P)^2$ reduction in power can be achieved. The other component is caused by gain error in delay units, the noise power spectrum caused by gain error shows a flat noise characteristic.

Finally, the effect of phase deviation caused by gain error in delay units to the frequency synthesizer output in multiphase fractional division techniques can be calculated as

$$S_{\Phi_{out}}(f)\Big|_{\text{Gain Error}}=\frac{1}{T}\cdot|T\cdot N_{nom}\cdot G(f)|^2\cdot\left(\frac{2\pi}{P\cdot N_{nom}}\right)^2\cdot\frac{1}{12}\cdot\left[(1-\gamma)\cdot P\right]^2, \quad (12)$$

where T and $G(f)$ represents the input reference clock period and the closed-loop transfer function of the frequency synthesizer, respectively [15].

In summary, from (12) the effect of delay unit gain error equivalently introduces a flat noise into the frequency synthesizer that causes low-passed noise at the synthesizer output. Moreover, the assumption of $e_1[k]$ as an additional white noise may not be true because the quantization error of a first-order MASH structure often shows a periodic feature. Thus, in addition to in-band noise, spurious tones will also occur at the frequency synthesizer output.

B. Re-Quantized Σ-Δ Modulator Technique

Fig. 6(a) shows the proposed digital control circuit diagram with re-quantized Σ-Δ modulator circuit. Two MASH Σ-Δmodulators are constructed in the re-quantized modulator, where the first one is a third-order MASH 1-1-1 modulator and the second one is a second-order MASH 1-1 modulator. A 20-bit fractional word is applied to the MASH 1-1-1 modulator, and the output *y[k]* controls the divider to produce a division value $N+y[k]$, where

$$y[k]=\alpha_{in}+Q_3[k]\cdot \quad (13)$$

$Q_3[k]$ is the same as those defined previously, which represents the output quantization noise caused by MASH 1-1-1 modulator and has a third-order noise shaped characteristic. In (13), a fractional word α_{in} plus an error term controls the division of divider. The error term in *y[k]* causes a phase deviation at the output of the divider that can be derived as

$$\Phi_n[k]=\frac{2\pi}{N_{nom}}\cdot\sum_{i=0}^{k}(Q_3[k])\cdot \quad (14)$$

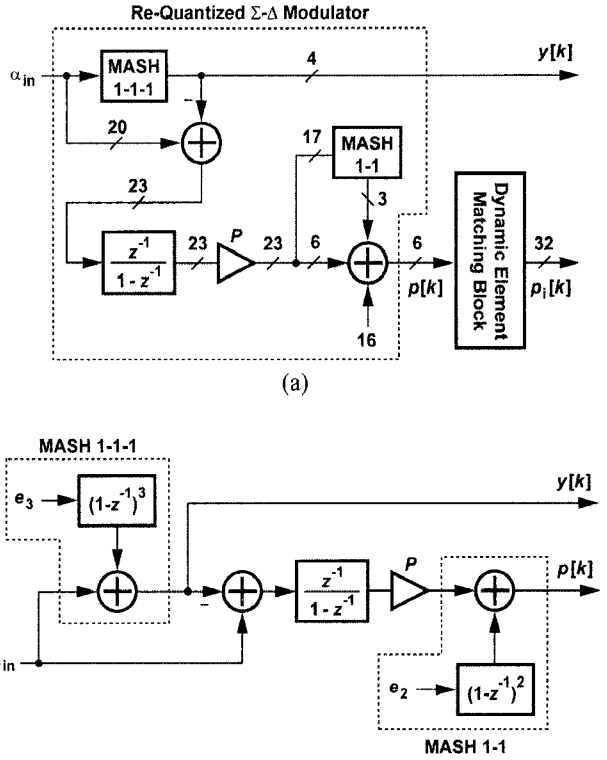


Fig. 6. (a) Architecture of the proposed digital control circuit with re-quantized Σ-Δ modulator. (b) Linear model of the re-quantized Σ-Δ modulator.

Shown in Fig. 6(a), the output of MASH 1-1-1 is subtracted with the input fractional word α_{in} to obtain $-Q_3[k]$. The subtracted value is then integrated to achieve the summation term in (14) but with negative polarity. Ideally, if this negative term can be applied to compensate (14) by controlling the amount of additional delay time in delay line 1, quantization error effect should be totally eliminated. However, since MASH 1-1-1 is operated with a 20-bit fractional division, a unit delay time τ of $T_{VCO}/2^{20}$ would be required. If the VCO operates at a frequency of 2.14 GHz for example, a unit delay time of 0.000446 psec would be needed. Such a delay-locked loop and delay line 1 would be infeasible for any available technologies. In the proposed work, an 18-dB reduction is required for our frequency synthesizer, which is equivalent to *1/8* reduction on quantization error or suppressing the 3 MSBs of the quantization error, thus an unit delay time of 58.4 psec is needed, which is designed in our delay-locked loop and delay line 1. The remaining 17-bit errors will be truncated by means of the MASH 1-1 modulator.

The output of integrator is then multiplied by P, which is defined previously as the ratio between T_{VCO} and unit delay time τ, and is equal to *8* in this work. Note that a multiplication of *8* can be derived easily by shifting the binary word 3 bits leftward. The multiplied signal is then divided into two components, an integer component of 6 bits and a fractional component of 17 bits, respectively. The 17-bit fractional component is re-quantized by a second-order MASH 1-1 Σ-Δmodulator. Finally, the output signal $p[k]$ is constructed by adding the 6-bit integer component with the output of the second Σ-Δmodulator. As shown in Fig. 6(a), an integer number of 16 is also added to $p[k]$. This is to insure the output signal $p[k]$ to be positive, since in PLL based frequency synthesizers, a constant delay time added on the feedback signal to PFD would not affect the performances of the synthesizer. Note, the number 16 is determined through simulation results, this will be explained later with the discussion of the number of delay units needed in delay line 1.

Fig. 6(b) shows the linear model of the re-quantized Σ-Δ modulator. The output signal $p[k]$ decides the number of subcircuits in delay line 1 to pass its input signal through slow path. If the delay units are ideal, a total additional delay time $\tau p[k]$ can be achieved by delay line 1. The total additional delay time can be equivalently converted into an additional phase expression

$$\Phi_{delay\ line\ 1}[k]=\frac{2\pi}{P\cdot N_{nom}}\cdot\gamma\cdot p[k] \qquad (15)$$
$$=\frac{2\pi}{P\cdot N_{nom}}\cdot\gamma\cdot\left(P\cdot\sum_{i=0}^{k}(-Q_3[k])+Q_2[k]\right)$$

where $Q_2[k]$ represents the output quantization noise caused by the MASH 1-1 modulator which has a second-order noise shaped characteristic. By summing (14) and (15), a total phase deviation contributed by divider and delay line 1 can be calculated as

$$\Phi_n[k]=\frac{2\pi}{P\cdot N_{nom}}\cdot\left\{P\cdot(1-\gamma)\cdot\sum_{i=0}^{k}Q_3[i]+\gamma\cdot Q_2[k]\right\}. \qquad (16)$$

Therefore, the power spectral density of the phase deviation can be written as

$$S_{\Phi_n}(f)=\left(\frac{2\pi}{P\cdot N_{nom}}\right)^2\cdot\frac{1}{12}\cdot(2\sin(\pi fT))^4\left[(1-\gamma)^2\cdot P^2+\gamma^2\right]. \qquad (17)$$

In (17), the power spectrum of phase deviation also contains two noise components, such as (11), one caused by quantization noise and the other caused by delay unit gain error. However, in (17), both components are shaped by the filter $\sin(\pi fT)^4$. While in (11), with multiphase fractional division technique, delay unit gain error generates flat noise in the frequency synthesizer.

Finally, the effect of phase deviation caused by delay unit gain error to the frequency synthesizer output in re-quantized Σ-Δ modulator technique can be calculated as

$$S_{\Phi_{out}}(f)\Big|_{\text{Gain Error}}=\frac{1}{T}\cdot\left|T\cdot N_{nom}\cdot G(f)\right|^2\cdot\left(\frac{2\pi}{P\cdot N_{nom}}\right)^2\cdot \qquad (18)$$
$$\cdot(2\sin(\pi fT))^4\cdot\frac{1}{12}\cdot\left[(1-\gamma)\cdot P\right]^2$$

According to (17) and (18) the effect of delay unit gain error equivalently introduces a white noise filtered by a second-order high-pass filter on the frequency synthesizer output. Compared with the results in (11) and (12) using multiphase fractional division technique, the in-band noise and spurious tones can thus be avoided.

Now, the number of subcircuits needed in delay line 1 to produce proper additional delay intervals is analyzed.

The number of subcircuit needed is directly proportional to the quantization error caused by the first Σ-Δ modulator MASH 1-1-1, which causes phase deviation at the divider output, and inverse proportional to the delay time of a unit delay element, that is

$$T_{VCO} \cdot N_{nom} \cdot \frac{(\Phi_n`[k]_{max} - \Phi_n`[k]_{min})}{2\pi} \cdot \frac{1}{\tau} \cdot = P \cdot N_{nom} \cdot \frac{(\Phi_n`[k]_{max} - \Phi_n`[k]_{min})}{2\pi} \quad (19)$$

However, the exact number should be obtained through behavioral simulation, and observing the dynamic range of the output signal *p[k]*. Fig. 7 shows the behavioral simulation results of a re-quantized Σ-Δ modulator. The output signal *p[k]* is in the range of +16~-16 without adding the constant number 16 previously mentioned. Thus, 32 subcircuits are required in delay line 1 for multiphase compensation utilizing the re-quantized Σ-Δ modulator proposed in Fig. 6(a).

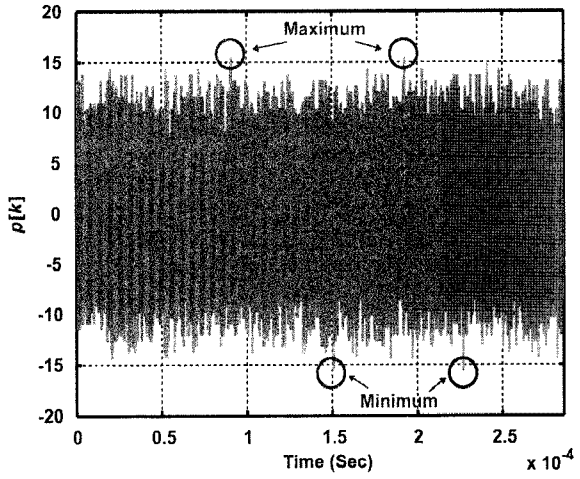


Fig. 7. Behavioral simulation result of re-quantized Σ-Δ modulator output signal *p[k]*, without adding constant integer 16.

3. Dynamic Element Matching Technique

Refer to the subcircuit model shown in Fig. 4(b), ideally all the delay units are equal with a delay time τ, but due to mismatches, they have a random distribution. To simplify the analysis, only the effect of delay mismatch m_i is considered. During each reference cycle, certain amount of subcircuits in delay line 1 is selected. The selected subcircuits operate with its slow path which contributes an additional delay time for compensating the quantization noise. A mismatch value *m[k]* can be defined as the deviation time from the ideal delay time at the output of delay line 1. Thus, *m[k]* can be equivalently derived by summing up all m_i of the delay units in each selected subcircuit. A simplest way of choosing the subcircuits is by thermometer code. Therefore, the mismatch value at the delay line 1 output can be described as

$$m[k] = \sum_{i=1}^{p[k]} p_i[k] \cdot m_i = \sum_{i=1}^{p[k]} m_i, \quad (20)$$

where $p_i[k]$ is a one-bit signal that controls the i^{th} subcircuit in delay line 1, and has the value of either 0 or 1. If $p_i[k]$ equals to 0, the subcircuit operates with its fast path, on the other hand, if $p_i[k]$ equals to 1, the subcircuit operates with its slow path. Assume *p[k]* is a random number, and the multiphase mismatch value *m[k]* in (20) can be modeled as a random process with white noise spectrum. Thus, the noise power caused by multiphase mismatch of delay line 1 can be obtained as

$$S_m(f) = \left(\frac{2\pi}{8 \cdot N_{nom}} \cdot \frac{\sigma_m}{T_{VCO}/8}\right)^2 = \left(\frac{2\pi}{N_{nom}} \cdot \frac{\sigma_m}{T_{VCO}}\right)^2, \quad (21)$$

where σ_m represents the variance of *m[k]*. And the effect of mismatch noise to the frequency synthesizer output can be derived as

$$S_{\Phi_{out}}(f)\Big|_{\text{Mismatch Noise}} = \frac{1}{T} \cdot \left|T \cdot N_{nom} \cdot G(f)\right|^2 S_m(f) = \frac{1}{T} \cdot \left|T \cdot N_{nom} \cdot G(f)\right|^2 \cdot \left(\frac{2\pi}{N_{nom}} \cdot \frac{\sigma_m}{T_{VCO}}\right)^2 \quad (22)$$

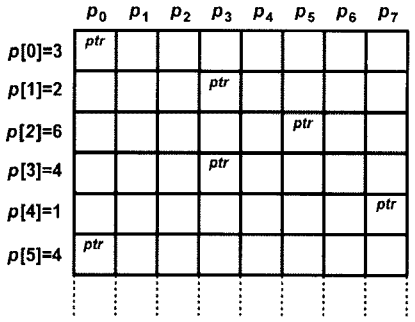
From (22), if the subcircuits are chosen by thermometer code, the mismatch noise *m[k]* in spectrum will be a flat noise that causes in-band noise and spurious tones at the frequency synthesizer output.

Dynamic element matching is a technique for oversampled digital to analog converters to improve their linearity. The purpose of DEM is to select elements such that mismatch noise can be pushed away to high offset frequency where it can be removed by filtering. As shown in Fig. 2 and Fig. 3, in the proposed multiphase compensation frequency synthesizer with delay line 1, DEM techniques can be employed to select the subcircuit in delay line 1

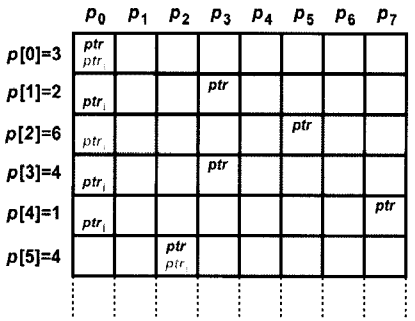
to push the mismatch noise to high offset frequencies.

Many DEM algorithms, including random selection, individual level averaging, data weighted averaging [14], and segmented encoder [17], were reported. In the proposed frequency synthesizer, a DEM technique utilizing data weighted averaging (DWA) is employed to yield a first-order shaping of the mismatch noise. In Fig. 8(a), the selection of the subcircuits in DWA is shown. For convenience, eight subcircuits are used in this example. During each clock cycle, a number of subcircuit corresponding to the input code $p[k]$ is selected clockwise, starting from the position indicated by a pointer ptr, with $0 \leqq aptr < L$, where L is the number of subcircuits in delay line 1. At each clock cycle, the pointer is updated by incremented modulo L with the input code. On the next cycle, the selection will start from the new position of the pointer. The concept is to select all the delay units in the fasted way, since the sum of the mismatch of all delay units is zero. This ensures the low frequency noise components to be minimized. Mathematically, the mismatch noise $m[k]$ can be shown as [13,14]

$$m[k]=\sum_{i=0}^{ptr[k]-1} m_i - \sum_{i=0}^{ptr[k-1]-1} m_i \quad (23)$$
$$= IM[ptr[k]] - IM[ptr[k-1]]$$



(a)



(b)

Fig. 8. (a) Example of data weighted averaging algorithm. (b) Example of data weighted averaging algorithm with increased index.

The function $IM[ptr]$, called integral mismatch, corresponds to the mismatches of the delay units accumulated along the array up to the position of the pointer. Now the power spectrum of the mismatch noise in (23) can be expressed as

$$S_m(f)=\left(2\sin(\pi fT)\right)^2 \cdot \left(2\pi \frac{\sigma_m}{T_{VCO}}\right)^2 \cdot \quad (24)$$

The integral mismatch function $IM[ptr]$ can be assumed to be white random process with a variance σ_m. Therefore, the effect of mismatch noise to the frequency synthesizer output can be expressed as

$$S_{\Phi_{out}}(f)\Big|_{\text{Mismatch Noise}} = \frac{1}{T} \cdot \left|T \cdot G(f)\right|^2 \left(2\sin(\pi fT)\right)^2 \cdot \left(2\pi \frac{\sigma_m}{T_{VCO}}\right)^2 \cdot \quad (25)$$

While DWA has the advantage of noise shaping the spectrum of delay mismatches, it also creates spurious tone. A $F_{ref}/2$ tone has been observed in behavioral simulations. This fractional tone occurs because the average number of subcircuits selected to operate with slow path in a reference cycle is $L/2$. Thus, all subcircuits in delay line 1 will be selected once by an average of two reference cycles. Further, since the sum of the mismatch of all delay units is zero, a periodic mismatch noise of period $2T_{ref}$ occurs.

To resolve this problem, a simple modification in DWA mechanism has been presented, named data weighted algorithm with increased index (DWAinc). In Fig. 8(b), the selection of the subcircuits in DWAinc is shown. The algorithm of DWAinc is similar to DWA. In addition to the pointer ptr, another pointer ptr_i is applied, same with $0 \leqq ptr_i < L$. Initially, ptr_i is set to zero, during each clock cycle, if ptr is not equal to ptr_i, the subcircuit selection will be the same as DWA. But if ptr equals to ptr_i at the beginning of a clock cycle, a random number will be assigned to both ptr and ptr_i, and the subcircuit selection will continue by the new ptr. For example, in Fig. 8(b), initially both ptr and ptr_i are 0, the selection starts from the subcircuit p_0 and proceeds in a rotational manner such as DWA. However, in the fifth clock cycle, the subcircuit selection ends at p_7 and sets ptr to zero. Therefore, at the beginning of the sixth clock cycle an equivalent value of ptr and ptr_i is detected, thus a new random value 2 is assigned to them and the subcircuit selection

proceeds from p_2. In the behavioral simulation, great reduction on the $F_{ref}/2$ tone has been detected, with the expense of little in-band noise increment compared to DWA. But still much lower than those with no dynamic element match technique applied.

Fig. 9 shows the proposed digital control circuit with DEM block. The two DEM algorithms, DWA and DWAinc are both built in the digital control circuit. Finally, Fig. 10 shows a linear model of multiphase compensation Σ-Δ fractional-N frequency synthesizers, including the effect of quantization noise, multiphase mismatch and delay unit gain error.

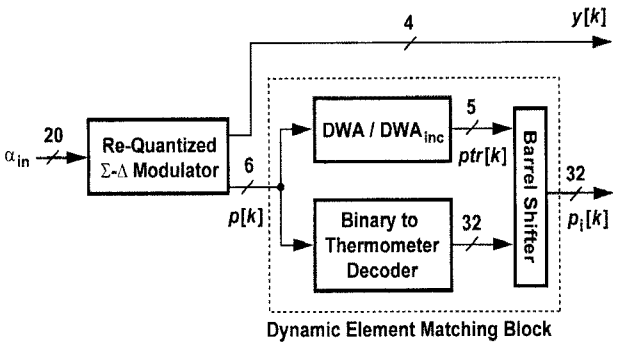


Fig. 9. Architecture of the proposed digital control circuit with DEM block.

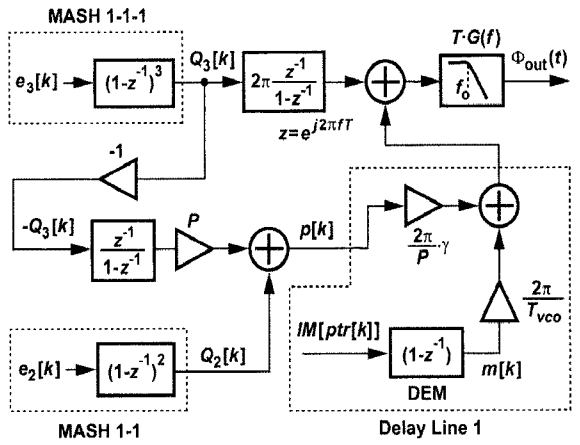


Fig. 10. Linear model of a multiphase compensation Σ-Δ frequency synthesizer.

III. CIRCUIT IMPLEMENTATION

This frequency synthesizer is implemented in a 0.18-μm CMOS technology. All the blocks shown in Fig. 2 except the loop filter capacitors are implemented on-chip. A summary of the designed loop parameters are shown in Table 1.

Table 1. Frequency synthesizer parameters.

Fractional-N Frequency Synthesizer Parameters	
Reference Frequency	35 MHz
Output Frequency	2.11GHz – 2.17GHz
Loop Bandwidth	200 KHz
Charge Pump Current	50 μA
VCO Gain	200 MHz/V

1. Subcircuits in Delay Line 1

An example of a subcircuit in delay line 1 is shown in Fig. 11. The subcircuit is used to generate the additional delay time τ. The selection of fast path and slow path is by setting $p_i[k]$ to 0 and 1, respectively. The delay line 1 consists of 32 subcircuits.

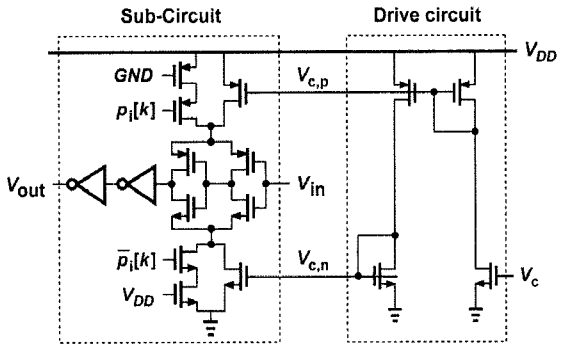


Fig. 11. Schematic of the i^{th} subcircuit in delay line 1, and the driver circuit.

The delay units in delay line 2 of delay-locked loop shown in Fig. 2 are also constructed by the subcircuit in Fig. 11. Delay line 2 consists of 16 subcircuits, the 16 subcircuits are divided into two groups, each of which consists 8 subcircuits cascaded in line. The subcircuits in the first line operate by slow path, and input a 0-degree signal of a period $T_{VCO}/4$. The subcircuits in the second line operate by fast path, and input a 90-degree signal of a period $T_{VCO}/4$. The output signals of the two lines compare their phases at the phase frequency detector. Ideally, when delay-locked loop is in locked condition, the delay time difference between slow path and fast path of all subcircuits will be τ, or equivalently $T_{VCO}/8$.

The delay time of each subcircuit in both delay line 1 and delay line 2 are set the same by sharing the same voltage control signal V_c.

2. Divider

Shown in Fig. 12, the core of the frequency divider is

a pulse-swallow divider. The pulse-swallow divider consists of a dual-modulus prescaler, a fixed-ratio program counter and a programmable swallow counter. The prescaler is built with current-mode logic (CML), and the other two counters are built with static CMOS logic. The output of the prescaler drives a level shifter buffer to produce rail-to-rail signals for the following stages. The overall divide ratio is equal to $NP+S$. In this work, N=4, P=14, S=1~16, so the total divided ratio can be varied from 57 to 72.

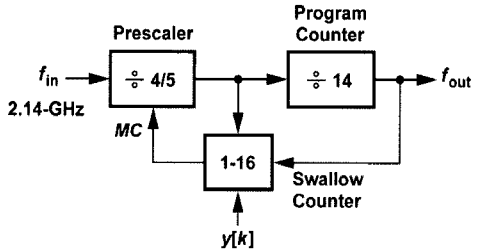


Fig. 12. Architecture of the multi-modulus divider.

A divided-by-4 TSPC flip-flops is also implemented in the divider, and is not depicted in Fig. 12. The purpose of the divided-by-4 circuit is to gene-rate two quadrature signals with a period of $T_{VCO}/4$ for the delay-locked loop inputs.

3. PFD

Besides the nonideal effect of multiphase mismatch, nonlinearity in the PFD-CP I/O characteristic also increases in-band noise and spurious tone. Typical PFD-CP nonlinearity shown in Fig. 13, include current source mismatch between up and down currents, and dead zone. The solid lines represent nonlinear circuit, and the dashed lines represent the idea ones. Q and $\Delta\Phi$ represents the amount of charge injected into the loop filter and input phase error of PFD-CP, respectively. To resolve the nonlinearity problem, a simple way is to inject a dc current

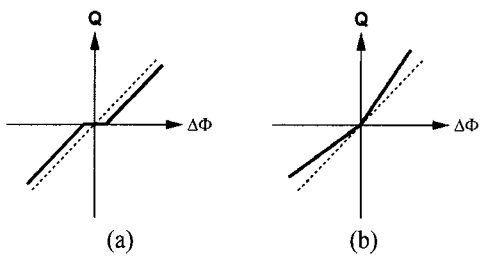


Fig. 13. PFD-CP nonlinear I/O characteristic. (a) Current source mismatch. (b) Dead zone.

into the loop filter. This forces the lock point of the PLL no longer at 0-degree of phase error and, thus, the residual nonlinearity near 0-degree phase error can be avoided. However, the method of injecting dc current into the loop filter increases the reference spurs.

Another solution is by the injection of periodic current pulses into the loop filter. The idea is to yield a constant down current pulse, and allow the width of the up current pulses to vary with the input phase error. By this method, the operation of PFD-CP can be forced outside the nonlinear region. Fig. 14 shows the proposed modified PFD architecture and the timing diagram of the signals in the PFD-CP in locked condition. The *Up* and *Dn* signals controls the up and down currents of CP, respectively. As shown, an additional D-Flip-Flop (DFF) is introduced. Unlike conventional tri-state PFD, in the proposed circuit, the DFF reset signal is controlled by the signals *Up* and Dn_{delay}, when both of them are high, the output of the NAND logic becomes low and the three DFF are reset. On the other hand, in conventional tri-state PFD the reset signal is controlled by the signals *Up* and *Dn*. The Dn_{delay} signal is triggered by the rising edge of input signal V_{FB_dely}. A delay line circuit which is not depicted in Fig. 14, generates V_{FB_delay} which is a replica of V_{FB} with the delay time t_d. The combination of V_{FB} and V_{FB_delay} guarantees a constant down current periodically injected to the loop filter with a pulse width of t_d. The delay time is designed long enough to force the PFD away from its nonlinear region.

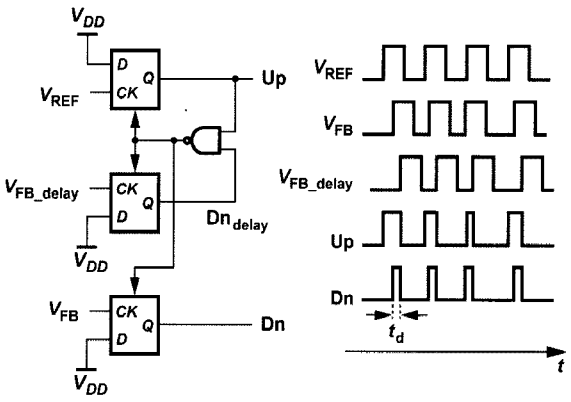


Fig. 14. Architecture of phase frequency detector, and the constant current pulse circuit.

4. VCO

The VCO is built with a negative-g_m CMOS LC oscil-

lator, consisting of a differential spiral inductor and two MOS varactors. To have wide tuning range and small VCO gain, coarse digital tuning is provided by 3-bit binary weighted switching MIM capacitors, the capacitors values are 200 pF, 400 pF, and 800 pF. The VCO is designed to provide tuning range over a 0.4-1.4V range with a nominal K_{VCO} of 200 MHz/V.

5. Loop Filter

A third-order passive loop filter is used as the frequency synthesizer loop filter, shown in Fig. 15. The loop filter components are as follows: C_1 = 30 pF, C_2 = 422 pF, C_3 = 3 pF, R_2 = 7.5 KΩ and R_3 = 4.5 KΩ, of which R_2, C_1, and 15 pF of C_2 are off-chip. The remaining of 15 pF of C_2 is on chip to help reduce the voltage variation caused by fast charge pump current switching through the inductive bond wires. Given that the VCO gain is 200 MHz/V, the divider modulus is around 61, and the charge pump current is 50μA, the proposed frequency synthesizer bandwidth is approximately 200KHz.

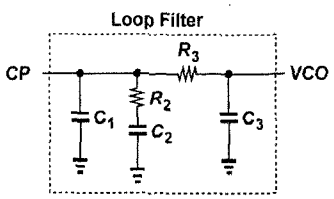


Fig. 15. A third-order passive loop filter.

IV. Experimental Results

The proposed frequency synthesizer is fabricated in a 0.18-μm CMOS technology. The die photo of the chip is shown in Fig. 16. The die area is 0.92 mm × 1.15 mm (1 mm^2) including the measurement pads. The chip is tested on an evaluation printed circuit board. The total power consumption is 27.2 mW. All digital control signals are supplied through the three-wire serial interface, and the reference frequency used is 35 MHz.

The frequency synthesizer is tested in four different operation modes: without multiphase compensation method, multiphase compensation without DEM techniques, multiphase compensation with DWA and, multiphase compensation with DWAinc, respectively. Fig. 17 shows the frequency synthesizer output spectrum in locked condition. Fig. 18 shows the synthesizer output phase noise, with and without multiphase compensation. As shown, with quantization noise compensation technique, a 10-dB reduction of phase noise at the offset frequency of 10 MHz with a 2.14 GHz carrier signal can be achieved. The 10-

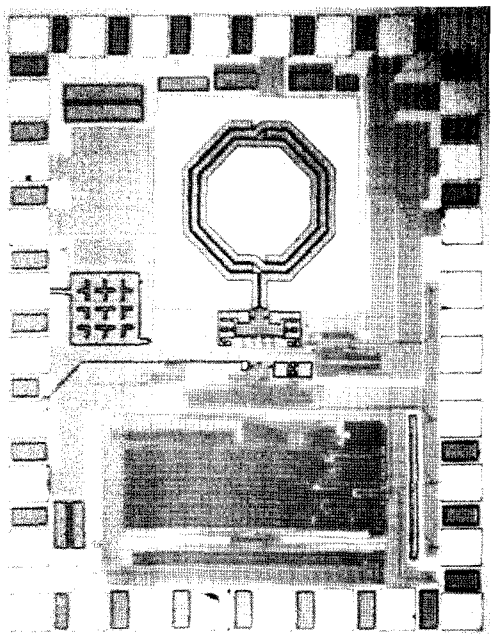


Fig. 16. Die photo of the frequency synthesizer.

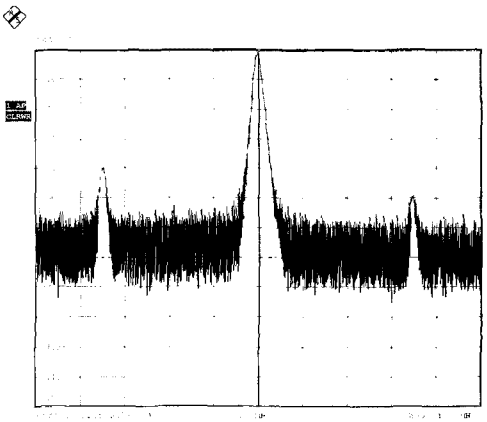


Fig. 17. Output spectrum of the frequency synthesizer.

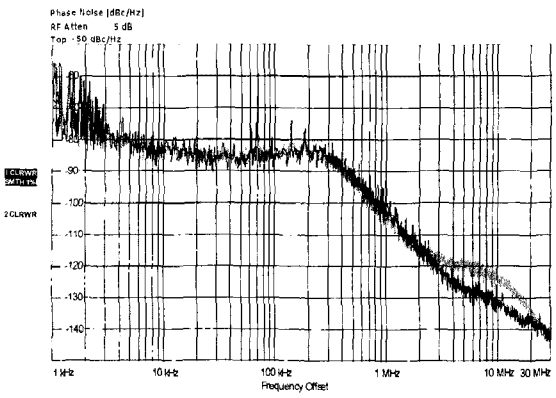
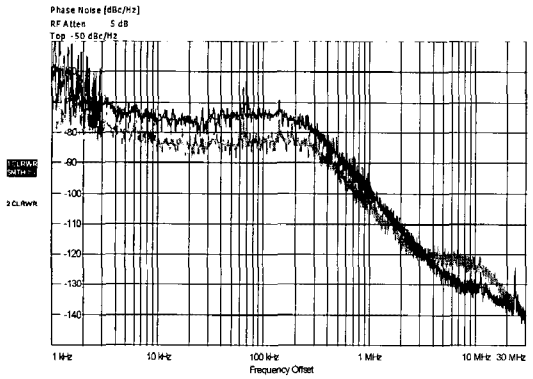


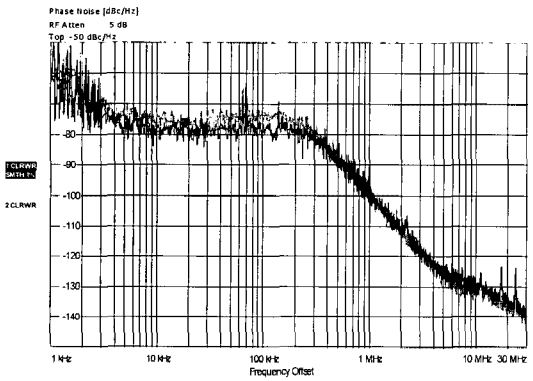
Fig. 18. Phase noise measurement results, without multiphase compensation (light) and with multiphase compensation (dark).

dB reduction rather than an 18-dB reduction is caused by the high noise floor at 10 MHz frequency offset rather than the quantization noise.

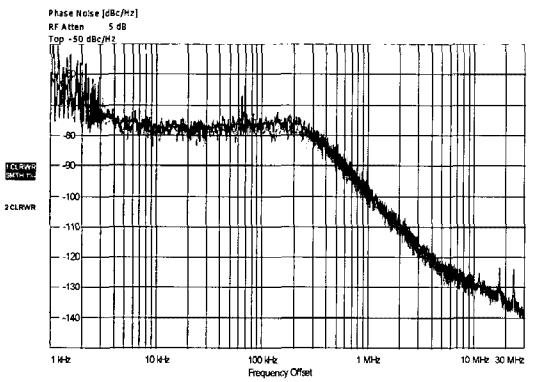
For the measurement results of multiphase compensation method with DEM techniques activated and deactivated, the measured in-band noise floor is -82 dBc/Hz for all three compensation modes. These measurement results correspond to an amount of up to 40% delay mismatches. Therefore, possible noise sources, such like noise from CP current source, nonlinear PFD+CP I/O characteristic and, digital circuit noise, might have been folded back to low offset frequencies and thus dominates the in-band noise.



(a)



(b)



(c)

Fig. 19. Measurement results of output phase noise, with V_c manually set to 0.7 V. (a) No compensation applied (light) and, compensation applied without DEM technique (dark). (b) Compensation applied without DEM technique (light) and, Compensation applied with DWA technique (dark). (c) Compensation applied with DWA technique (light) and, Compensation applied with DWAinc technique (dark).

Although the in-band noise now dominates by various noise sources rather than multiphase mismatch, in order to demonstrate the effect of DEM techniques, the measured phase noise performance improvement can be observed by manually setting signal V_c=0.7. Note, in ordinary, V_c is generated by the locked delay-locked loop. The idea here is to manually lower the potential of V_c to increase the delay time mismatches, which has been verified in transistor-level simulations. Shown in Fig. 19(a), 10-dB in-band noise increment due to multiphase compensation without DEM technique is detected compared to the case with no compensation applied. In Fig. 19(b), shows a 4-dB in-band noise reduction due to DWA technique compared to the case with no DEM technique applied. Also, a fractional tone $f_{fref}/2$ appears when DWA is activated. Finally, in Fig. 19(c), compared to DWA a little in-band noise increment is shown in DWAinc technique with a 7-dB suppression on the $f_{fref}/2$ tone. A summary of performances is shown in Table 2.

Table 2. Measured performance summary.

Fractional-N Frequency Synthesizer	
Technology	0.18 μm CMOS
Power Consumption	27.2 mW
Frequency Range	2.11GHz~2.17 GH
Frequency Step Size	4 Hz
Synthesizer Phase Noise (with out compensation)	-82 dBDc/Hz @ 10KHz -84 dBDc/Hz @ 100KHz -103 dBDc/Hz @ 1MHz -122 dBDc/Hz @ 10MHz
Synthesizer Phase Noise (with compensation)	-82 dBDc/Hz @ 10KHz -84 dBDc/Hz @ 100KHz -103 dBDc/Hz @ 1MHz -132 dBDc/Hz @ 10MHz
Bandwidth	250 KHz
Lock Time	< 25 μsec
Chip Size	0.92 × 1.15 mm^2
Reference Spur	-40 dbc @ 35 MHz

V. CONCLUSIONS

In this work, a multiphase quantization noise suppression technique for fractional-*N* frequency synthesizers is proposed and demonstrated in 0.18-μm CMOS technology. The experimental results show the out-of-band phase noise contributed by the modulator is reduced by 10 dB, where the out-of-band phase is dominated by the quantization noise. The phase noise cancellation technique relaxes the fundamental tradeoff between phase noise and bandwidth in conventional fractional-*N* frequency synthesizers and does not require tight component matching. The measurement results show -82 dBc/Hz in-band phase noise within the loop bandwidth of 200 kHz, and -103 dBc/Hz and -132 dBc/Hz out-of-band phase noise at 1 MHz and 10 MHz offset frequency. The lock time is less than 25 μs.

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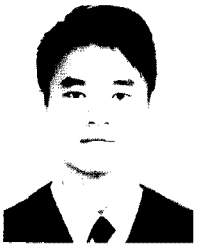

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