Implementation and Performance Analysis of a Digital IF Transceiver for an SDR-based Reconfigurable Base Station

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ABSTRACT

This paper presents the implementation and performance test of a Digital IF transceiver for a SDR-based mobile communication base station. The transceiver is reconfigurable to HSDPA and to three profiles, 7 MHz, 3.5 MHz, and 1.75 MHz, each incorporating the IEEE 802.16d WiMAX standard. The transceiver can be reconfigured to other standard profiles through software downloaded onto identical hardware platforms. Experimental results show that the transceiver can be reconfigured to other systems and the performance of the transceiver satisfies the recommended performance criteria of each standard.

Key Words : SDR (Software Defined Radio), Digital IF, HSDPA (High Speed Downlink Packet Access), WiMAX, OFDM, Transceiver

I. Introduction

Recently, mobile communication systems have been recommended to support several frequency bandwidth profiles according to the required user bandwidth in various radio environments. Upcoming fourth-generation mobile systems based on Orthogonal Frequency Division Multiplexing (OFDM) technology have a range of system bandwidth profiles [1]-[3].

In view of the implementation issues, a base station with conventional hardware architecture consisting of a Radio Frequency (RF) part, an Intermediate Frequency (IF) part and a baseband modem part is not sufficiently flexible to accommodate several bandwidth profiles efficiently. Therefore, a software radio architecture that can flexibly adopt the various system profiles is needed for the future mobile communication base station [4],[5]. SDR technology is a promising feature that makes it possible to accommodate several standards through software changes on an identical hardware platform for mobile communication systems[6]. Software radio architectures can be identified where the analog to digital conversion takes place in view of translating an RF analog signal to a digital signal. As analog to digital conversion takes place near the receiving antennas, it is evident that software architecture can achieve increasing flexibility via increased programmability found in digital filter technology, as in [7].

Many studies related to the Digital IF transceiver using SDR technology have been conducted. The research into Digital IF transceivers for mobile base stations using SDR technology has mainly focused on the implementation and design of the transceiver to support a single standard, such as W-CDMA (Wideband Code Division Multiple Access) [8]. In addition, several studies on Digital IF transmitter or receiver architecture to reduce the hardware implementation complexity have been performed, especially for the handset application requiring low power consumption [9]-[11]. However, the study and the implementation structure of the digital IF transceiver using SDR technology which can adopt the heterogeneous system for the mobile base

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논문번호 : KICS2008-05-204, 접수일자 : 2008년 5월 8일, 최종논문접수일자 : 2008년 9월 1일

station has not yet been reported.

In this study, we present an SDR-technology-based digital IF transceiver for a mobile communication base station that is reconfigurable to an HSDPA standard and to three bandwidth profiles, 7 MHz, 3.5 MHz, and 1.75 MHz, incorporating the IEEE 802.16d WiMAX standards. In addition, the test results show the performance of the implemented transceiver satisfies the recommended performance criteria of each standard by revealing the EVM value of the downlink IF output taken from the measurement instruments.

This paper is organized as follows. In section II, the overall Digital IF transceiver architecture and design specifications are described. In section III, the implemented base station and the transceiver board, including the printed circuit board (PCB) assembly, is presented. In section 4, the test result, including the reconfiguration function to the other system standards through a software download is verified by examining the downlink IF transceiver output signals. Finally, conclusions are presented in Section V.

II. Design of the Digital IF Transceiver

In this section, we introduce the overall implemented Digital IF transceiver architecture and design specifications. The main functions of the Digital IF transceiver include the frequency up-conversion of a baseband signal from a modem to an analog IF signal, in addition to the frequency down-conversion of an analog IF signal from an RF transceiver to a digital baseband signal. The RF transceiver down-converts the RF signal from a receiver antenna to an analog IF signal in the heterodyne architecture system. In addition, the Digital IF transceiver has a channelization function that splits one Analog to Digital Converter (ADC) output signal into two paths for two FAs signal processing events on the down-conversion side, and it combines the two FAs digital signals into one combined digital signal for the up-conversion side. The one combined digital signal is then entered into the Digital to Analog Converter (DAC) on the up-conversion side, as the designed transceiver supports two FAs diversity paths in both the uplink and downlink directions.

Digital IF technologies incorporate solutions to problems that easily occur on conventional heterodyne systems using analog components such as rejection of in-phase and quad-phase signal mismatch and DC offset problems. Therefore, Digital IF transceivers can provide higher performance than analog IF transceivers having signal distortion by nonlinearity, because they can combine multiple FAs on a digital domain using the complex quadrature modulation and demodulation technique for a multicarrier system.

2.1 The design of transmitter parts

The transmitter architecture of the presented Digital IF transceiver for a base station supporting two FAs is shown in Fig. 1. As seen in the figure, the transceiver takes a functional block for frequency up-conversion and digital combining of two FA signals for the downlink direction.

In the HSDPA system, digital in-phase and quad-phase baseband signals received from a modem corresponding to each FA are sent to the Digital IF transmitter at a rate of 4 oversamples of the fundamental frequency of 3.84 Mbps and at a

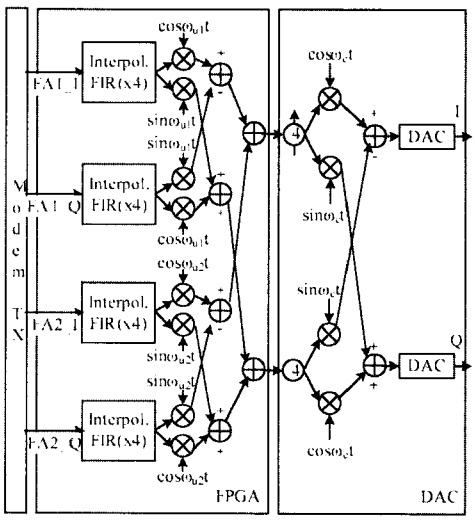

Fig. 1. Transmitter architecture of transceive

rate of two oversamples of the fundamental frequency for the WiMAX system. Each digital signal is interpolated to a higher sample rate signal by passing through the x 4 interpolation Finite Impulse Response (FIR) filters. As can be seen in Fig. 1 each signal is modulated to a higher frequency using a numerically controlled oscillator (NCO) to remove the image signals. After this digital complex quadrature modulation (DCQM), the two FA signals are digitally combined to each in-phase and quad-phase signal entering the commercial DAC chip.

Finally, DAC generates the IF analog two-channel output signal centered on 80 MHz and this signal is passed over to the RF transceiver. When $S_I(t)$ is I-channel DAC input signal from FPGA expressed in (1), it can be shown easily that the resulting analog IF I-channel signal $A_I(t)$ is expressed by the following equation (2).

$$S_I(t) = (I_1(t)\cos w_{u1}t - Q_1(t)\sin w_{u1}t) + (I_2(t)\cos w_{u2}t - Q_2(t)\sin w_{u2}t) \tag{1}$$

$$\begin{aligned} A_I(t) &= S_I(t)\cos w_c t - S_Q(t)\sin w_c t \\ &= \{(I_1(t)\cos w_{u1}t - Q_1(t)\sin w_{u1}t) + (I_2(t)\cos w_{u2}t - Q_2(t)\sin w_{u2}t)\}\cos w_c t \\ &\quad - \{(I_1(t)\sin w_{u1}t + Q_1(t)\cos w_{u1}t) + (I_2(t)\sin w_{u2}t + Q_2(t)\cos w_{u2}t)\}\sin w_c t \\ &= I_1(t)\cos(w_{u1} + w_c)t - Q_1(t)\sin(w_{u1} + w_c)t \\ &\quad + I_2(t)\cos(w_{u2} + w_c)t - Q_2(t)\sin(w_{u2} + w_c)t \end{aligned} \tag{2}$$

Similarly, Q-channel signal $S_Q(t)$ and $A_Q(t)$ are

$$S_Q(t) = (I_1(t)\sin w_{u1}t + Q_1(t)\cos w_{u1}t) + (I_2(t)\sin w_{u2}t + Q_2(t)\cos w_{u2}t) \tag{3}$$

$$\begin{aligned} A_Q(t) &= S_I(t)\sin w_c t + S_Q(t)\cos w_c t \\ &= \{(I_1(t)\cos w_{u1}t - Q_1(t)\sin w_{u1}t) + (I_2(t)\cos w_{u2}t - Q_2(t)\sin w_{u2}t)\}\sin w_c t \\ &\quad + \{(I_1(t)\sin w_{u1}t + Q_1(t)\cos w_{u1}t) + (I_2(t)\sin w_{u2}t + Q_2(t)\cos w_{u2}t)\}\cos w_c t \\ &= I_1(t)\sin(w_{u1} + w_c)t + Q_1(t)\cos(w_{u1} + w_c)t \\ &\quad + I_2(t)\sin(w_{u2} + w_c)t + Q_2(t)\sin(w_{u2} + w_c)t \end{aligned} \tag{4}$$

where $I_i(t)$ and $Q_i(t)$, i = 1, 2, are in-phase and quad-phase signals, respectively, associated with two baseband channels. Here, ω_{u1} = 16.16 MHz, ω_{u2} = 20.96 MHz, and ω_c = 61.44 MHz for the HSDPA system. For WiMAX systems, ω_{u1} = 12 MHz, ω_{u2} = 20 MHz, and ω_c = 64 MHz respectively.

2.2 The design of receiver parts

Figure 2 shows the transceiver architecture of the receiver side for the uplink direction. The receiver side has two main functions, frequency down-conversion and channelization, that split one ADC output signal into two paths. The input of this receiver is an analog IF signal from an RF transceiver. Here, the RF transceiver down-converts the RF signal from a receiver antenna to an analog IF signal. The analog IF signal to Digital IF receiver side involves analog to digital conversion through an ADC operating with a specific sampling clock rate.

Band-pass sampling or sub-sampling is considered in the sampling process for the presented transceiver receiver design. For band-pass signals, band-pass sampling states that sampling rate at the rates just more than two times of the signal bandwidth can perfectly reconstruct the original information using in-band alias. Therefore, this sampling scheme can be efficiently implemented at an IF or RF sampling stage with sampling rates lower than the Nyquist sampling rate. For a Digital IF transceiver using a band-pass sampling scheme, the ADC sampling frequency must be selected carefully so that digital images do not overlap each other after the analog to digital conversion [12],[13].

The sampled signal is then split into two paths for FA channel splitting. After being demodulated to the baseband signal using the NCO blocks, the output signal is down-sampled by two through a decimation filter adapted to each in-phase and

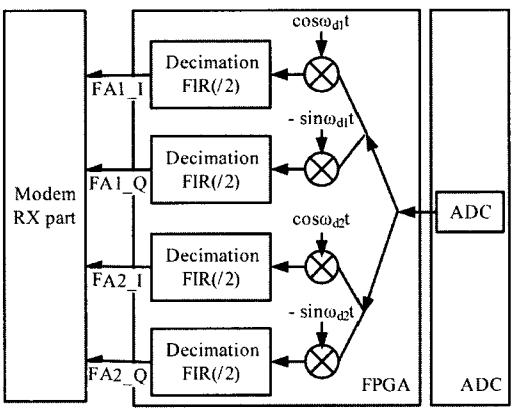

Fig. 2. Receiver architecture of transceiver

quad-phase path for HSDPA. Here, ω_{d1} = 16.16 MHz, and ω_{d2} = 20.96 MHz for HSDPA, as shown in Fig. 2. When the transceiver is reconfigured to the WiMAX system, ω_{d1} = 12 MHz, and ω_{d2} = 20 MHz.

2.3 Design of the digital FIR Filters

As the signal bandwidths and digital sample rates differ for each system and profiles, the filters should be designed individually. The same filter was used on the down-conversion side for the receiver. All interpolation filters have the same type of raised cosine filter and the same number of tabs, specifically, 129. We focused on the FIR performance and speed rather than logic cell dimensions when we designed the digital filters. The designed digital FIR filter specifications are shown in Table 1, according to the HSDPA system and three WiMAX profiles.

Table 1. FIR filter specifications.

Profile	HSDPA	WiMAX		
		7 MHz	3.5 MHz	1.75 MHz
FIR type	Raised cosine	Raised cosine	Raised cosine	Raised cosine
Interpol. rate	x 4	x 4	x 8	x 16
Decim. rate	x 2	x 4	x 8	x 16
Rolloff factor	0.22	0.115	0.115	0.115/0.115
# of Taps	129	129	129	129/129
Sampling freq. (MHz)	64	64	64	64/8
Cutoff freq. (MHz)	2.8	3.5	2	2/1.2
Coeff. width (bits)	16	16	16	16/16

Ⅲ. Implementation of Digital IF Transceiver

In this section, we introduce the implemented reconfigurable dual mode base station termed ReMO (Reconfigurable Mobile Convergence for a two-mode access system) briefly. In addition, we discuss about the presented Digital IF transceiver including PCB assembly module. The ReMO system, which incorporates a heterodyne architecture, was developed to verify the feasibility of applying SDR technology to a mobile communication base station reconfigurable to a HSDPA system based on WCDMA (Wideband Code Division Multiple Access) technology and to an IEEE 802.16d WiMAX system based on OFDM technology[14], [15]. The ReMO system uses SDR technologies in which modems and other functional blocks can be reconfigured easily, with software downloaded onto identical hardware platforms [16].

The ReMO based on SDR technology was developed adopting the open hardware platform architecture of Advanced Telecom Computer Architecture (ATCA). Therefore, all the functional hardware blocks and components of the ReMO system, including the implemented Digital IF transceiver board, termed the Analog Digital Conversion Block (ADCB), follow the ATCA architecture. The Digital Processing Sub-system (DPS) rack, which manages the digital signal processing function and external network interfaces of the ReMO, is shown in Fig. 3 as the board marked with a dotted red line.

The implemented ADCB hardware board is represented in Fig. 4. It includes two Digital IF Conversion Modules (DICMs), an intelligent platform management controller module (IPMC), and a power module. The DICM module is mounted on an ADCB board as a daughter board for easy troubleshooting. The ADCB board can adopt two DICMs to support a two-path transmitter and receiver diversity. One DICM module on an ADCB board can process two channels simultaneously for one (A or B) diversity path. In the DICM, we used a commercial DAC chip, the AD9777, made by Analog Devices, which converts a digital signal to

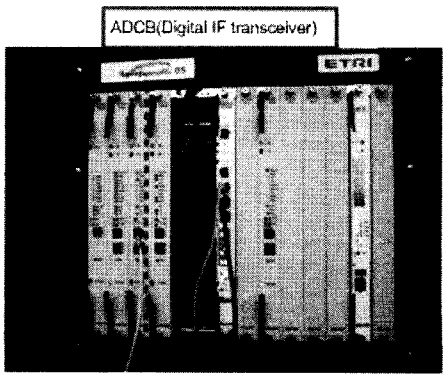

Fig. 3. DPS rack of ReMO system

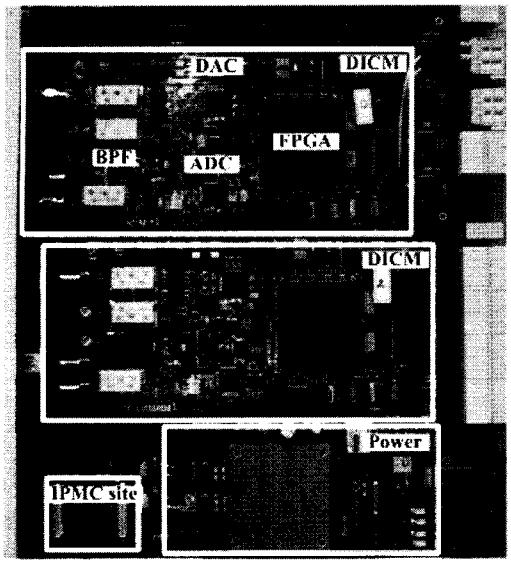

Fig. 4. Appearance of the ADCB board hardware

an analog signal [17]. The chip has x2/x4/x8 interpolation functionality internally and has an output sample speed as high as 400 Msps. In the HSDPA, the DAC is operating at a data rate of 245.76 (4 x 61.44) MHz and uses two half-band filters to achieve x 4 interpolation function internally. Finally, it outputs an IF analog signal of 80 MHz after being up-converted by 61.44 MHz via DCQM. The DAC is operating at a data rate of 256 (4 x 64) MHz for the WiMAX. In addition, we used a commercial off-the-shelf ADC chip, the AD6645, made by Analog Devices, which converts an analog signal to a digital signal [18]. The sampling clock for ADC and DAC on a DICM is provided by the PLL module on board, and alternated to others according to the configured system profiles and specific system clock speed. We selected an ADC sampling frequency of 61.44 MHz, i.e., interpolated by 16 with a fundamental frequency of 3.84 MHz for the HSDPA system. When ReMO is reconfigured to the WiMAX system, the transceiver is operating with a 64 MHz ADC sampling clock rate, i.e., interpolated by 8 with a fundamental frequency of 7 MHz * 8/7 = 8 MHz incorporate with WiMAX 7 MHz profile. In addition, the demodulated signal is then down-sampled by 4 through a decimation filter adapted to each I and Q path. The adopted ADC satisfies both of these sampling clock rates, because it has a maximum 80 Msps sampling rate.

Generally, for a Digital IF transceiver, a DAC data sample rate must be considered in selecting the IF frequency. Because the adopted DAC can operate at a conversion rate of 400 Msps, theoretically, we can boost the IF frequency up to 100 MHz by the Nyquist sampling criteria. In the ReMO system, we selected an IF frequency of 80 MHz in both the HSDPA and WiMAX.

The overall digital signal processing for the Digital IF block is implemented with a Field Programmable Gate Array (FPGA) chip, the Vertex II series XC2VP70 (manufactured by Xilinx Inc.) [19]. This FPGA chip provides interpolation filtering, a digitally programmable NCO, DCQM, FA combining for a digital up-conversion process, and FA channelization, demodulation, and decimation filtering for down-conversion. The FPGA also provides a high-speed serial communication interface named Multi Gigabit Transceiver (MGT) between the ADCB board and the BPB modem board. Because MGT technology uses the digital low voltage differential signaling (LVDS) format, it is robust against noise and crosstalk between the physical signal lines. Therefore, it can provide a reliable high-speed communication interface. In ReMO, the speed of this serial communication is as high as 614.4 Mbps and 1.2288 Gbps for a HSDPA downlink and uplink transmission respectively, and 640 Mbps for both WiMAX links. The small sized IPMC module on an ADCB board provides management functions, such as reset sequence and power supply management. The IPMC is located on every blade of the ReMO system, following ATCA standards, and supports a Reconfigurable Base Station Manager (RBSM) to monitor each device of the blade over the IPM Bus. Here, the RBSM is a middleware platform that performs reconfiguration, management, and operation of the overall ReMO systems.

Ⅳ. Test Results of the Digital IF Transceiver

In this section, we examine the experimental results of the presented Digital IF transceiver board. We conducted the performance test for a downlink by re-

configuring to other system profiles sequentially. The aim of the test was to identify the reconfigurability to other system profiles on the same hardware platform and to certify that the measured performance of the transceiver achieves the criteria that each standard demands.

4.1 The test environments

The Fig. 5 represents the overall test configuration for downlink. The interface between the BPB and the ADCB is a fabric interface, which is one of the five ATCA backplane interfaces. The ADCB up-converts the digital baseband modem signal from a Baseband Processing Block (BPB) to an IF analog signal of 80 MHz. This analog IF signal was measured using Vector Signal Analyzer (VSA) equipment commercially available. The VSA measures the frequency response spectrum and constellation of the downlink IF transceiver output signal and provides the precise EVM value.

The system clock for the ADCB was a Phase Locked Loop (PLL) clock locked to the 10 MHz reference clock provided by the Clock Generation and Distribution Block (CGDB) board. The CGDB board generates and distributes the required clock signal for overall ReMO systems. The reconfiguration to the HSDPA system and to three WiMAX profiles was accomplished by downloading the corresponding FPGA configuration file for each system through a RBSM control. In addition, the reconfiguration function was verified by examining the frequency response spectrum and constellation of the downlink IF transceiver output signal. Table 2 shows the major input signal parameters for each system to verify the transceiver performance.

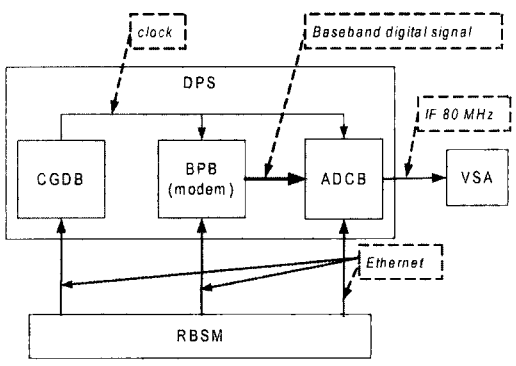

Fig. 5. Overall test configurations

Table 2. Input test signal parameters

Profile	HSDPA	WiMAX		
		7 MHz	3.5 MHz	1.75 MHz
Duplexing	FDD	FDD	FDD	FDD
Modulation & Coding	16 QAM TC 3/4	64 QAM RS-CC 3/4		
Frame Duration (ms)	2	5	5	8
CP	-	1/8		
N_FFT	-	256		
N_used	-	200		
Channel	HS-PDSCH	-	-	-

For the HSDPA transmitter test, the generated signal at the BPB entering the ADCB through the MGT is a signal having 2 ms frame duration, a turbo-coded 16 QAM modulated signal, i.e., 16 QAM-TC 3/4. For WiMAX, the generated signal at the BPB is an OFDM signal having 5 ms frame duration, a code rate of 3/4 Reed-Solomon convolutional-coded and 64 QAM modulated signal, i.e., 64 QAM-3/4 modulation and coding scheme (MCS) with a different signal bandwidth according to each profile. Each profile of the WiMAX system had the same FFT size but different sub-carrier spacing according to the signal bandwidth of each profile. All input signals were 64 QAM modulated.

The considered performance criterion was EVM, which is the most widely used modulation quality metric in digital communications systems. EVM is the root-mean-square (rms) value of the error vector over time at the instants of the symbol clock transitions [20]. By convention, EVM is usually normalized to the outermost symbol magnitude at the symbol times and expressed as a percentage, as shown in the following equation:

$$EVM = \left(\frac{rms \quad error \quad vector}{outermost \quad symbol \quad magnitude} \right) \times 100\% \tag{5}$$

Moreover, EVM may be normalized to the square root of the average symbol power. In this way, EVM can be related to the SNR:

$$SNR = -20 * \log\left(\frac{EVM}{100\%} \right) \tag{6}$$

4.2 Test results on HSDPA performance

To verify reconfigurability to the HSDPA system according to the RBSM mode change commands, we measured the spectrum and constellation of the downlink IF output using VSA equipment that is commercially available. The measured EVM value of the signal is shown in Fig. 6 as -39.2 dB.

The minimum requirement for transmit modulation is that the EVM shall not be worse than 12.5 %rms when the base station is transmitting a composite signal that includes 16 QAM modulation [21]. The EVM value of 12.5 %rms is evaluated to the SNR of 18.1 dB according to Eq. (6). Considering the estimated SNR loss of 10 dB in the RF and an implementation margin of 5 dB, the output EVM value of the Digital IF transceiver should be larger than the SNR of 33.1 dB to meet the recommended criteria. As a result, the measured EVM value of -39.2 dB (SNR of 39.2 dB) satisfies the condition with a 6.1 dB margin.

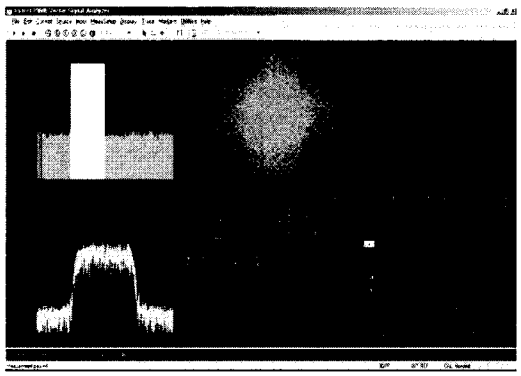

Fig. 6. Performance of the HSDPA (EVM = -39.2 dB)

4.3 Test results on WiMAX performance

We also conducted the same test for the WiMAX systems. The test results of the three WiMAX profiles are presented in order in Figs. 7, 8, and 9. In a WiMAX system, the term Relative Constellation Error (RCE) is usually used rather than EVM, though these terms are equivalent. As can be seen in Figs. 7 through 9, a similar EVM value of less than -43 dB regardless of the operating WiMAX bandwidth profiles was obtained regardless of the operating WiMAX bandwidth profiles.

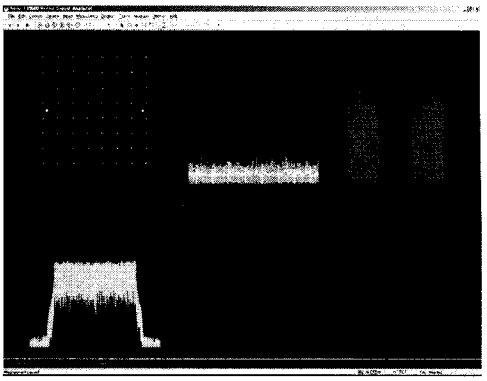

Fig. 7. Performance of the WiMAX 7 MHz profile (EVM = -43.2 dB)

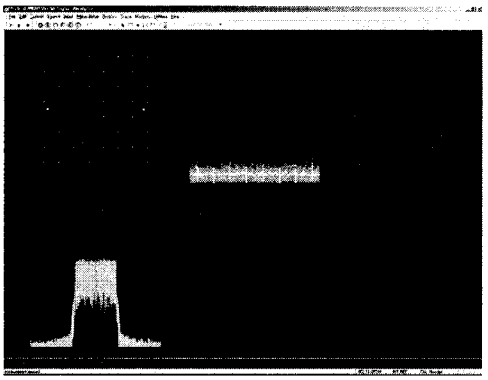

Fig. 8. Performance of the WiMAX 3.5 MHz profile (EVM = -44.1 dB)

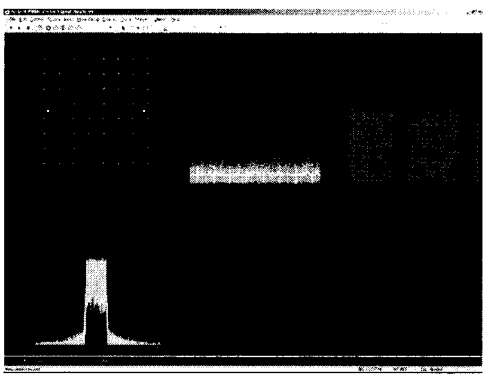

Fig. 9. Performance of the WiMAX 1.75 MHz profile (EVM = -43.6 dB)

The recommended allowed transmitter SNR performance of 64 QAM - 3/4 burst type MCS in [20] is less than -31 dB of EVM (and the same as 31 dB of RCE). This result indicates that the output EVM value of the Digital IF transceiver should be less than -40 dB to meet the recommended criteria considering the estimated 4 dB SNR loss of RF

and implementation margin of 5 dB. Additionally, the exact measured EVM values in this test were -43.2 dB, -44.1 dB, and -43.6 dB for the corresponding WiMAX 7 MHz, 3.5 MHz, and 1.75 MHz bandwidth profiles, respectively. Therefore, the measured EVM values of all three profiles satisfy the abovementioned condition with a 3 or 4 dB margin.

V. Conclusions

In this paper, we suggested the software radio architecture of the reconfigurable Digital IF transceiver and verified the feasibility by implementing the transceiver that can support the HSDPA system and three WiMAX profiles using SDR technologies. Verification was performed using off-the-shelf equipment to examine the spectrum and the constellation on an IF output. In addition, the developed transceiver was successfully reconfigured to other systems, satisfying the recommended performance criteria of all supported system profiles.

If the suggested SDR technology based transceiver architecture is applied to a mobile communication base station, especially in upcoming 4G systems with various bandwidth profiles, rapid deployment to the upgraded technology would be possible with low cost and time to market consistently.

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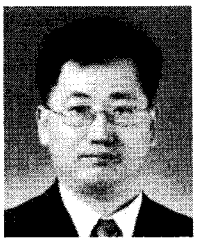

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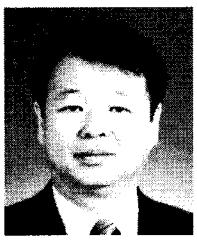
나 성 웅 (Sung Woong Ra) 종신회원



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<관심분야> 영상처리, 영상코딩, MPEG-IV, 화상회의 시스템