Characterization of Electrical Properties and Gating Effect of Single Wall Carbon Nanotube Field Effect Transistor

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We attempted to fabricate carbon nanotube field effect transistor (CNT-FET) using single walled carbon nanotube(SWNT) on the heavily doped Si substrate used as a bottom gate, source and drain electrode were fabricated by e-beam lithography on the 500 nm thick SiO_2 gate dielectric layer. We investigated electrical and physical properties of this CNT-FET using Scanning Probe Microscope(SPM) and conventional method based on tungsten probe tip technique. The gate length of CNT-FET was 600 nm and the diameter of identified SWNT was about 4 nm. We could observed gating effect and typical p-MOS property from the obtained V_G-I_{DS} curve. The threshold voltage of CNT-FET is about -4.6 V and transconductance is 47 nS. In the physical aspect, we could identified SWNT with phase mode of SPM which detecting phase shift by force gradient between cantilever tip and sample surface.

Keywords : CNT, SPM, Nanotube, CNT-FET

1. INTRODUCTION

The development of Silicon-based integrated devices as the key technology of microelectronics for the last 30 years has been kept pace with Moore's law. However, device shrinkage beyond 100 nm led to several technical problems as new limiting factors : Thermal dissipation, power consumption, electrical property fluctuation, leakage current, etc. As the metal line width become narrower, scattering at surface and too high current density deteriorate a frequency performance of device. In the lithography process, we need to develop a more accurate lithography technology. So the nano-scale dimension and ballistic property material is a necessary factor in the future device technology[1]. To overcome these physical limits, much techniques have been proposed as alternative technologies. There are two paradigm in nano-technology. First is a top-down approach. It is a realization of nano-scale structure from the bulk material by using conventional Silicon process technique. Double gate transistor or vertical gate transistor[2] are the example of top-down approach. In these structure, there are 2 or 3 channel region in 3 dimension, and it make easy to control the channel. Because of above technologies based on the Si process, it seems to be a leading technique of nano-technology. However unstable nano-scale lithography and high cost were pointed out as a limit of development. Another is a bottom-up approach. It means nano-device fabricating out of nano-scale material such as semiconducting DNA[3], various nano-wire and Carbon nanotube(CNT). Especially, CNT has been widely studied in a characterization and process[4-7] as the promising candidate to replace silicon-based MOS due to their high thermal conductivity, ballistic conductance, and type conversion from p-type to n-type by doping process [8-10]. However, the use of CNTs for nanoelectronics has so far been limited, because of difficulties in purifying and positioning semiconducting CNTs where we want. In spite of these problems in process, intensive researches were performed for CNT-FET. It has a similar structure with conventional Si MOS-FET. But CNT is used as a conducting channel under electric field induced

by gate bias instead of Si in conventional MOS-FET. Because the dimension of CNT is nano-scale, area of device can be reduced outstandingly. So, it is very advantageous for the ultra-high density integrated circuit compare to the Si-based devices. Also, its ballistic property can decrease a wire resistance and scattering, if it is used as conducting line. But, to realize such a excellent device, we have to overcome some problems in fabrication process. In physical aspect, difficulty in controlling a chirality which determining semiconducting or metallic property of CNT and purifying semiconducting CNT from compound of CNT and carbon material is a problem to solve. In mass product aspect, positioning a CNT where we want is very important. The present methods are dispersing, Atomic Force Microscope(AFM) manipulation or direct CNT growth. But these method has a very low yield. In spite of these disadvantages, many groups intensively research about the device using CNT and almost problems will be solves in near future. To actualize a new advanced CNT device, the wide comprehension and research about physical characteristics have to be preceded. In particular, fabrication of CNT-FET structure, measurement and analysis are necessary for the improvement of CNT-FET.

In this work, we focused on the device fabricating and characterization of electrical property of field effect transistor using SWNT. These researches and results will be helpful to understand in device property aspect of CNT-FET which is a stronger candidate for the future device.

2. EXPERIMENTS

The CNT-FET which used in this experiment was fabricated with a follow procedure. The diagrams of process flow are depicted in Fig. 1. The heavily doped p-type(100) Si wafer with 0.018 Ωcm that was employed as a back gate. The gate oxide(500 nm) SiO_2 was thermally grown on Si substrate. Source and drain contact pad were patterned by lithography, and the lift-off method of Au(2000 Å)/Ti(100 Å) layer. And then, we fabricated coordinate system to find a exact location of the CNT by E-beam lithography.

The coordinate system consists of fine dots which were patterned by lift-off of Au(300 Å) /Ti(100 Å), diameter of dot is 100 nm and spacing between dots is 2 um. Single-walled nanotubes produced by laser ablation(ILJIN Nanotech, Korea) were dispersed from a 1,2-dicholoroethane solution by spinning onto the substrate after sonication. Van der Waals force between CNTs make CNT get tangled. Since, the sonication of CNT suspension is necessary. Source/drain electrodes were formed by E-beam lithography based on the coordinate system after we confirmed the location of CNTs by SEM or SPM. To reduce the contact resistance between CNT and metal contact, rapid thermal annealing(RTA) at 600~800 °C for 30s in a N_2 or Ar gas were performed. Figure 2 shows the image of fabricated CNT-FET.

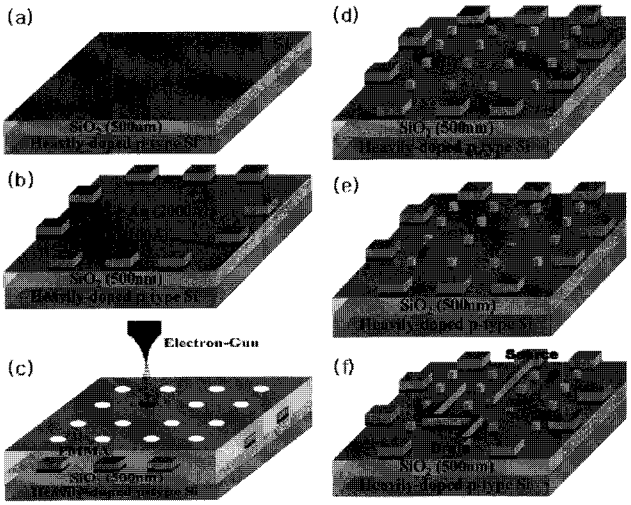

Fig. 1. (a) Thermally grown SiO_2 on Si wafer (b) Patterning of metal pad (c) nano-dots patterning using E-beam lithography (d) coordinate system (e) Dispersion of CNT on oxidized Si wafer (f) Patterning of source and drain electrodes.

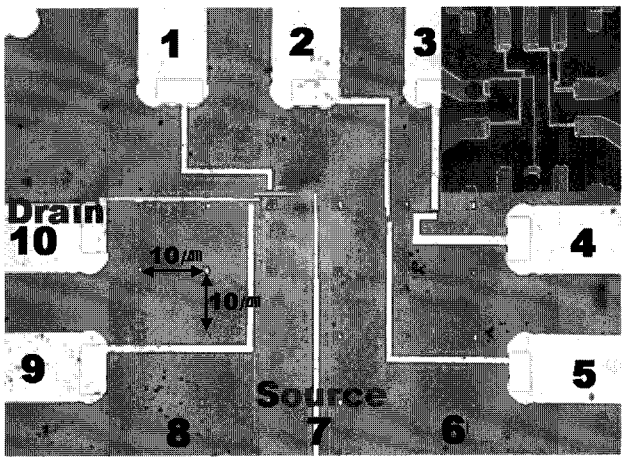

Fig. 2. Microscope image of fabricated CNT-FET.

We used a SPM to analyze a physical dimension and properties of CNT-FET. In phase shift image in Dynamic Force Microscope(DFM), we could verify the existence of SWNT clearly. It is somewhat difficult to observe a

SWNT in topology image. By graphical analysis, exact dimension of device was known. Figure 3 shows a phase shift image and cross-sectional profile. To characterize electrical properties of CNT-FET, V_G-I_{DS} curve were measure with V_G sweeping from 0V to -8 V with fixed -0.5 V V_{DS}. From the curve, we could verify the gate effect of device. Also, V_{DS}-I_{DS} curve were obtained with V_{DS} sweeping from 0V to -6 V under various V_G, namely 0 V, -0.5 V, -1 V, -1,5 V, -2 V, -2.5 V, -3 V.

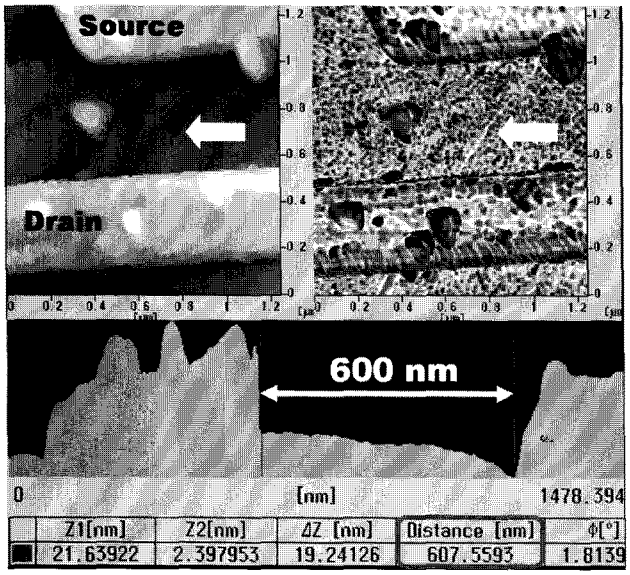

Fig. 3. SPM images and analyzed profiles of CNT-FET.

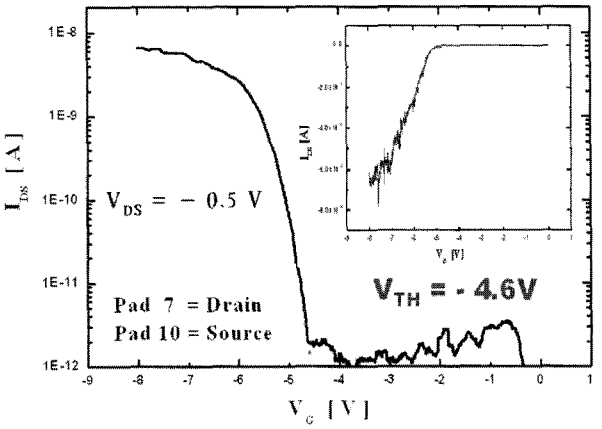

Fig. 4. Transfer characteristic for a p-type CNT-FET.

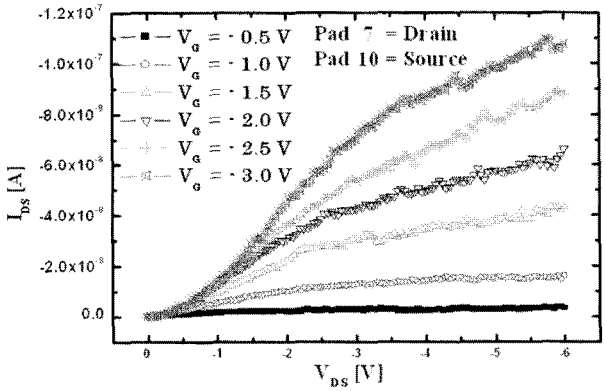

Fig. 5. V_{DS}-I_{DS} curve of CNT-FET.

3. RESULTS

We got the topology image and phase shift image of CNT-FET simultaneously using SPM. From these images, we could know the exact dimension and shape of device. Distance from source to drain electrode had been calculated from image analysis. in topology image, it is nor clear to identify the SWNT lying between source and drain. On the contrary, in phase shift image, we could easily observe a SWNT. Bright line in phase shift image of Fig. 3 is a SWNT. When we scan with a DFM mode of SPM, the vibrating frequency and phase of cantilever change with a different material. Image converting from phase variation is a phase shift image. From the profile between source and drain, we could know that the channel length of CNT-FET is 600 nm.

V_G-I_{DS} curve and V_{DS}-I_{DS} curve of device showed a typical p-MOS characteristics. These are coincident with results of early reported research. Figure 4 shows a transfer characteristic if a CNT-FET.

At V_G = - 4.6, I_{DS} increased suddenly. This phenomenon means that SWNT become a channel which current flows. From the V_{DS}-I_{DS} curve, we could know that fabricated CNT-FET has a typical p-MOS property and its threshold voltage(V_{TH}) is about -4.6 V. Current I_{DS} increase linearly as V_{DS} increase, and become saturated with a high V_{DS}. Since the I_{DS} can be controlled by back gate voltage(V_G) below 0 V, CNT-FET is a enhancement mode p-type FET. The transconductance was calculated. $g_m = \Delta I_{DS} / \Delta V_G$ = 47[nS]. And On/Off ratio was almost 10^4. When we compare these results with those of another research, it is clear that the thickness of a gate oxide greatly influence to a trans- conductance which means a gating effect of a device. Figure 6 shows a comparison of several result of relation between oxide thickness and transconductance[11-14]. Another key factor of effective device using CNT is a contact resistance between CNT and metal electrode. The On-resistance of it was 54 MΩ. It is high value. As a result, to fabricate a more effective

CNT-FET, we need to reduce a thickness of gate oxide without high leakage current and to decrease a contact resistance using proper material or additional RTA process.

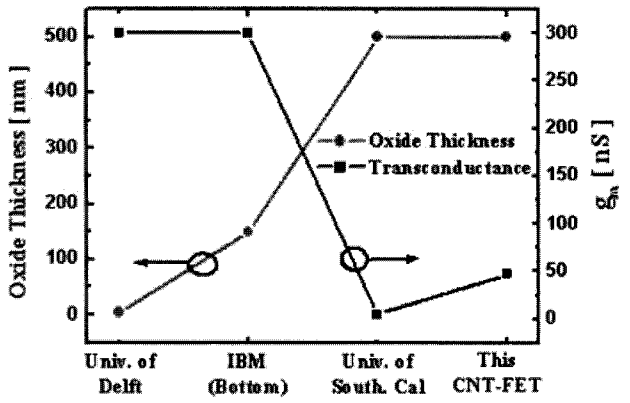

Fig. 6. Relation between transconductance and oxide thickness.

4.CONCLUSION

We fabricated nano-size field effect transistor using SWNT. In process, E-beam lithography was employed to make a nano-dot coordinate system. CNT-FET operated normally and shows typical p-MOS behavior. Also, we observed gate effect of it and its V_{TH} = - 4.6.

In conclusion, through this work, we obtained basis of fundamental technique for ultra high density memory using semiconducting carbon nanotube. Simultaneously we recognized some obstacle in fabrication. The control and locating of nano-size CNT was a main problem. But we expect that these problems would be solved with combining nano-technology and conventional Si processing.

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