Stepwise *Ni*-silicide Process for Parasitic Resistance Reduction for Silicon/metal Contact Junction

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The parasitic resistance is studied to silicon/metal contact junction for improving device performance and to lower contact/serial resistance silicide in natural sequence. In this paper constructs the stepwise *Ni* silicide process for parasitic resistance reduction for silicon/metal contact junction. We have investigated multi-step *Ni* silicide on *SiGe* substrate with stepwise annealing method as an alternative to compose more thermally reliable *Ni* silicide layer. Stepwise annealing for silicide formation is exposed to heating environment with 5 °C/sec for 10 seconds and a dwelling for both 10 and 30 seconds, and ramping-up and the dwelling was repeated until the final annealing temperature of 700 °C is achieved. Finally a direct comparison for single step and stepwise annealing process is obtained for 20 nm nickel silicide through stepwise annealing is 5.64 Ω/square at 600 °C, and it is 42 % lower than that of as nickel sputtered. The proposed stepwise annealing for *Ni* silicidation can provide the least amount of *NiSi* at the interface of nickel silicide and silicon, and it provides lower resistance, higher thermal-stability, and superior morphology than other thermal treatment.

Keywords : *Ni*-silicide, Sheet resistance, Stepwise annealing

1. INTRODUCTION

The parasitic resistance associated with the silicon/metal contact junction becomes one of the major concerns for improving device performance, and the search of lower contact/serial resistance silicide in natural sequence. *NiSi* has no adverse line-width dependence of sheet resistance, which was open a big problem in $TiSi_2$ at which the nucleation of *C*54-$TiSi_2$ could not occurred well enough at smaller line width[1-3]. The sheet resistance of the narrow line was found to even decrease because of the edge effect, and the silicon consumption during the silicidation is the smallest among *Ti*, *Co* and *Ni*[4,5]. This is suitable for ultra-shallow S/D junction formation for scaled CMOS. The mechanical stress of the nickel silicide film on silicon substrate is also the smallest. Contact resistance to *p*-type silicon, which was a problem for $TiSi_2$, is the smallest due to its lowest barrier height, and that to *n*-type silicon was also small. Bridging failure between the gate and source/drain hardly occurs for the nickel silicide due to its reaction mechanism – nickel is the diffusion element, while silicon is diffusion element for $TiSi_2$ and *CoSi*, cobalt is diffusion specimen for Co_2Si and $CoSi_2$ [4].

On the other hand the major concern for nickel silicide is its low formation temperature. In fact the maximum allowable process temperature is known as 700-750 °C[1,4,6]. Once the processing temperature exceed 800 °C, *NiSi* will transform into the $NiSi_2$ phase, and this maximum allowable process temperature goes down as the thickness of deposited nickel film goes thinner[6]. It is believed that the *Ni-Si* system, the metal rich Ni_2Si forms at approximately 200 °C. Upon further heat treatment the monosilicide, *NiSi* forms at about 350 °C and the disilicide, $NiSi_2$ at about 750 °C. Annealing temperature of silicide formation varies from a few hundred °C up to above 1000 °C depending on annealing time and sample type[7,8]. Due to the fact the phase transition, however, is related with annealing temperature, nickel silicide in some research was performed about 350 °C for 30 minutes[9,10].

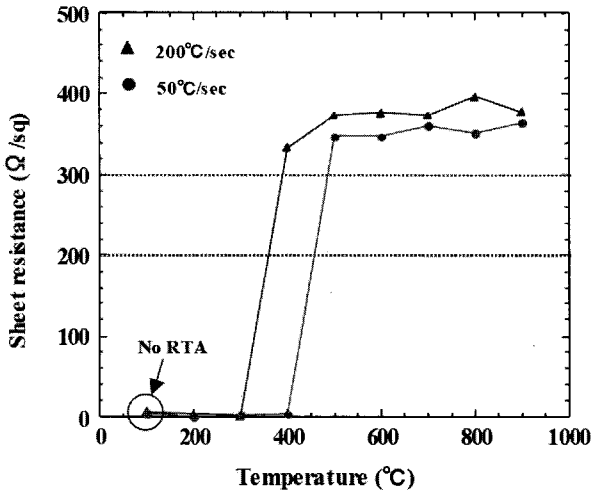

Fig. 1. Sheet resistance with the single ramping temperature of both 50 ℃ and 200 ℃.

Since *Ni* silicide has many advantages such as low processing temperature, low contact resistance, smooth surface and interface, simple processing, no risk for bridging (*Ni* is diffusion specimen) and no line width dependence. *Ni* silicide is one of the promising candidates for future silicide. On the other hand, low thermal stability of thinner nickel film deposited sample, formation of high resistivity $NiSi_2$ phase at relatively low temperature and low morphological stability (thermal agglomeration which is believed also related with *NiSi* phase) can cause a problem. If the $NiSi_2$ phase is unavoidable, we shall find a way to compose *NiSi* and $NiSi_2$ mixed structure for higher thermal stability with controlling the amount of $NiSi_2$ as little as possible up to the highest temperature region available. With this composite method disadvantages of nickel silicide described above can be avoided.

In this paper, we have investigated multi-step *Ni* silicide *SiGe* with stepwise annealing method as an alternative to compose more thermally reliable nickel silicide layer. Conventional RTA annealing method for nickel silicide formation is briefly reviewed in Section II, and stepwise annealing process is followed in Section III. Then, the comparison between a single step annealing and the stepwise annealing and the conclusion will be provided in Section VI and V, respectively.

2. CONVENTIONAL RTA METHOD FOR NICKEL SILICIDE FORMATION

In advance to performing stepwise annealing process, a conventionally used RTA annealing process with the temperature trace of a single ramp rate (both 50 and 200 ℃/sec) and annealing for 30 minutes is applied to thin *Ni* film on silicon substrate to form a *Ni* silicide. Once (001) silicon substrates, cleaned with 1 % HF solution, are prepared, 400 Å of helicon RF sputtered *Ni* is deposited, and the sample are loaded RTA chamber immediately to minimize oxidation of the sputtered *Ni* surface. Varying the highest temperature for annealing from 100 to 900 ℃ with 100 ℃ steps, the sheet resistance is measured. The measured sheet resistance according to the ramping and the annealing temperature is shown in Fig. 1. It is observed that the fast ramped-up sample shows higher sheet resistance than slowly ramped-up sample. The higher sheet resistance is speculated that the thermal agglomeration of *Ni* molecules since the thermal agglomeration of nickel silicide is known to be higher than 800 ℃. For convincing our speculation of thermal agglomeration, two difference SEM images of samples, annealed at 300 and 400 ℃ with 200 ℃ ramping temperature. In Fig. 2, the sample annealed at 300 ℃ has fine surface morphology and lower sheet resistance than the other. For this reason, we have decided to investigate stepwise *Ni* silicide process to minimize a potential thermal agglomeration for parasitic resistance reduction for silicon/metal contact junction.

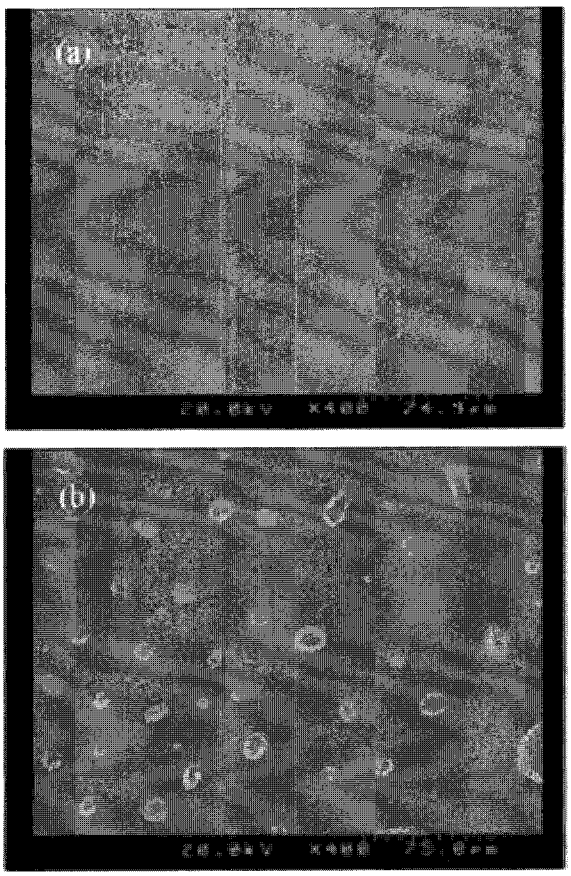

Fig. 2. SEM sample images annealed at (a) 300 ℃ and (b) 400 ℃ with 200 ℃/sec ramped. The sample annealed at 300 ℃ shows smoother surface morphology, and it corresponds to the lower sheet resistance after annealing.

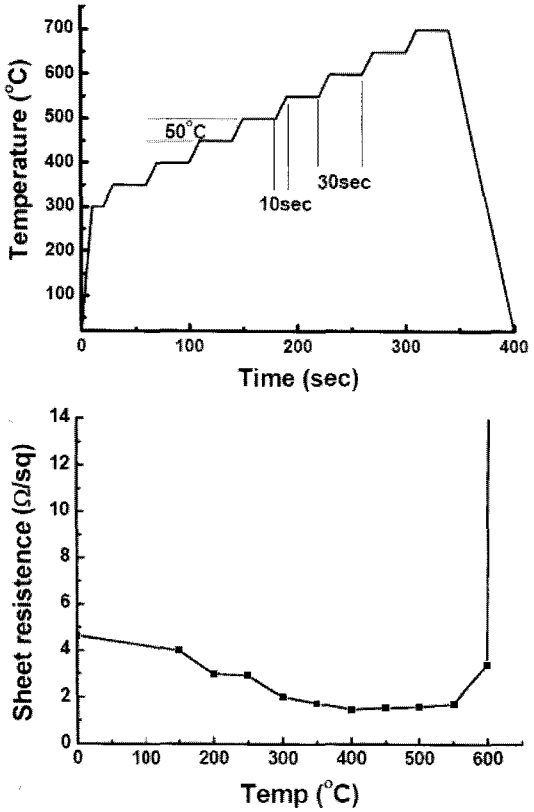

Fig. 3. Temperature trace for stepwise annealing with immediate cooling (top) and the corresponding sheet resistance of composed *Ni* silicide film (bottom).

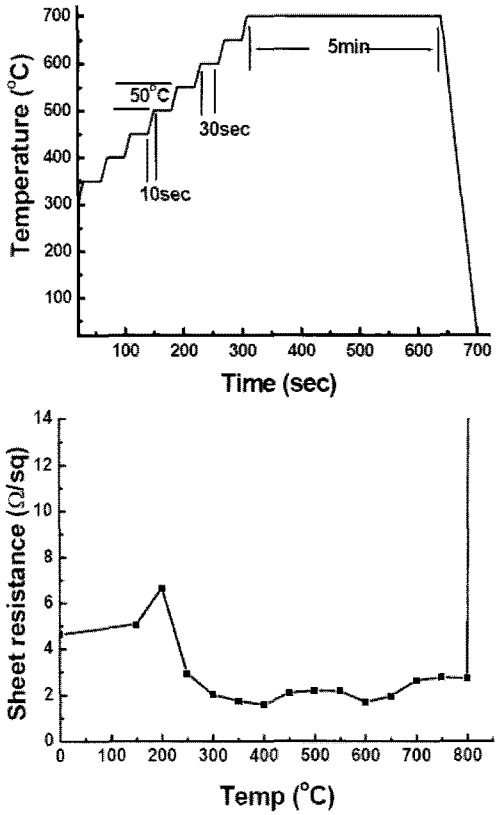

Fig. 4. Temperature trace for stepwise annealing with extended annealing at a highest temperature (top) and the corresponding sheet resistance of composed *Ni* silicide film(bottom).

3. STEPWISE ANNEALING FOR SILICIDE FORMATION

In this section, we demonstrate a stepwise annealing method unlikely with a conventional single ramping step annealing for *Ni* silicide formation. Substrates prepared in the same way described in the previous section are exposed to the heating environment with 5 °C/sec for 10 seconds and a dwelling for 30 seconds, and the ramping-up and the dwelling was repeated until the final annealing temperature of 700 °C is achieved. Once the annealing temperature of 700 °C is reached, we have compared the sheet resistance of the samples of one with annealing period of 30 seconds at 700 °C and without sustaining period. Figure 3 and 4 shows stepwise annealing temperature profile and the measured sheet resistance of the two sample; Fig. 3 is for the immediate cooling and Fig. 4 is for the 5 minutes annealing.

The sheet resistance in Fig. 3 shows a good sheet resistance profile once it reaches to 400 °C and presents a good stability in the sheet resistance along with the temperature variation up to 550 °C. Figure 4 looks a relatively unstable sheet resistance profile in that temperature window, but it is more stable in the higher temperature range between 600 to 800 °C. From the Fig. 3 and 4, it is speculated that the Ni_2Si is enabled around 200 °C, *NiSi* is dominant between the temperature range of 400 and 600 °C, and $NiSi_2$ is formed above 700 °C. The lowest sheet resistance obtained for the *Ni* silicide with 40 nm thick nickel film is 1.57 Ω/square at 400 °C, which show the 24 % of sheet resistances compared with the deposited *Ni* film when the maximum temperature is hold for some time.

A further investigation for increased temperature of 800 and 900 °C is also performed to cross check out speculations on the sheet resistance according to the temperature variation. Through the SEM measurement shown in Fig. 5, it is found that the surface of composed nickel silicide is smooth up to the annealing temperature of 800 °C, while the agglomeration on surface appears at 900 °C. Therefore, stepwise annealing method with an extended maximum temperature showed the *Ni* silicide with lower resistance and higher thermal stability. Employing stepwise RTA, good quality of *Ni* silicide was achieved even in elevated temperature. We have tried to investigate the mechanism for the elevated temperature through XRD measurement as well as microscopic image; however, no clear functional mechanism related to this temperature has found yet, and this remains as a future work.

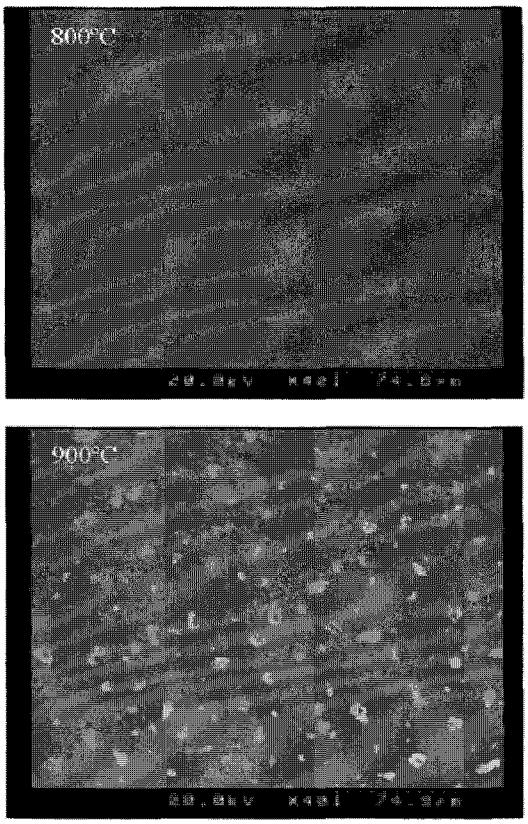

Fig. 5. SEM image of *Ni* silicide surface annealed at 800 and 900 °C.

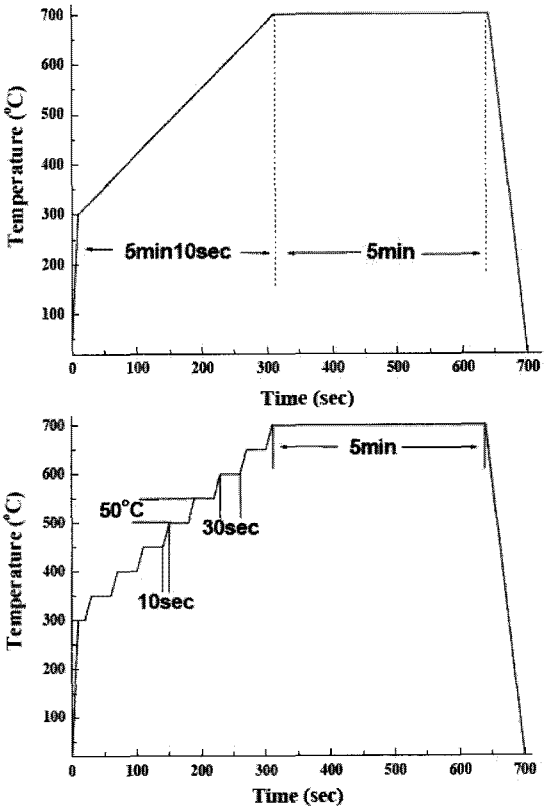

Fig. 6. Temperature traces of (a) the single step annealing and (b) the proposed stepwise annealing process.

4. A DIRECT COMPARISON OF SINGLE STEP AND STEPWISE ANNEALING PROCESS

In order to confirm the validity of the proposed stepwise annealing, a direct comparison of the single step and stepwise annealing process is compared with the same temperature ramping-up rate and the same dwelling time at 700 °C. The sheet resistance and the surface morphology are examined. Figure 6 depicts the annealing temperature profile of the single step annealing and stepwise annealing process, respectively.

The hypothesis behind is that the stepwise temperature holds of 30 seconds while the process temperature reaches to the final annealing temperature if there exists any diversity in the two samples. Once the silicide process is performed on the 40 nm thick nickel sputtered samples, the surface morphology, first of all, is compared using optical micrograph as presented in Fig. 7. The surface of the stepwise annealed sample is clear as a mirror, but the single step annealed sample looks like nickel begins to gathering together, as similar to the starting of the thermal agglomeration.

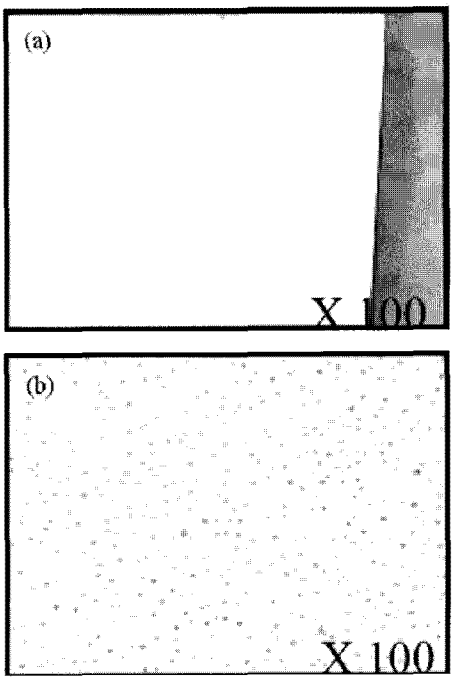

Fig. 7. Optical micrograph of nickel silicide performed with (a) the single step annealing and (b) the proposed stepwise annealing process.

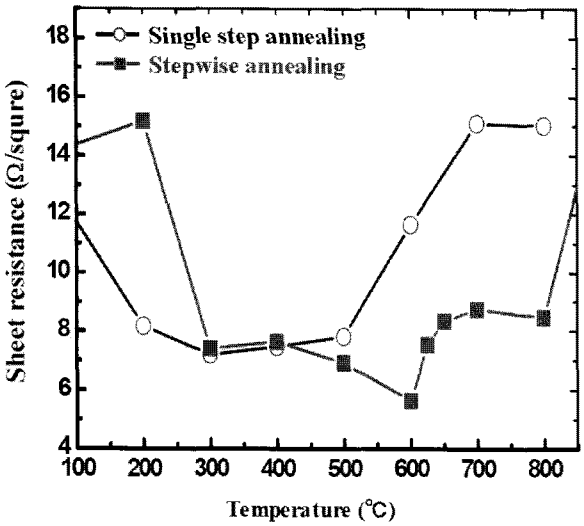

Fig. 8. A comparison of the sheet resistances of the 20nm thickness nickel silicide.

To examine the difference of the sheet resistance of nickel silicide, 20 nm of nickel sputtered samples are additionally prepared. As shown in Fig. 8, the sheet resistance processed with stepwise annealing process is lower than the single step annealing in the higher range of temperature. The lowest sheet resistance obtained from 20 nm nickel silicide through stepwise annealing is 5.64 Ω/square at 600 °C, and it is 42 % lower than that of as nickel sputtered.

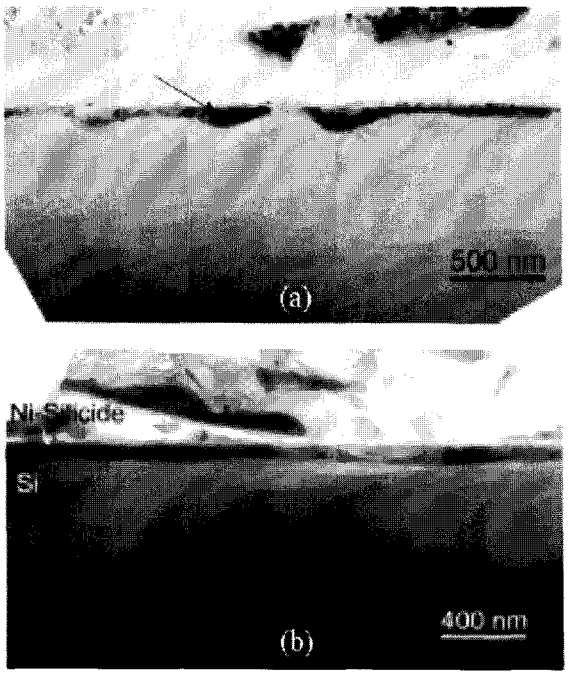

Fig. 9. TEM images of nickel silicide formed at 700 °C with (a) the single step annealing and (b) the proposed stepwise annealing process.

It is suspected that the single step annealed nickel silicide has a tendency to transit its phase to $NiSi_2$ at lower temperature. Also, there is no resistance incensement at the Ni_2Si phase transition region (below 200 °C) for single step annealed sample. On the other hand, stepwise annealed sample has Ni_2Si phase transition region even the thickness of deposited nickel is as thin as 20 nm. To prove this hypothesis, we have attempted the stepwise annealing on various substrate including poly-silicon, arsenic implanted silicon, silicon-on-insulator (*SOI*), arsenic implanted *SOI*, *SiGe* and arsenic implanted *SiGe*, and the proposed stepwise annealing process gives generally lower sheet resistance as well as thermally stable silicide formation.

To further investigate the interfacial phenomenon caused by the two annealing methods, cross sectional TEM (Hitachi HF-2000) measurement is employed. As presented in Fig. 9, TEM image acquired from the single step annealed silicide shows the gathered nickel with round shaped structure, and as a consequence the thickness of the silicide is not uniform (or shows discontinuity). On the other hand, stepwise annealed nickel silicide presents fairly uniform thickness and no significant evidence of discontinuity. This uniform thickness clearly supports the lower sheet resistance of stepwise annealed nickel silicide.

5. CONCLUSION

Due to the electrical and physical advantages, *Ni* silicide is one of the promising candidates for the future of silicide formation in semiconductor device fabrication. However, the thermal stability and low morphological stability could be a hindrance for realization in current device fabrication. It is believed that most of these problems are related with nickel silicide process condition, such as high temperature ramping-up, unstable Ni_2Si phase transition, abrupt phase change to $NiSi_2$ and etc. Among these considerations, unstable Ni_2Si phase transition could be alleviated with low process temperature (~350 °C) with prolonged annealing (~30 minutes). To prevent the abrupt phase change to $NiSi_2$, careful control of the maximum process temperature and the ramping-up rate are required. In this paper, the proposed stepwise annealing for *Ni* silicidation can provide the least amount of $TiSi_2$ at the interface of nickel silicide and silicon, and it provides lower resistance, higher thermal stability, and nice morphology than other thermal treatment. With some amount of dwelling while the temperature ramping-up, a time to phase change from *Ni* to *NiSi* at lower temperature region is secured, thus the stable composition and much uniform layer of *NiSi* are achieved.

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