Real Time Implementation of Active Power Filters for Harmonic Suppression and Reactive Power Compensation using dSPACE DS1104

Seethapathy Kumar† and B. Umamaheswari*

Abstract – In this paper, an Active Power Filter (APF) is implemented using a dSPACE DS1104 processor to compensate harmonics and reactive power produced by nonlinear load. The reference source current is computed based on the measurement of harmonics in the supply voltage and load current. A hysteresis based current controller has been implemented in a DSP processor for injecting the compensating current into the power system, so that APF allows suppression of the harmonics and reactive power component of load current, resulting in a supply current that is purely sinusoidal. Simulation and experimental results of the proposed APF to meet the IEEE-519 standards are presented.

Keywords: Active power filter, Harmonics and reactive power, Hysteresis controller.

1. Introduction

Advancements in power electronics have brought about significant improvement in the speed and torque control of electric drives. The usage of such devices for high frequency switching has introduced harmonics and reactive power in the power sector. The traces of harmonics in the current spectrum causes transformer overheating, circuit breaker nuisance, rotary machine vibration, voltage quality degradation, destruction of electric power components, torque pulsations, and resonance conditions with shunt capacitors and malfunctioning of medical facilities [1]. The nonlinear load in the utility consumes reactive power, causes mains voltage sags/swells, and transmission losses [2]. Therefore, an efficient solution for solving these pollution problems has become essential for power systems.

The method traditionally used for compensation of harmonics alone requires the addition of a passive filter that can be used for eliminating a certain range of frequencies from the power system. However, the passive filter performance is highly sensitive to variations in power system impedance and the frequency of the utility. There is an additional risk of series/parallel resonance. In recent years, many APF control algorithms have been developed to suppress both harmonics and reactive power [3-6]. In order to design an active filter, the instantaneous reactive power theory has often been applied as the main paradigm for calculating the required amount of compensation current [7]. The calculation process of this theory gives satisfactory results where three phase balanced sinusoidal currents flow on the source side, but a larger capacity is needed for the energy storage element to compensate the unbalanced active currents.

In this paper, an instantaneous reference source current is computed by measuring the source voltage and load current, which retains similar distortion in the applied voltage and in phase. Therefore, the nonlinear load behaves like a linear load, the reactive power is completely compensated, and unity power factor (UPF) operation is achieved. UPF operation also provides effective reduction of total harmonic detection. Based on this concept, the reference signals are generated to compensate either harmonic only or both harmonic and reactive power. A hysteresis based current controller is implemented to inject the compensating current to the power system so that the APF allows the actual source current to follow the reference source current.

The rest of the contents are organized as follows. In Section II, the overall structure of the APF is first introduced. Then, the estimation of reference current signals and the optimum selection of sampling frequency for the hysteresis current controller are discussed in Section III. Also, a real implementation of a prototype model using dSPACE 1104 with the TMS 320C30 DSP processor is introduced in Section IV and some simulation results of the proposed strategy are confirmed with experimental results given in Section V. Finally, some conclusions are made in Section VI.

2. System Description

Fig. 1 shows the customer generated harmonic and reactive power that is compensated by using Active Power Filter. It consists of a standard three phase voltage source inverter with a capacitor C_{dc} on the dc bus to maintain

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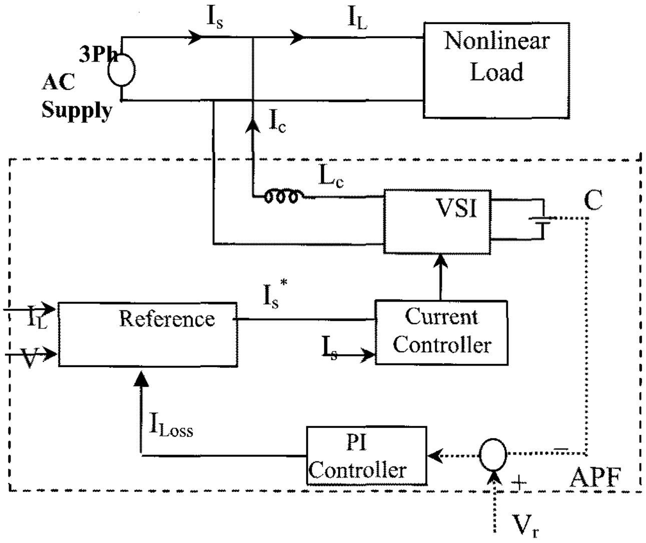


Fig. 1. Schematic Diagram of the Compensatory System.

constant dc voltage. The non-linear load is a voltage source inverter with a motor speed controller that draws a pulsating current from the ac source that is rich in harmonic and reactive power components.

Assume that the generated supply voltage (V_s) is purely sinusoidal. There are many non-linear loads in the industrial sector, distorting the main voltage. The APF also allows similar distortion in the compensated source current so that reactive power is completely compensated and UPF operation can be achieved. It might have a time lag or lead, or may be in phase with the voltage, depending on either harmonics only or both harmonics and reactive power compensation capability. Thus, the fundamental frequency component of the reference current will be equal to the fundamental frequency component of the load current (I_L) plus loss component I_{loss} for harmonic compensation, and $I_l\cos\Phi$ plus I_{loss} for both harmonic and reactive power compensation. The I_{loss} is estimated using the PI voltage controller of the dc bus.

Based on the above principle, the reference current can be estimated by measuring the supply voltage harmonics, fundamental load current, and their respective angles. The estimated reference currents and the actual source currents are then processed through the hysteresis current controller to obtain the switching signals for driving the APF.

3. Control Scheme

The control scheme of an APF consists of two major parts. The first is the estimation of an instantaneous reference source current to compensate either harmonic only or both harmonic and reactive power simultaneously. Secondly, the hysteresis current controller is used to generate compensation current as a similar distortion level present in the main voltage.

3.1 Instantaneous Reference Source Current Computation

The reference current is computed by measuring the supply voltage harmonics and the fundamental load current, which retains the same level of distortion as source voltage. Due to the similarity in shape, the current to voltage amplitude ratio is constant for all frequency components. This concept is used for the estimation of reference current for compensating both harmonics and reactive power simultaneously.

For the compensation of harmonics only, the ratio of fundamental current to fundamental voltage is scaled to (I_l/V_l) and rotated by appropriate angles, and then the harmonic components of the reference current can be written in the mathematical expression as

$$i_s^*(t) = \sum_{n=1}^{k}\left(\frac{I_1}{V_1}\right)V_n \sin(n\omega t + \theta_n + n(\phi_1 - \theta_1)) \tag{1}$$

$$I_1 = I_l + I_{Loss}, \text{for} \quad n = 1 \tag{2}$$

For the compensation of harmonics and reactive power simultaneously, both voltage and current should be of similar shape and in phase. The sum of fundamental and harmonic components makes the shape of the current equal to the relative level of harmonics in the voltage and in phase. As such, the reactive power is completely compensated. Hence, the estimated reference current to compensate both harmonic and reactive power is expressed in terms of fourier series as

$$i_s^*(t) = \sum_{n=1}^{k}\left(\frac{I_1}{V_1}\right)V_n \sin(n\omega t + \theta_n) \tag{3}$$

$$I_1 = I_l + I_{Loss}, \text{for} \quad n = 1 \tag{4}$$

3.2 Hysteresis Current Controller

The closed loop hysteresis current controller switches a voltage source inverter (VSI) such that the source current follows a set of references to meet the harmonic suppression and reactive power compensation of load currents. The basic block diagram of a hysteresis based closed loop current controller is shown in Fig. 2.

If the generated error signal e(t) exceeds the hysteresis upper limit, negative voltage is applied by the inverter to the injection inductor (L_i). This causes the current in the L_i to decrease. When the current reaches the lower hysteresis limit a positive voltage is applied, and when the current increases the same cycle repeats. Hence, the source current is forced to track the sine reference waveform within the desired hystresis band limit and the result of this comparison is used to control the switches in the inverter. With a digital controller, the sensed source current information is updated at the sampling frequency of the analogue to the digital converter (ADC). If this sampling frequency is too low there is a chance that the current will have exceeded the hysteresis limits by the time that the comparison is made. Figure 3 presents the results of a simulated inverter controller with two different sampling frequencies. The injected current is sampled at **2MHz** in (a) and at **200kHz** in (b). The centre solid line in each figure is the current reference and the jagged solid line is the inverter's current output. The high speed sampling of 2MHz gives very good results, and with only 0.5μs between samples the current will not get far outside the hysteresis limits. This can be compared with the case of 200 kHz sampling, where the current regularly exceeds up to 15-20% of the hysteresis limits. Therefore, acceptable current waveforms are achieved by choosing the optimum sampling frequency so that the overshoot is kept to 5-10% of hysteresis band, ΔI. This maintains the current ripple reasonably close to the design value for a traditional analogue hysteresis current controller. Therefore, optimum sampling frequency (f_{sample}) is needed to achieve an acceptable overshoot as a function of the injection inductance used and the voltage applied across the inductance is given by Equation (5) as [8].

$$f_{sample} = \frac{\frac{1}{2} V_{DC}}{Li} \frac{1}{\Delta_{iover}} \tag{5}$$

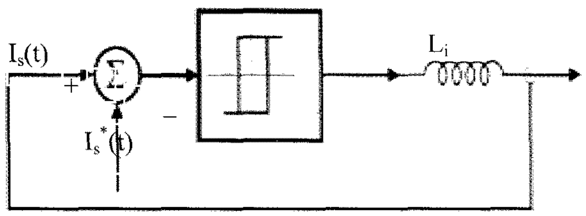


Fig. 2. Closed loop hysteresis current controller.

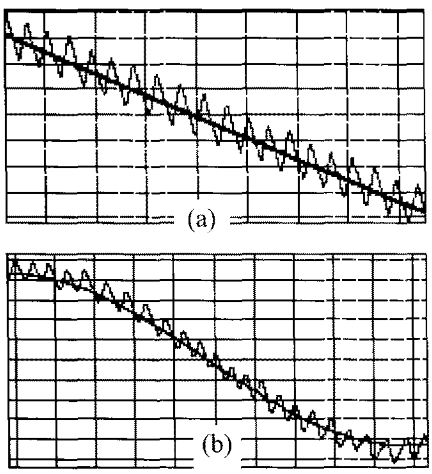


Fig. 3. Sampling Frequency at (a) 2MHZ (b) at 200KHZ.

4. Real Time Implementation of APF

The APF controller is built with a DSP add on card (dSPACE DS 1104), analog signal conditioning, and the host. This communicates with the Texas TMS320C30 32 bit floating point processor through its synchronous serial port with a 6.8MHz clock. A 12 bit serial ADC is used for the current feedback with a sampling time of 0.2msec. For experimental purposes, the supply voltage is stepped down to 80V and the IGBTs are 800V with 12Amp rating.

The APF consists of a single phase supply feeding a non-linear load, which is a three phase motor driven through a rectifier-inverter unit as shown in Figure 4. In case of three phase supply with balanced/unbalanced nonlinear loads, each phase must operate independently.

In order to implement the compensation control algorithm using dSPACE, multi-tasks are performed simultaneously

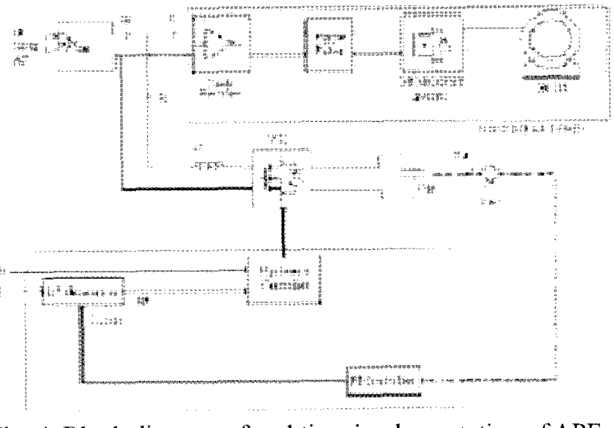


Fig. 4. Block diagram of real time implementation of APF.

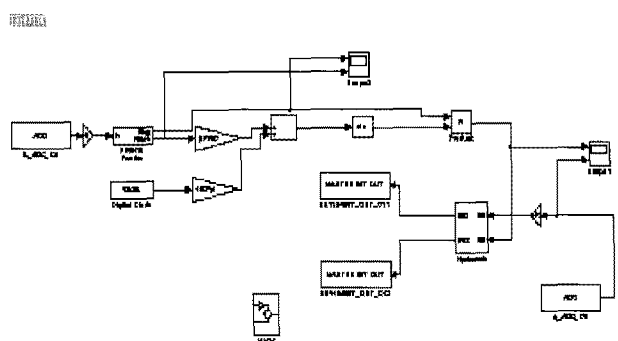


Fig. 5. Real time implementation of APF fed by VSI using dSPACE.

such as acquiring input signals, extraction of different frequency components, and generation of reference signal. Main voltage and load current are sampled at 0.2msec for one cycle on the occurrence of zero crossing interrupt. Using DFT, different frequency components of voltage and the fundamental component of the load current magnitude and angle are extracted. Based on this, the reference current is calculated as per equations (1-4) with a fundamental frequency of 50Hz and a magnitude of 5A. While sampling the input signals for the present cycle, reference currents generated from different frequency components of the previous cycle are outputted. Hence, there is a finite delay of slightly more than one cycle. The dc link voltage is regulated through a PI controller to calculate the loss component, to which is added the fundamental load current. It takes approximately 2.2 ms to calculate the various frequency components of the voltage, considering up to the 9[th] harmonics. Estimated reference current and sensed source current are then processed in the hysteresis controller to obtain the switching signals for application to the VSI after proper isolation and amplification. The three phase VSI injects compensating current into the network. A C_{dc} is used for energy storage, charged by the network and maintained at a constant DC voltage. The only real power used is due to losses in the inverter. Once the load current is fully compensated by APF,

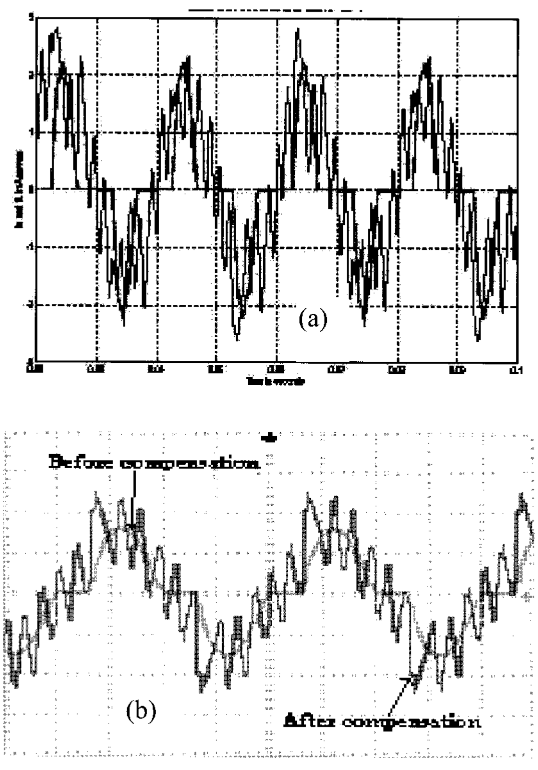


Fig. 6. Source current waveform before and after compensation (a) Simulation result at 0.2msec (b) Experimental results at 0.2msec.

the source current become sinusoidal with a hysteresis band of 0.1A due to the asynchronous nature of the hysteresis current controller. Figure 6 shows the ramp in the compensated source current. The maximum switching frequency is at 5 kHz with a magnitude of 0.9% of the 250Hz component of the compensating current. Figure 7 gives the typical graphical user interface when the APF is operating with the hysteresis controller. It has a switching frequency of 50Hz and machine speed of 500rpm.

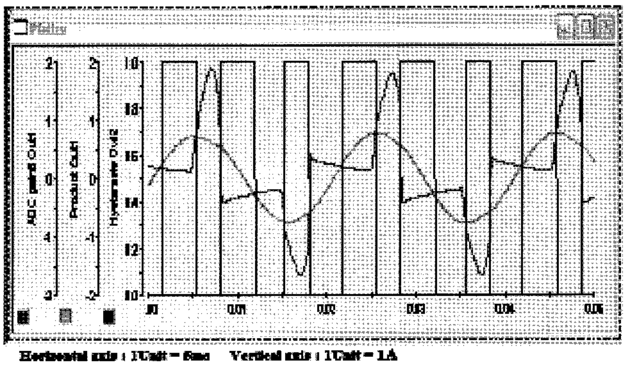


Fig. 7. Graphical display of the load current (I_L), compensated source current (I_c), and hysteresis controller switching signals.

5. Simulation and Experimental Results

The proposed APF control algorithm is simulated using Matlab combined with a power system block set and Simulink. Various simulation results are obtained for harmonics only as well as both harmonics and reactive power compensation, verified with experimental results. Parameters used for the experiments are given in Appendix. I.

Figure 8 depicts the simulation results of the source voltage (V_s), load current (I_L), compensated source current (I_c), and dc-link voltage (V_{dc}) waveforms under steady state for harmonic only compensation. It reveals that the post compensated mains voltage and currents are sinusoidal. However, in this case, the reactive power is not completely compensated due to the waveform difference between the main voltage and current. If the UPF operation is preferred, the load behaves as a linear load, and the resultant source current will have the same waveform as that of the supply voltage. But the reactive power compensation requires more current from 6.3 to 8.39 A, as compared to the harmonic only compensation case for similar load as shown in Figure 9.

Figure 10 presents the harmonic spectrum of source current waveforms, before and after harmonic and reactive power compensation at a 145watt load. It may be observed that the harmonics are drastically reduced in source current from 82.5% to 2.86%, which is well below the specific limit of 5-10% of standard IEEE-519. Some important

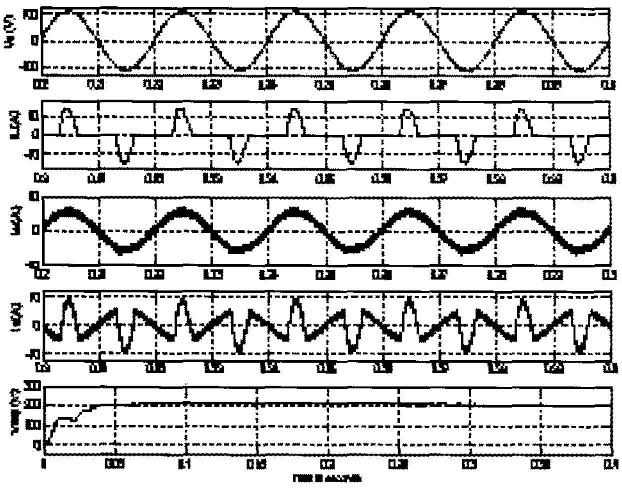


Fig. 8. Source voltage (V_s), load current (I_L), compensated source current (I_c), and dc-link voltage (V_{dc}) waveforms for harmonic only compensation.

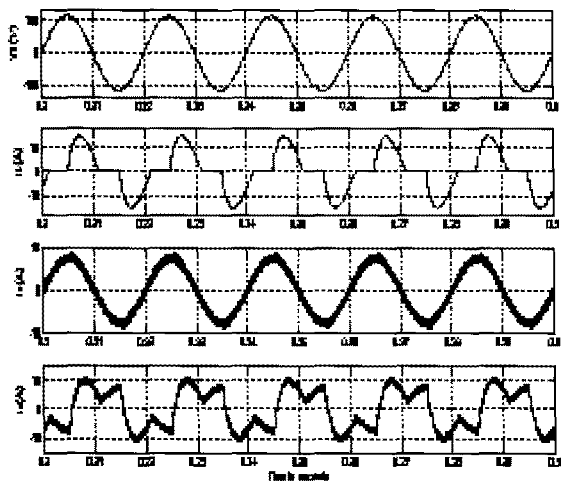


Fig. 9. Source voltage (V_s), load current (I_L), compensated source current (I_c), and dc-link voltage (V_{dc}) waveforms for harmonic suppression and reactive power compensation, with ideal mains.

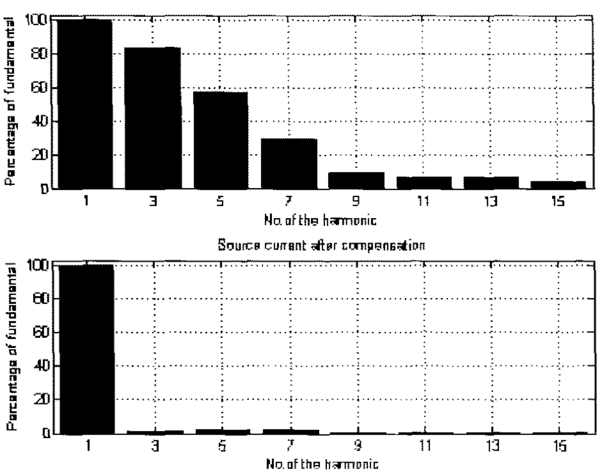


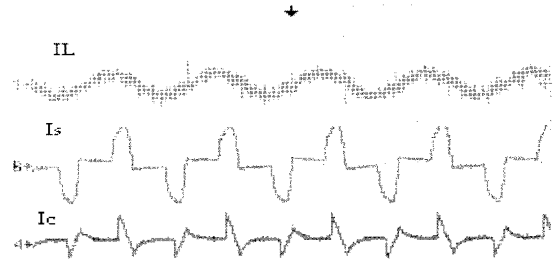
Fig. 10. Frequency spectrum of source current, before and after compensation.

Table 1. THD and power for either harmonic only and/or reactive power compensation.

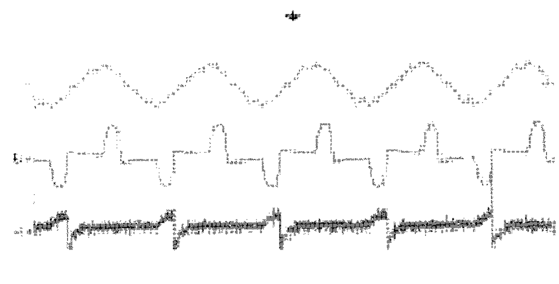
THD and power components	Before compensation	After compensation	
		Harmonics only	Harmonics and reactive power
THD %	96.53	1.34	8.65
Real power W	142	145	145
Reactive power VAR	21	20	0.8

parameters before and after compensation are presented in Table I. It is observed that for the case of harmonic compensation, harmonic power drawn from the source is reduced to zero. For both harmonics and the reactive power compensation case, reactive power is compensated completely, while only a part of the harmonic power is compensated by the APF.

Figure 11 shows the experimental results of the load current, source current, and compensated current of the harmonic compensation only and/or reactive power compensation, respectively. Wherein, the compensation current is slightly deviated from the simulation results. This is simply because measuring a small current is very difficult and the input to the current feedback ADC has a noticeable level of noise in the presence of electromagnetic interference.



(a)



(b)

Fig. 11. Experimental results (a) Different current waveform for harmonic suppression (b) Different current waveform for harmonic suppression and reactive compensation.

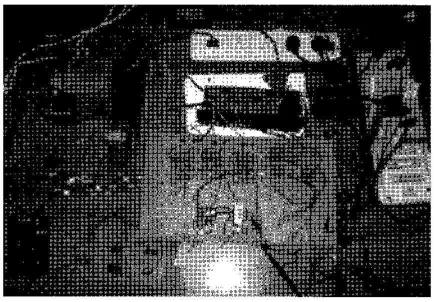


Fig. 12. Experimental setup.

6. Conclusion

The APF is able to suppress the dominant lower order harmonics to meet the IEEE-519 standard as well as reduce the reactive power consumption to achieve UPF. A hybrid power filter can be used, consisting of a passive filter, to suppress the major harmonic content, and an APF for fine tuning purposes. While implementing APF, the sampling frequency of the current feedback is fixed by the ADC. It will affect the inverter controller ability to determine accurately when the current has exceeded the hysteresis band.

Appendix: I

Injection Inductance (L_i): 40mH, Core: 30mm, toroidal core, No.of Turns: 98, No.of Strands: 3, Wire Gauge: 22SWG, **Capacitance (C_{dc})**: 2200μF, Voltage: 440V, DC, Type: Electrolytic

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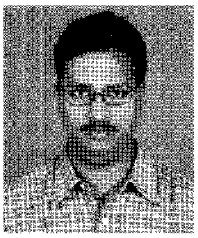

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