Journal of the Korean Institute of Electrical and Electronic Material Engineers, Vol. 21, No. 8, p. 699, August 2008.

논 문 21-8-3

Capacitance-voltage Characteristics of MOS Capacitors with Ge Nanocrystals Embedded in HfO_2 Gate Material

Byoungjun Park[1], Hye-Ryeong Lee[1], Kyoungah Cho[1], and Sangsig Kim[1,a]

Abstract

Capacitance versus voltage (C-V) characteristics of Ge-nanocrystal (NC)-embedded metal-oxide-semiconductor (MOS) capacitors with HfO_2 gate material were investigated in this work. The current versus voltage (I-V) curves obtained from Ge-NC-embedded MOS capacitors fabricated with the NH_3 annealed HfO_2 gate material reveal the reduction of leakage current, compared with those of MOS capacitors fabricated with the O_2 annealed HfO_2 gate material. The C-V curves of the Ge-NC-embedded MOS capacitor with HfO_2 gate material annealed in NH_3 ambient exhibit counterclockwise hysteresis loop of about 3.45 V memory window when bias voltage was varied from -10 to + 10 V. The observed hysteresis loop indicates the presence of charge storages in the Ge NCs caused by the Fowler-Nordheim (F-N) tunneling. In addition, capacitance versus time characteristics of Ge-NC-embedded MOS capacitors with HfO_2 gate material were analyzed to investigate their retention property.

Key Words : Germanium, Memories, Nanotechnology, HfO_2

1. INTRODUCTION

Nano-floating gate memory (NFGM) devices with nanocrystal (NC) floating gate embedded in dielectrics have been attracted attention in the field of memory-related electronics, and they have been widely investigated for replacing conventional flash memory devices utilizing continuous floating gates. The NFGM devices can provide faster write/erase speeds, higher density, lower power consuming memory, compared with conventional flash memory ones. Moreover, the NFGM devices composed of nanocrystals (NCs) isolated by dielectrics are more resistible to leakage current than conventional continuous floating gate memory ones[1]. Si NCs have widely been utilized for the fabrication of NFGM[2]. However, many groups have more recently researched Ge NCs due to their smaller band gap than those of Si NCs[3]. The smaller bandgap provides a higher confinement barrier for the retention mode and a smaller barrier for the program and erase modes. Besides, Ge-NC-embedded NFGM devices have a good compatibility with current complementary metal-oxide-semiconductor (CMOS) technology. On the other hand, the fabrication of Ge NCs inside dielectrics is much more difficult than that of Si NCs because of the relatively low evaporation temperature of Ge material and the difference in surface energy with respect to oxides [4]. Therefore, the size and distribution control in gate dielectric materials are essential for using Ge NCs in the fabrication of NFGM, and many research groups have studied the ion implantation method for the formation of Ge NCs floating gate[5].

In general, SiO_2 dielectrics have been used as a conventional dielectric material for MOS-based devices including NFGM. However, The use of SiO_2 dielectrics has approached the electrical and structural limits, and there has been many

1. Department of Electrical Engineering, Korea University (Anam-dong 5-ga, Seongbuk-gu, Seoul 136-701, Korea)
a. Corresponding Author : sangsig@korea.ac.kr
Received : 2008. 4. 24
Accepted : 2008. 7. 19

attempts to replace SiO_2 dielectrics with higher dielectric constant (k) materials including HfO_2, ZrO_2, and Al_2O_3. Among a variety of high-k dielectric materials, HfO_2 dielectrics have been largely investigated due to their high dielectric constant (~25), large bandgap (5.58 eV), and good stability with polycrystalline Si gate materials[6]. However, HfO_2 gate layers also have some electrical problems related to reliability including the low breakdown voltage due to large amount of defects and stressing induced degradation as the other high-k materials have faced. There have been many studies including the annealing process to improve the stabilities of the gate layers.

In this work, HfO_2 was employed for a high-k gate material, and an amide precursor TEMAH was used instead of $HfCl_4$ used conventionally as aprecursor of HfO_2 to obtain the high quality metal oxides with very low impurities. Ion implantation method was used to form Ge layers in the gate material, and rapid thermal annealing (RTA) process was applied not only to form Ge NCs but also to improve the stability of HfO_2 gate material in O_2 and NH_3 ambient. The effect of annealing gases was compared after capacitance versus voltage (C-V) and current versus voltage (I-V) measurements made for capacitors containing Ge NCs embedded HfO_2 gate material, and their memory characteristics are investigated. To evaluate the retention characteristics, capacitance versus time (C-t) measurement was carried out at room temperature.

2. EXPERIMENT

Tetrakis Ethyle Methyle Amino Hafnium (TEMAH) and O_3 were utilized as the precursors of HfO_2 gate material. The atomic layer deposition (ALD) method was used to deposit 20-nm thick HfO_2 layers on (100) p-type Si substrates at 250 ℃. The layers were then implanted at room temperature with $^{74}Ge^+$ ions at 17 keV with a dose of $1x10^{16}$ cm^{-2} for the fabrication of NFGM. The dose of ions and the kinetic energy of ions were determined using a TRIM (transport of ions in matter) simulation code. The Ge-ions-implanted HfO_2 gate material in the MOS capacitors were annealed in O_2 and NH_3 gas ambient for 10 min at 800 ℃ to form Ge NCs in this material and improve the dielectric properties as reducing unwanted defects or trap sites, and Ti/Au electrodes were then deposited using thermal evaporator system; their thicknesses are 25 and 100 nm, respectively. The size of top electrodes was 1.93×10^{-3} cm^2. The relative permittivity of HfO2 was found to be ~22. The size of Ge NCs within HfO_2 gate material was examined by the plan-view high-resolution transmission electron microscopy (HRTEM, Tecnai F30). The ion distribution in the MOS capacitors was obtained by energy dispersive x-ray (EDX) analysis. The high frequency (1 MHz) C-V, C-t and I-V measurement were conducted using a HP 4285A LCR meter and a HP 4155C semiconductor analyzer at room temperature in air.

3. RESULT AND DISCUSSION

The schematic of fabrication process for the MOS capacitors with Ge-NC-embedded HfO_2 gate material is shown in Fig. 1. The HfO_2 gate material was deposited by ALD, and Ge ions were implanted in HfO_2 gate material after selecting the proper energy and dose condition through a TRIM simulation code. After a RTA process, implanted Ge ions were aggregated into discrete Ge NCs in HfO_2 gate material and Ti/Au gate metals were deposited by a thermal evaporator.

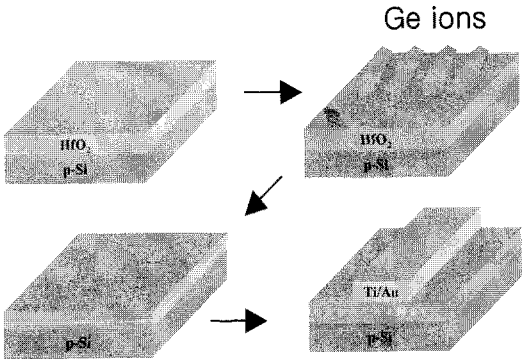

Fig. 1. Schematic of the fabrication process for Ge-NC-embedded MOS capacitors.

The plan-view HRTEM image of the MOS capacitor with Ge NCs embedded in HfO_2 gate material is shown in Fig. 2(a). Spherical Ge NCs are present in the HfO_2 gate material annealed in NH_3 ambient for 10 min at 800 ℃. The size and density of the Ge NCs are about 3 nm and 3.81 x 10^{12} cm^{-2}, respectively, and Coulomb blockade effect and the quantum confinement effect are significant for the 'write/erase' process due to the nano-scaled size effect of Ge NCs. The HfO_2 gate material seems to be partially crystallized, but overall HfO_2 gate material maintains an amorphous phase when it was annealed in NH_3 ambient. Microstructure of HfO_2 films grown by ALD or chemical vapor deposition depends on the temperature, the thickness, the laminate structure, the substrate orientation, and the employed precursor[7]. In this study, the dependence of annealing gases was investigated using O_2 and NH_3 gases. In addition, the EDX spectrum of the MOS capacitor with Ge NCs embedded in HfO_2 gate material is shown in Fig. 2(b), and it reveals the presence of Ge, Hf, O ions in this MOS capacitor.

RTA method has usually been used to improve the characteristics of high-k gate materials including HfO_2. RTA process reduces point defects in HfO_2, resulting in strain-induced self-organization[8], and post deposition annealing of HfO_2 films in O_2 ambient can reduce the interface trap density (in the order of ~10^{11} cm^{-2}) and oxygen vacancies which are the major origin of unwanted deep traps[9]. However, C-V curves in Fig. 3(a) obtained from HfO_2gate material without Ge NCs annealed in O_2 ambient for 10 min at 800 ℃ show counterclockwise memory hysteresis about 4.54 V when the bias voltage varied from -10 to 10 V, indicating the presence of traps or defects of HfO_2 gate material. It may be due to oxygen vacancies of as-deposited HfO_2 films or grain boundary defects as a result of crystallization. It has been reported in Ref. 10 that as-deposited HfO_2 is amorphous, but that annealing at temperature higher than

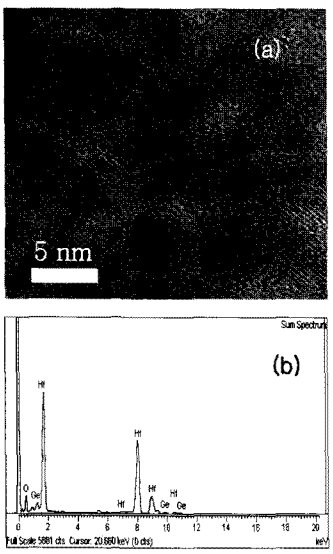

Fig. 2. (a) Plan-view HRTEM image of Ge NCs embedded in HfO_2 gate material. (b) EDX spectrum of Ge-NC-embedded HfO_2 gate material.

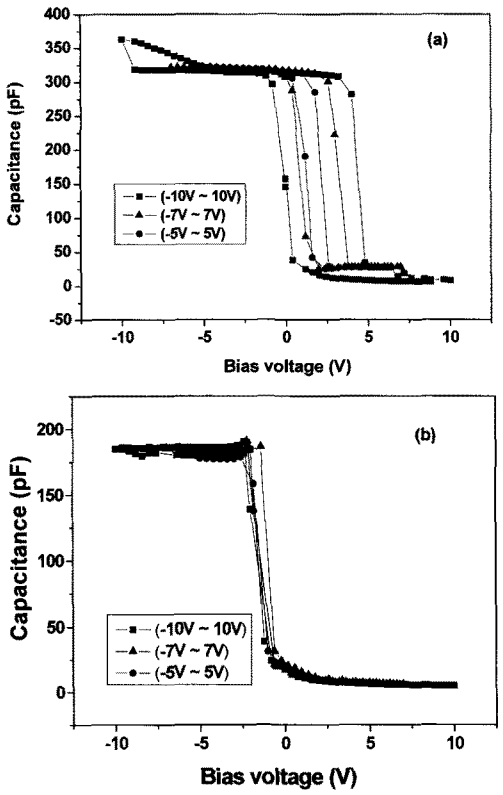

Fig. 3. C-V curves of MOS capacitors without Ge NCs in HfO_2 gate material annealed in (a) O_2 and (b) NH_3 ambient for 10 min at 800 ℃.

650 ℃ may cause pronounced crystallization and that the distorted chemical bonding at the grain boundary create trapping sites. These unwanted properties have restricted the application of HfO_2 for the conventional CMOS process and many studies have conducted to overcome crystallization-related problems of HfO_2. The reduction of the physical thickness of the HfO_2 films appears to be effective in suppressing the crystallization of HfO_2 (~2 nm)[11]. However, thickness control cannot be adapted to some devices and can cause a leakage current problem.

Recently, nitridation by NH_3 annealing has been widely researched for improvement of HfO_2 gate material characteristics since it can improve scalability and provide lower leakage and higher breakdown fields. Especially, Choa et al studied the change in chemical state related to N incorporation for a post annealing treatment in an NH_3 atmosphere, and they reported that the incorporated N is bonded to the SiO_2 interfacial layer and the silicate film, but not to pure HfO_2[12]. The suppression of crystallization during high temperature treatment, the reduction of B penetration, the N-induced drastic increase dielectric constant of the HfO_2 gate films, and band-gap narrowing is induced by N incorporation into Hf based high-k dielectrics[13]. Figure 3(b) represents the C-V curves obtained from the HfO_2 gate material without Ge NCs annealed in NH_3 ambient for 10 min at 800 ℃. The hysteresis windows related with traps are not represented in this case, in contrast to the C-V curves taken from the HfO_2 gate material annealed in O_2 ambient. Also, there are just few grain boundaries in HfO_2 gate material after 800 ℃ annealing in NH_3 ambient from plan-view HRTEM image (not shown here), while the other NH_3 films annealed in N_2 or O_2 atmosphere above 650 ℃ are mostly crystallized and have many grain boundaries in many studies. The surface nitridation of Si substrate by rapid thermal annealing in NH_3 ambient prior to high-k dielectric deposition helps in achieving reduced equivalent oxide thickness (EOT) as well as preventing boron penetration[14]. However, this pre-nitridation technique can cause higher C-V hysteresis due to a larger amount of positive charges. In this study, the nitridation was adopted after the film deposition to improve the electrical characteristics of the HfO_2 gate material. The C-V curves demonstrate that the post deposition annealing of the HfO_2 gate material using NH_3 gas can reduce the C-V hysteresis related with traps or defects. It suggests that NH_3-treated HfO_2 gate material can be one of the proper candidates for replacement of SiO_2 for scaling down of CMOS technology.

Figure 4(a) shows the leakage current comparison between two samples annealed in O_2 and NH_3 ambient. The leakage current of the MOS capacitor annealed by NH_3 gas is much smaller than that of the sample annealed by O_2 gas. The leakage current of as-grown samples is much higher than those of annealed capacitors (not shown). It may be related with reduction of defects, leading to the reduction in gate leakage current. Umezawa et al explained such reduction using band gap theory[15]. Oxygen vacancy (V_o) levels in HfO_2 are located at 1.2 eV below the bottom of the HfO_2 conduction band (about 0.4 eV

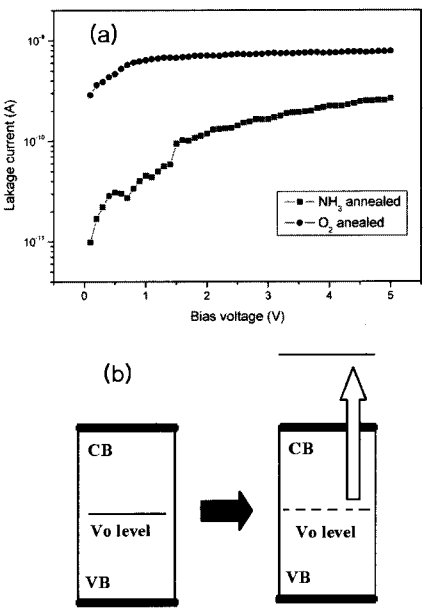

Fig. 4. (a) Leakage current comparison of O_2 and NH_3 annealed MOS capacitors (b) The change of the band diagram by NH_3 annealing.

above the bottom of the Si conduction band)[16]. Then N atoms favorably couple with V_{os} and modify the charged states of V_o from neutral (V_o^0) to positively charged (V_o^{2+}), resulting in the elimination of V_o related gap states. Accordingly, V_o mediated leakage paths can be eliminated by N incorporation. Fig. 4(b) represents the above-described mechanism using the change of V_o level through NH_3 annealing.

C-V characteristics of MOS capacitors with and without Ge NCs in HfO_2 gate material are represented in Fig. 5(a). The counterclockwise hysteresis with a 3.45 V memory window is exhibited for the MOS capacitors with Ge NCs when the bias voltage was varied from - 10 to 10 V, while there is a little memory window in a C-V curve taken from the MOS capacitors without Ge NCs. Generally, the memory characteristics observed for the NCs-embedded MOS capacitors may be explained by the storage of the injected charges in three possible sites; NCs-related traps, defects inside the gate material or the interface states between the gate material and Si. In this result, the trapping of electron or hole is mainly caused by NCs-related traps. The same thickness of interfacial layer seen in the capacitor without Ge NCs (not shown) as that with Ge NCs and its little C-V hysteresis rule out the possibility of memory characteristics related with defects inside the gate material or the interface states between the gate material and Si. Clear flatband voltage shift from the electron and hole charging-discharging mechanism was observed in the high-frequency C-V measurement. And the counterclockwise hysteresis with 3.45 V memory window was represented when the bias voltage was varied from - 10 to 10 V. This result reveals that Ge NCs also act well as charge storage in HfO_2 gate material when it was annealed in NH_3 gas ambient. The C-V curves were taken for many capacitor samples to ensure uniformity. The window of the C-V loop also indicates the magnitude of the trapped charge carriers in the floating gate layer. The estimated number of trapped charges in the Ge-NCs for a threshold voltage shift is about 1.1×10^{11} cm^{-2}.

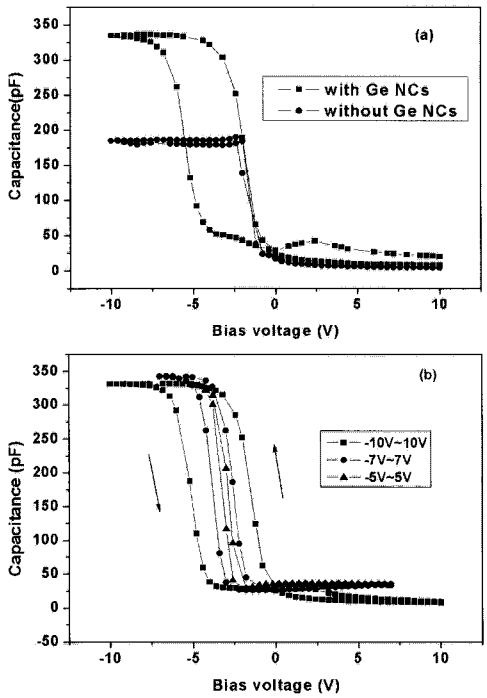

Fig. 5. (a) C-V curves of MOS capacitors with and without Ge NCs in HfO_2 gate material annealed in NH_3 ambient for 10 min at 800 ℃ (b) C-V curve of MOS capacitors with GeNCs in HfO_2 gate material annealed in NH_3 ambient for 10 min at 800 ℃.

The retention characteristics of storage charges in Ge-NCs embedded in the HfO_2 gate layer were examined at room temperature. C-t measurement result reveals the capacitance decrease as a function of time as shown in Fig. 6. The capacitor was first charged for 20 s at a bias voltage of 8 V. Then, the C-t measurements were carried out under a stress voltage of -1 V applied to the top electrode. It can be seen that after 10^4s at a stress voltage of - 1 V, the decay of capacitance is just 1.06 % for the MOS capacitors with Ge NCs in HfO_2 gate material annealed in NH_3 ambient for 10 min at 800 ℃, suggesting good charge retention characteristics, while all the capacitance decreased out after 10^4s with -1 V stress voltage for MOS capacitors without Ge NCs in HfO_2 gate material (not

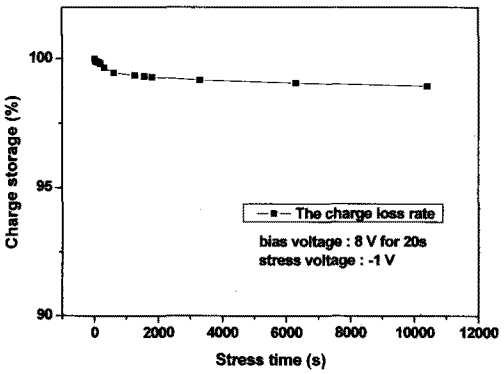

Fig. 6. C-t characteristics of the MOS capacitor with Ge NCs in HfO_2 gate material annealed in NH_3 ambient for 10 min at 800 ℃.

shown). The results prove that the long retention time comes not from defects or leakage path in HfO_2 gate material but from the Ge NCs embedded in HfO_2 gate material. It is also clearly shown that no significant initial time decay can be observed in Fig. 6. It means the any significant lateral channel leakage between Ge NCs is absent[17] and that charge loss can mainly occur through leaking from isolated Ge NCs to the Si substrate via the tunneling. Shi et al[18] studied a model of deep trapping centers concerning three-dimensional quantum confinement and the Coulomb blockade effect. They state that a long retention time can be achieved by introducing deep trapping centers in NCs and reducing the interface states between gate material and the Si substrate. Based on the model, we suggest here that many deep trapping centers are present in Ge NCs and unwanted interface states between HfO_2 gate material and Si substrate are reduced well through NH_3 annealing[19].

4. CONCLUSION

In this work, N-containing precursor, TEMAH, was used for the HfO_2 deposition by ALD and the effect of nitridation of HfO_2 gate material was shown via C-V and I-V measurement. C-V curves of MOS capacitors without Ge NCs in HfO_2 gate material annealed with O_2 and NH_3 reveal that nitridation by NH_3 annealing improves the film characteristics associated especially with traps and interfacial layers. Also, the leakage current from the capacitors annealed in NH_3 ambient is lower than that of O_2 annealed capacitors, indicating that NH_3 annealing suppresses the leakage current path which affects transistor performance. C-V curves of MOS capacitors with Ge-NC-embedded in HfO_2 gate material annealed in NH_3 ambient are counterclockwise, indicating the charge storages in the Ge NCs by the tunneling of charge barriers between the substrate and the Ge NCs. The hysteresis window is 3.45 V when the bias voltage was varied from -10 to 10 V. The C-t characteristics of the MOS capacitor with Ge-NC-embedded in HfO_2 gate material annealed in NH_3 ambient reveal that this MOS capacitor represents a good retention characteristics. Therefore, the nitridation of HfO_2 films by NH_3 annealing is effective to suppress defects or traps and the application of NH_3-treated HfO_2 in floating gate memory is possible for scaling in future memory devices.

ACKNOWLEDGEMENTS

This work was supported by the National Research Program for the 0.1 Terabit Non-Volatile Memory Development (10022965-2006-13), the Center for Integrated-Nano-Systems (CINS) of the Korea Research Foundation (KRF-2006-005-J03601), and the Korea Science and Engineering Foundation (KOSEF) through the National Research Lab.Program (M10500000045-06J0000-04510).

REFERENCES

[1] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, "A silicon nanocrystals based memory", Appl. Phys. Lett., Vol. 68, p. 1377, 1996.

[2] P. Normand, E. Kapetanakis, P. Dimitrakis, D. Tsoukalas, K. Beltsios, N. Cherkashin, C. Bonafos, G. Benassayag, H. Coffin, A. Claverie, V. Soncini, A. Agarwal, and M. Ameen, "Effect of annealing environment on

the memory properties of thin oxides with embedded Si nanocrystals obtained by low-energy ion-beam synthesis", Appl. Phys. Lett., Vol. 83, p. 168, 2003.

[3] S. Duguay, J. J. Grob, A. Slaoui, Y. L. Gall, and M. Amann-Liess, "Structural and electrical properties of Ge nanocrystals embedded in SiO_2 by ion implantation and annealing", J. Apple. Phys., Vol. 97, p. 104330, 2005.

[4] D. W. Kim, T. Kim, and S. K. Banerjee, "Memory characterization of SiGe Quantum dot flash memories with HfO_2 and SiO_2 tunneling dielectrics", IEEE transactions on electron devices, Vol. 50, No. 9, p. 1823, 2003.

[5] K. Masuda, M. Yamamoto, M. Kanaya, and Y. Kanemitsu, "Fabrication of Ge nanocrystals in SiO_2 films by ion implantation : control of size and position", J. Non-crystalline solids, Vol. 229-302, p. 1079, 2002.

[6] M. Balog, M. Schieber, M. Michman, and S. Patia, "Chemical vapor deposition and characterization of HfO_2 films from organo-hafnium compounds", Thin Solid Films, Vol. 41, No. 3, p. 247, 1977.

[7] A. Callegari, E. Cartier, M. Gribelyuk, H. F. Okom-Schmidt, and T. Zabel, "Physical and electrical characterization of Hafnium oxide and Hafnium silicate sputtered films", J. Appl. Phys., Vol. 90, p. 6466, 2001.

[8] A. Callegari, P. Jamison, E. Cartier, S. Zafar, E. Gusev, V. Narayanan, C. D. Emic, D. Lacey, M. Feely, R. Jammy, M. Gribelyuk, J. Shepard, W. Anderson, A. Curioni, and C. Pignedoli, "Interface engineering for enhanced electron mobilities in W/HfO_2 gate stacks", IEDM Tech. Dig., p. 825, 2004.

[9] N. Zhan, K. L. Ng, H. Wong, M. C. Poon, and C. W. Kok, "Effects of Rapid Thermal Annealing on the Interface and Oxide Trap Distributions in Hafnium Oxide Films", Electron Devices and Solid-State Circuits, IEEE conference on, p. 431, 2003.

[10] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics : Current status and materials properties considerations", J. Appl. Phys., Vol. 89, No. 10, p. 5243, 2001.

[11] S. C. Song, Z. Zhang, C. Huffman, J. H. Sim, S. H. Bae, P. D. Kirsch, P. Majhi, R. Choi, N. Moumen, and B. H. Lee, "Highly manufacturable advanced gate-stack technology for sub-45-nm self-aligned gate-first CMOSFETs", IEEE Trans. Electron Devices, Vol. 53, No. 5, p. 979, 2006.

[12] M.-H. Choa, K. B. Chung, C. N. Whang, D.-H. Ko, J. H. Lee, and N. I. Lee, "Nitridation for HfO_2 high-k films on Si by an NH_3 annealing treatment", Appl. Phys. Lett., Vol. 88, p. 202902, 1996.

[13] K. Y. Tong, E. V. Jelenkovic, W. Liu, and J. Y. Dai, "Nitridation of hafnium oxide by reactive sputtering", Microelectron. Eng., Vol. 83, p. 293, 2006.

[14] S. J. Lee, H. F. Luan, C. H. Lee, T. S. Jeon, W. P. Bai, Y. Senzaki, D. Robert, and D. L. Kwong, "Performance and reliability of ultra thin CVD HfO gate dielectrics with dual poly-Si gate electrodes", in VLSI Symp. Tech. Dig., p. 133, 2001.

[15] N. Umezawa, K. Shiraishi, T. Ohno, H. Watanabe, T. Chikyow, K. Torii, K. Yamabe, K. Yamada, H. Kitajima, and T. Arikado, "First-principles studies of the intrinsic effect of nitrogen atoms on reduction in gate leakage current through Hf-based high-k dielectrics", Appl. Phys. Lett., Vol. 86, p. 143507, 2005.

[16] H. Takeuchi, D. Ha, and T.-J. King, "Observation of bulk HfO_2 defects by spectroscopic ellipsometry", J. Vac. Sci. Technol., Vol. 22, No. 4, p. 1337, 2004.

[17] J. K. Kim, H. J. Cheong, Y. Kim, J.-Y. Yi, and H. J. Bark, "Rapid-thermal-annealing effect on lateral charge loss in metal - oxide - semiconductor capacitors with Ge nanocrystals", Appl. Phys. Lett., Vol. 82, p. 2527, 2003.

[18] Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, "Effects of traps on charge storage characteristics in metal-oxide-semiconductor memory structures based on silicon nanocrystals", J. Appl. Phys., Vol. 84, p. 2358, 1998.

[19] P. F. Lee, X. B. Lu, J. Y. Dai, H. L. W. Chan, E. Jelenkovic, and K. Y. Tong, "Memory effect and retention property of Ge nanocrystal embedded Hf-aluminate high-k gate dielectric", Nanotechnology, Vol. 17, p. 1202, 2006.