

Core Circuit Technologies for PN-Diode-Cell PRAM

Hee-Bok Kang*, Suk-Kyoung Hong*, Sung-Joo Hong*, Man Young Sung**,
Bok-Gil Choi***, and Jinyong Chung****

Abstract—Phase-change random access memory (PRAM) chip cell phase of amorphous state is rapidly changed to crystal state above 160 Celsius degree within several seconds during Infrared (IR) reflow. Thus, on-board programming method is considered for PRAM chip programming. We demonstrated the functional 512Mb PRAM with 90nm technology using several novel core circuits, such as metal-2 line based global row decoding scheme, PN-diode cells based BL discharge (BLDIS) scheme, and PMOS switch based column decoding scheme. The reverse-state standby current of each PRAM cell is near 10 pA range. The total leak current of 512Mb PRAM chip in standby mode on discharging state can be more than 5 mA. Thus in the proposed BLDIS control, all bitlines (BLs) are in floating state in standby mode, then in active mode, the activated BLs are discharged to low level in the early timing of the active period by the short pulse BLDIS control timing operation. In the conventional sense amplifier, the simultaneous switching activation timing operation invokes the large coupling noise between the VSAREF node and the inner amplification nodes of the sense amplifiers. The coupling noise at VSAREF degrades the sensing voltage margin of the conventional sense amplifier. The merit of the proposed sense amplifier is almost removing the coupling noise at VSAREF from sharing with other sense amplifiers.

Index Terms—PRAM, NVRAM, FeRAM, MRAM, GST (Ge₂Sb₂Te₅), SET, RESET, GBL, GXDEC, BL discharge (BLDIS)

I. INTRODUCTION

Non-volatile random access memory (NVRAM) delivers the high speed and provides the non-volatility. Thus, NVRAM can be used as working memory in equipment previously using, for example, DRAM or SRAM due to fast write and read time. There are various types of the promising candidates for future NVRAM, including FeRAM [1], MRAM, and phase-change random access memory (PRAM) [2,3]. The first commercialized FeRAM have been maturing an increasing variety of applications in RFID tags, smart cards, automotive electronics, industrial equipment, information processing systems, and more. PRAM and MRAM can find applications in mobile phones and consumer electronics as an alternative NOR Flash memory. PRAM is similar to the technology used in CDs and DVDs. In a PRAM, an electrical current heats a chalcogenide GST (Ge₂Sb₂Te₅) film into melting state and quenches with different heat-sink speeds resulting in either a low resistance crystalline (SET) state through slow heat sink or a high resistance amorphous (RESET) state through fast heat sink. This allows the two states to be read as logic '0' (SET) or logic '1' (RESET).

The access element of PRAM cell can be consisted of a select MOS type transistor, BJT or PN diode to the storage element serially connected thereto as shown in Table 1.

The logic value stored in the PRAM cell is evaluated by the current sense amplifiers. Typically, the current sense amplifier includes a comparator receiving the bitline (BL) current sensing voltage and a suitable reference

Manuscript received May 24, 2008; revised June 3, 2008

* R&D Div., Hynix Semiconductor, Ichon, 467-701, Korea

** Department of Electrical Engineering, Korea Univ., Seoul, 136-701, Korea

*** Department of Electrical & Electronic Engineering, Kongju National Univ., Cheonan, 330-717, Korea

**** Pohang University of Science and Technology

E-mail : kanghb@hynix.com

Table 1. Comparison characteristics of the various PRAM cells.

	PN diode cell	BJT cell	MOS cell
Cell size	O	Δ	Δ
Process	Δ	O	O
Current drivability	O	O	Δ
Write voltage	Δ	Δ	O
Sensing speed	Δ	Δ	O
Operation current	Δ	Δ	O
Standby current	Δ	Δ	O
Cell efficiency	< 40%	< 40%	< 40%
Embedded	Δ	O	O
Major target	NOR	NOR	MoDRAM
Endurance	1E6	1E6	1E11

(REF) voltage. In the case in which the BL voltage is higher than the REF voltage, the result is corresponding to a stored logic value '1', whereas in the case in which the BL voltage is lower than the REF voltage, this result is corresponding to the stored logic value '0'. The PN diode access element is switched on and then the BL sensing voltage reaches a steady-state value to be sensed. Accordingly, such a high BL sensing voltage level has to be taken into account for the timing of a reading operation. Inevitably, the reading operation is slowed down, since the timing has to be based on the worst BL sensing voltage.

Infrared (IR) reflow involves the transfer of thermal energy from infrared lamps to the board assembly with PRAM chip. The board assembly with PRAM chip is heated by IR reflow primarily by line-of-sight surface heat absorption. A solder reflow process follows an optimized temperature profile. A typical reflow temperature profile would reach to 250 Celsius degree. By the way, the PRAM chip cell phase of amorphous state is rapidly changed to crystal state above 160 Celsius degree within several seconds as shown in Fig. 1. Thus, firmware programming process on package level before printed circuit board (PCB) is almost impossible.

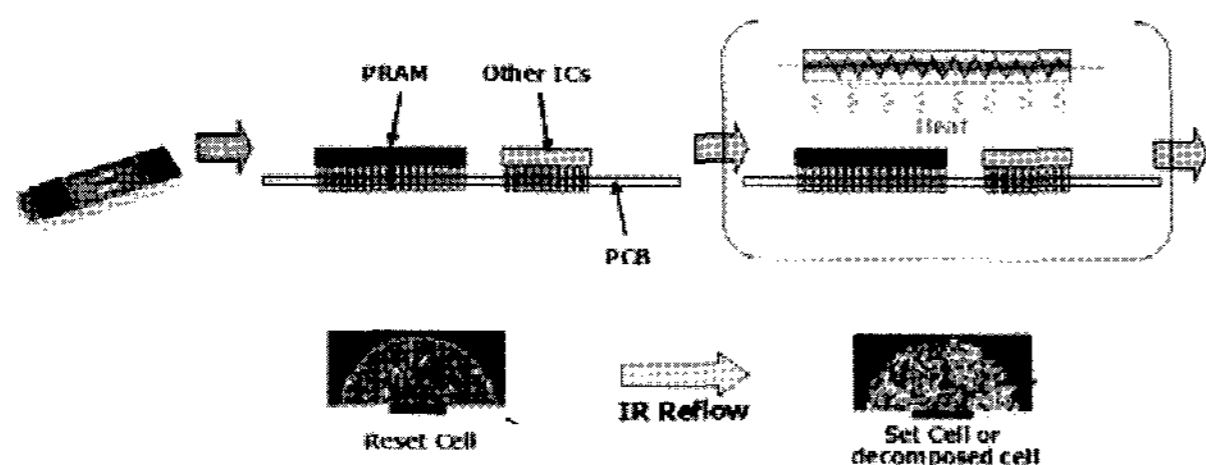


Fig. 1. The IR reflow temperature dependence of PRAM cell.

The on-PCB programming method is considered for PRAM chip programming.

II. CHIP DESIGN SCHEME AND MEASURED RESULTS

We have prepared and analyzed test chip of 512Mb PRAM for the pre-evaluation of core circuit properties. The core architecture of one bank structure is composed of 32Mb PRAM cell array. Unit cell with wordline (WL) and BL pitch of 216 nm was designed and fabricated by 90nm CMOS technology. Thin gate oxide is employed for low voltage circuit devices of 1.8 V in the peripheral region. On the other hand, thick gate oxide is employed for highly boosted pumping voltage circuit devices of 3 V, 4 V, and 5.5 V. Three leveled aluminum interconnection layers are used for core memory and peripheral blocks. Metal 1, 2, and 3 are used for BL, WL, and global BL (GBL), respectively. The phase change material is used with GST ($\text{Ge}_2\text{Sb}_2\text{Te}_5$). The vertical PN-diode switch cells are prepared on heavily doped N+ active base, while stacked metal contacts from N+ active base are formed for strapping with the shunting metal-2 WL at every 8-cells string. The ring-type and pillar-type bottom electrode contact (BEC) is formed with contact size of around 40 nm. The GST-BEC shape constructed as T-shape structure gave typical reset current value of 1 mA per cell. The electrical cell parameters of I-V characteristics of PN-diode PRAM cell are shown in Fig. 2.

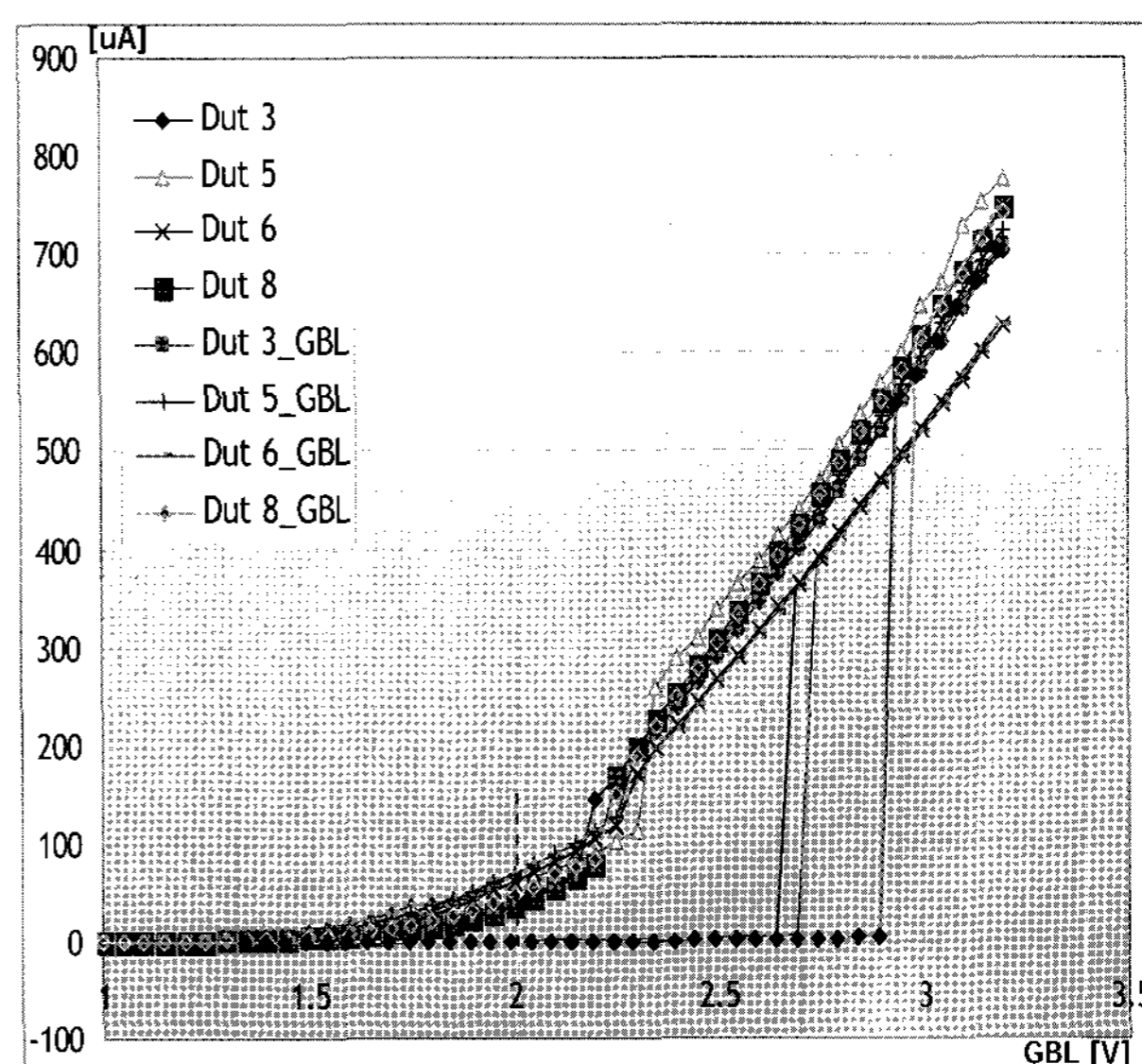


Fig. 2. I-V characteristics of PN-diode PRAM cell.

The snap-back voltage on the reset-state cell is around 2.5 V, which is sufficient for BL bias voltage of 1.8 V-2.0 V in cell current sensing. In general, the cell efficiency of 512Mb PRAM is less than 40%, due to large core circuit layout burden from the large cell write current. In this 90 nm CMOS technology, the cell write current for one bit cell is around 1.0 mA, which requires high current drivability in column and row decoding circuits. By the way, the power VPP voltage at write driver (WD) is about 5.5 V. WD voltage is dropped gradually from 5.5 V to ground voltage during going the write route of GBL, column switch, BL, GST, PN-diode, WL, and row decoder. Thus, switching device size on column and row decoder should be large enough for minimizing voltage drop at write current path. That prevents increasing the cell efficiency in high density PRAM chip. Thus, there are much needs for novel core architecture improving cell efficiency. The column decoding scheme of PRAM is similar to that of NOR flash, in which column switch is composed of NMOS transistor as shown in Fig. 3.

In the novel core architecture, column switch is composed of PMOS transistor, smaller than NMOS switch. In a cell array, BL charge should be discharged to prevent voltage increasing over snap-back voltage during active or standby mode by the reverse biased leakage current between WL of 4.0 V and floated BL. In conventional scheme, accumulated BL charge by leakage current is discharged by bitline discharge (BLDIS) NMOS switch. In the novel core architecture, BLDIS devices are composed of PN-diode cells, from

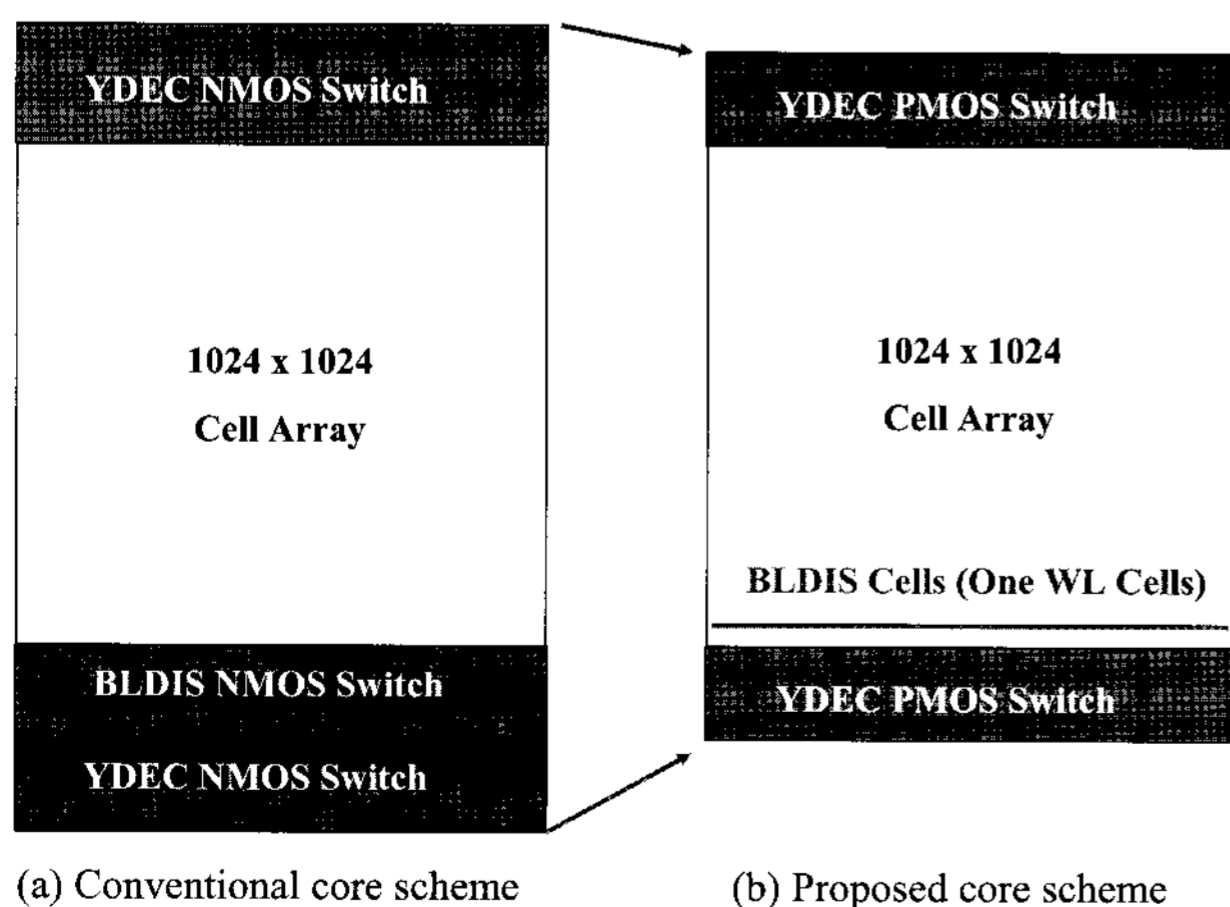


Fig. 3. Core block diagram of column decoder and bitline discharge (BLDIS) scheme.

which the core circuit layout size is decreased by 5%. The details of novel core circuits are shown in Fig. 4.

In cell array, N+ active node of 8-bit cell string is shunted with the metal-2 WL via metal contacts. Row decoder control signal line of GXDEC is used with metal-2 line, same level to WL. To avoid from adding additional metal line layer of GXDEC, one of WLs is used for GXDEC line by opening the shunting contact connection between WL to N+ active node, which make the GXDEC line free from cell. One WL of BLDIS cells is used for BLDIS switch. Current characteristics and BLDIS control of BLDIS cell are shown in Fig. 5. The reverse-state standby current of each PRAM cell is near 10 pA range. The total leak current of 512Mb PRAM chip in standby mode on discharging state can be more than 5 mA. Thus in the proposed BLDIS control, all BLs are in floating state in standby mode, then in active mode, the activated BLs are discharged to low level in the early timing of the active period by the short pulse BLDIS control timing operation.

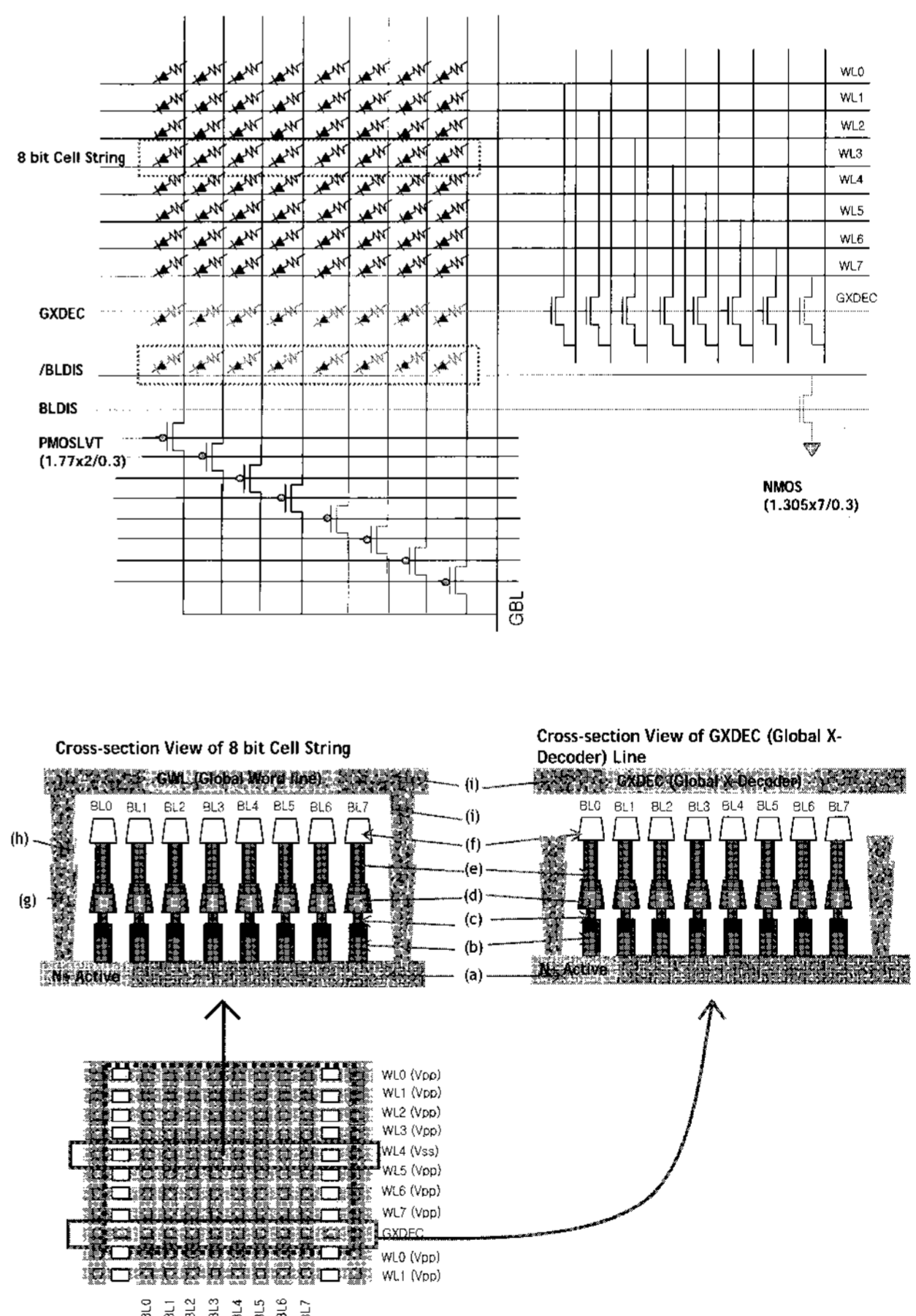


Fig. 4. Detailed circuits of PRAM cell array and decoder switch scheme.

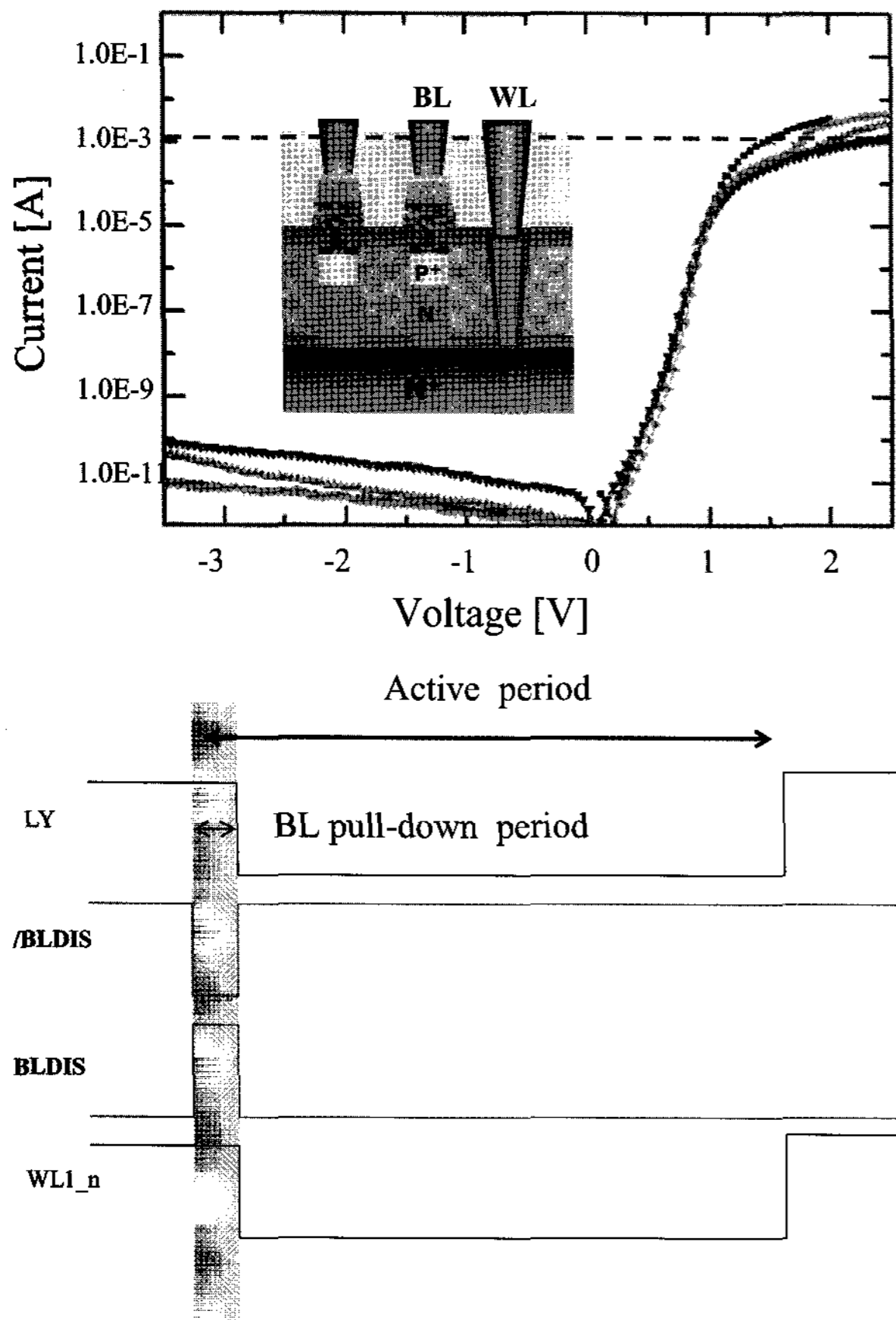


Fig.5. Current characteristics and BLDIS control of BLDIS cell.

The initial manufactured state of PRAM cell is in the condition of SET state with low GST resistance of less than 2k Ohm. During BLDIS operation, because of low discharge current level, BLDIS cells never reversely switch to the RESET state, so that the SET reliability of BLDIS cell is guaranteed. The column decoder switch characteristics of NMOS and PMOS devices are compared as shown in Fig. 6.

NMOS column switch devices, because of low current drivability at WD VPP voltage, which increases the column

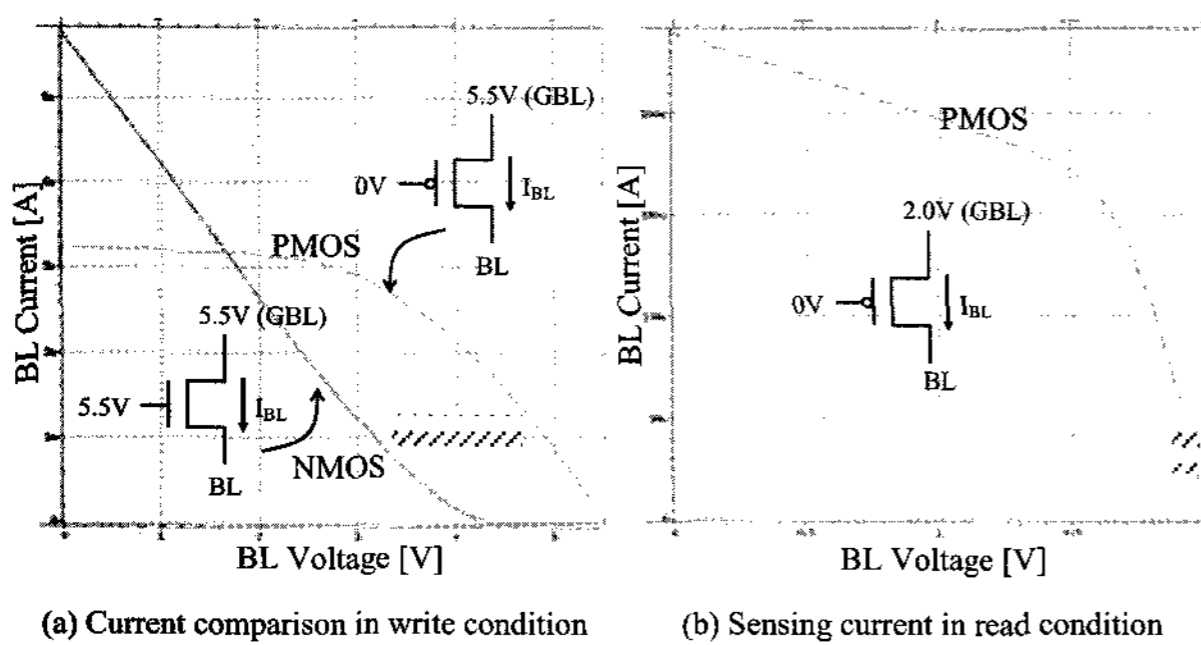


Fig. 6. Operation characteristics of column decoder PMOS switch.

decoding circuit layout size. By the way, compared with same NMOS switch size, PMOS switch has more high current drivability at VPP write condition. Thus, PMOS switch is more efficient than NMOS switch for column switch in write mode, and the current sensing operation in read mode can be worked well on current sensing voltage of 1.8 V - 2.0 V. Sensing voltage generating circuit and operation timing diagram is shown in Fig. 7. SAI voltage is the input sensing voltage signal from the cell sensing current. Read bias voltage for cell sensing current at MBL is targeted by adding the threshold voltage 1.2 V of PN diode and the half snapback voltage 0.6 V - 0.8 V of GST storage layer.

Sensing amplifier circuit and operation timing diagram is shown in Fig. 8. The reference voltage of VSAREF is shared with other sense amplifiers. In the conventional sense amplifier, the simultaneous switching activation timing operation invokes the large coupling noise between the VSAREF node and the inner amplification nodes of the sense amplifiers. The coupling noise at VSAREF degrades the sensing voltage margin of the conventional sense amplifier. The merit of the proposed sense amplifier is almost removing the coupling noise at VSAREF from sharing with other sense amplifiers.

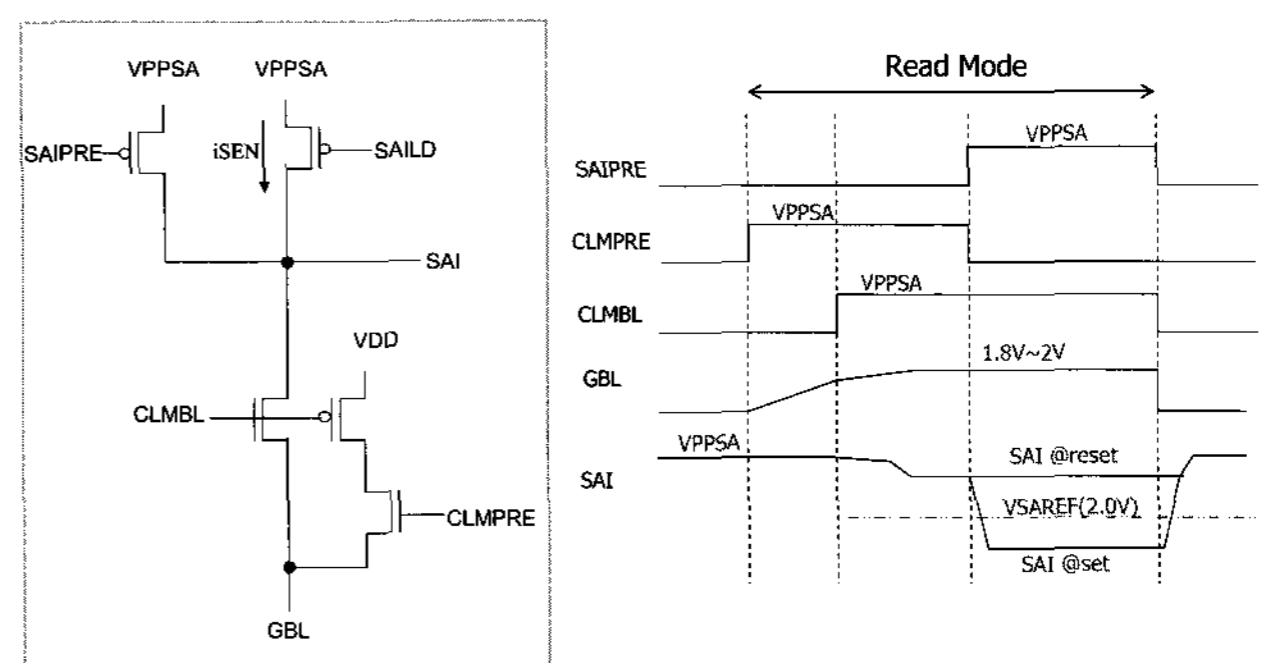


Fig. 7. Sensing voltage generating circuit and operation timing diagram.

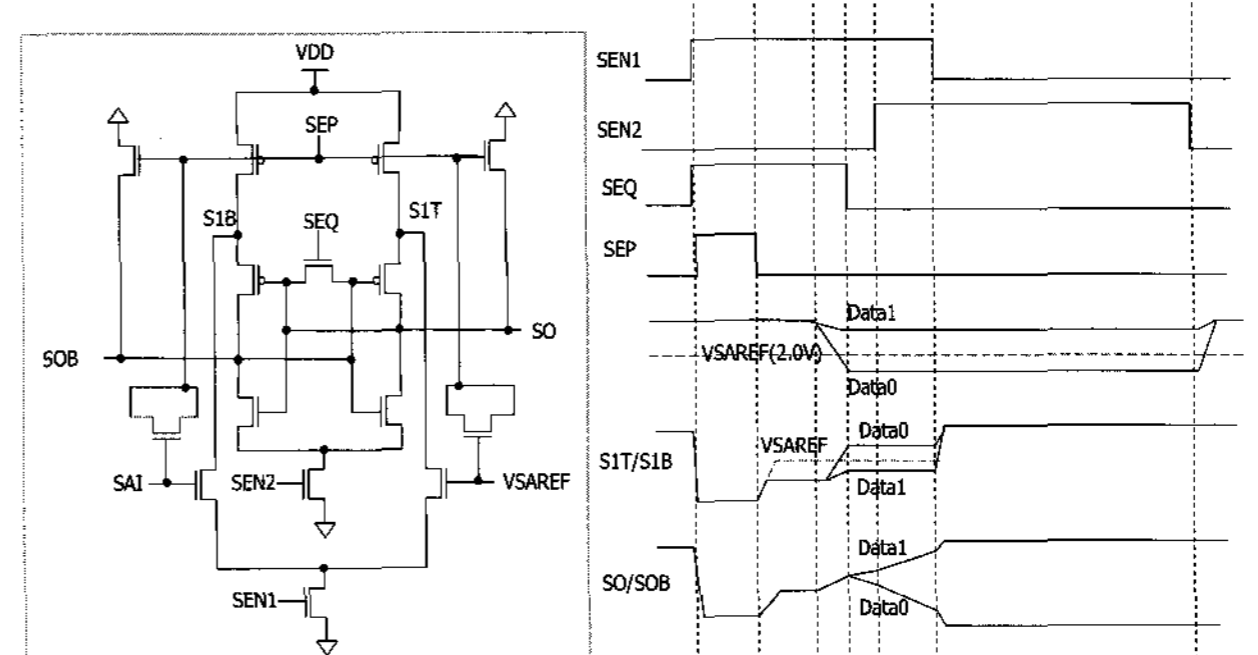


Fig. 8. Sensing amplifier circuit and operation timing diagram.

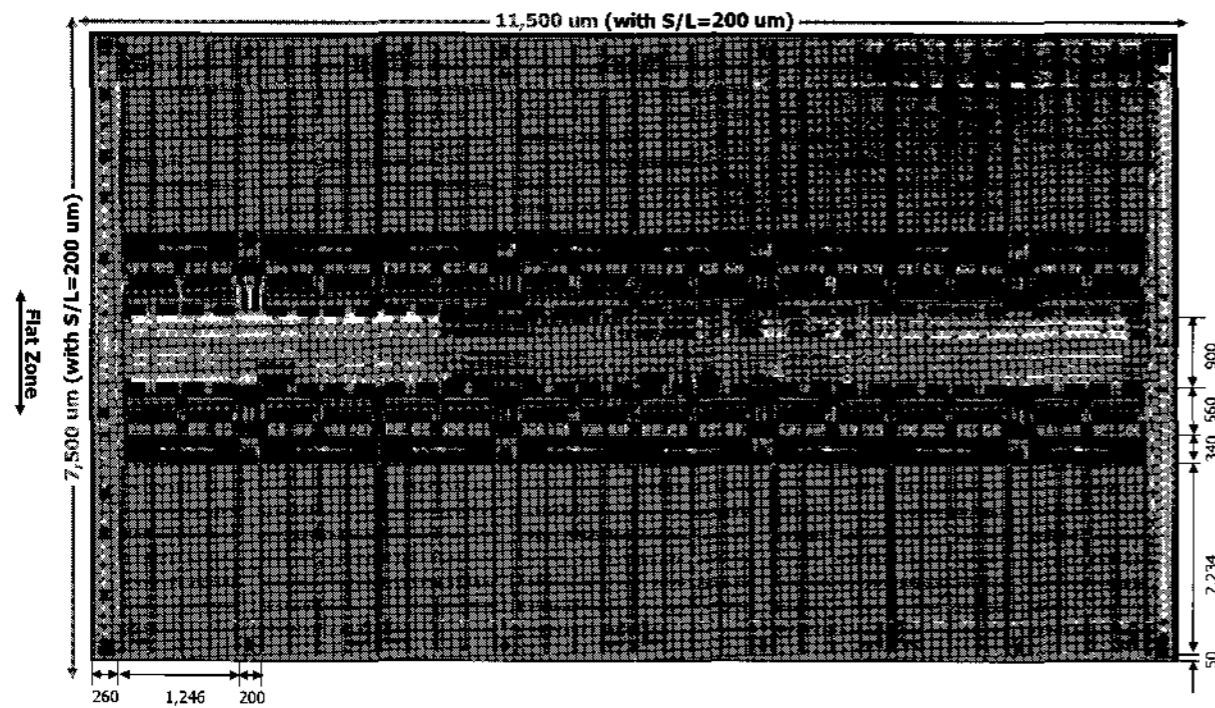


Fig. 9. Chip photo of 512Mb PRAM.

The test chip photo of 512Mb PRAM for evaluation of novel core circuit scheme is designed and evaluated as shown in Fig. 9.

III. CONCLUSIONS

Column switch is composed of PMOS transistor, smaller than NMOS switch. BLDIS devices are composed of PN-diode cells, from which the core circuit layout size is decreased by 5%. All BLs are in floating state in standby mode, then in active mode, the activated BLs are discharged to low level in the early timing of the active period by the short pulse BLDIS control timing operation. Row decoder control signal line of GXDEC is used with metal-2 line, same level to WL. Read bias voltage at MBL is targeted by adding the threshold voltage 1.2 V of PN diode and the half snapback voltage 0.6 V – 0.8 V of GST storage layer. The merit of the proposed sense amplifier is removing the coupling noise at VSAREF from sharing with other sense amplifiers.

REFERENCES

- [1] Hee-Bok Kang, et al., *J. of Korean Phys. Soc.*, pp. 490-492, 2004.
- [2] Ovshinsky, S. R., *Phys. Rev. Lett.* 21, pp. 1450-1453, 1968.
- [3] Lee, S. H. et al., *Proc. Symp. VLSI Tech. Dig.*, pp. 20-21, 2004.



Hee-Bok Kang received the B.S. in 1988, M.S. in 1990, and Ph.D. in 2008, the electrical engineering from Korea University, Seoul, Korea.

He joined LG Semiconductor in 1991 and now working for Hynix Semiconductor Inc., as a memory design engineer. He involved in DRAM and SRAM during 1991-1997, in FeRAM since 1998, in DRAM and PRAM during 2004-2007, and in FeRAM embedded RFID tag since 2004.

His current interests are to develop DRAM related researches such as 1T-FeRAM for the alternative next generation capacitor-less 1T-DRAM, FeRAM embedded system on a chip (SOC) and RFID tag, and next generation nonvolatile memories.



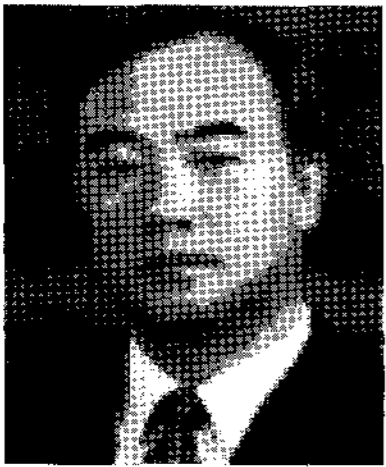
Suk-Kyoung Hong is senior member of technical staff at Hynix Semiconductor Inc., Korea. Since 1997, He has worked for development of FeRAM and now PRAM. He received his BS in metallurgy in 1982 from Kookmin University, his

MS in 1986 from Korea Advanced Institute of Science and Technology (KAIST) and his Ph.D. in 1997 from Seoul National University, Korea, both in materials science and engineering. From 1986 to 1997, he worked as manager in thin film device at Samsung Electronics Co., Ltd., Korea.



Sung-Joo Hong joined Hyundai Electronics in 1992 and now working for Hynix Semiconductor Inc., in developing DRAM, PRAM, and new advanced technology devices. He is currently vice president and leading the Device Division. His

current interests are to develop DRAM, PRAM, and new advanced technology devices related research and development.



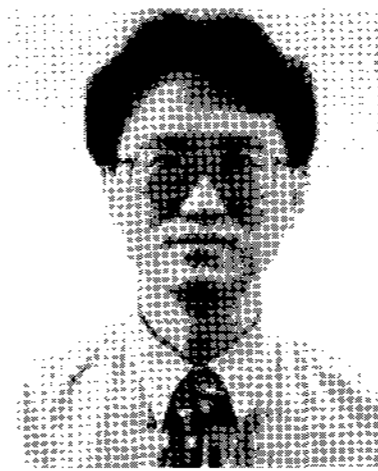
Man Young Sung received the Ph.D. degree in electrical engineering from Korea University in 1981. He is an IEEE member and a professor in Department of Electrical Engineering at Korea University.

He is currently the president of Korea Institute of Electrical and Electronic Materials Engineers.



Bok-Gil Choi received B.S., M.S. and Ph.D. degrees in Electrical Engineering from Korea University, Seoul, Korea, in 1979, 1983 and 1990, respectively. From 1983 to 1985, he worked as a FAB QC Engineer at LG Semiconductor, Korea.

In 1992, he joined the Department of Electrical Engineering, Kongju National University, Gongju, Korea, where he is currently a Professor. In 1996, he was a Visiting Professor with University of Illinois at Chicago (UIC), where he had been involved in the development of MCT IR detectors. His research interests are in the preparation and characterization of transition metal oxide thin films including vanadium and tungsten oxides for sensors and smart windows applications.



Jinyong Chung received the BSEE from Seoul National University in 1974 and MSEE from Korea Advanced Institute of Science and Technology in 1976.

From 1976 to 1978, he worked for Korea Semiconductor Inc, which became Semiconductor Business Unit of Samsung Electronics later, and involved in the design of timepieces and custom CMOS chip designs. Since 1979, he involved in memory design area, and worked for various California semiconductor companies, Western Digital, National Semiconductor, Synertek, Vitelic, and designed CMOS SRAM's, covering from 4K to 64K, mask ROM's, and CMOS DRAM's.

In 1987, he joined LG Semiconductor in Korea, where he developed 256K to 16M DRAM's, and other Standard Logic Products. In 1992, he joined Mosel-Vitellic in San Jose, where he developed high speed DRAM's, and the 256Kx8 High Speed DRAM for graphics application helped the company to go public.

In 1996, he joined Hynix Semiconductor Inc., as a senior vice president and chief architect in Memory R&D. After spending 7 years at Hynix in developing ultra high speed, super low voltage and low power Memory products, novel device research in ferroelectric and magnetic memories, he moved to POSTECH (Pohang University of Science and Technology) in 2003, where he serves as Research Professor. His current interest is to develop ultra low voltage SRAM and 3D & System-in-Package design for testability, and nano-scale CMOS circuit design.