Extraction of Effective Carrier Velocity and Observation of Velocity Overshoot in Sub-40 nm MOSFETs

Junsoo Kim, Jaehong Lee, Yeonam Yun, Byung-Gook Park, Jong Duk Lee, and Hyungcheol Shin

***Abstract*—Carrier velocity in the MOSFET channel is the main driving force for improved transistor performance with scaling. We report measurements of the drift velocity of electrons and holes in silicon inversion layers. A technique for extracting effective carrier velocity which is a more accurate extraction method based on the actual inversion charge measurement is used. This method gives more accurate result over the whole range of V_{ds}, because it does not assume a linear approximation to obtain the inversion charge and it does not limit the range of applicable V_{ds}. For a very short channel length device, the electron velocity overshoot is observed at room temperature in 37 nm MOSFETs while no hole velocity overshoot is observed down to 36 nm. The electron velocity of short channel device was found to be strongly dependent on the longitudinal field.**

***Index Terms*—Carrier velocity, MOSFETs, velocity overshoot, ballistic transport, scattering**

I. INTRODUCTION

Continued success in scaling bulk MOSFETs has brought increasing focus on fundamental performance limits [1]. It has been proposed that drain current is ultimately limited by the rate at which carriers can be transported from source to drain [2]. Thus the effective velocity of the carriers starts to play significant limits in MOSFET performance. The effective carrier velocity is one of the most important effects from the practical point of view as it is directly related with the increase of current drive and transconductance. And the intrinsic cutoff frequency determining maximum device speed is ultimately limited by the effective carrier velocity in velocity saturation region. Therefore, if velocity overshoot can be controlled, the performance of very short-channel MOSFET's can be improved with respect to the performance of long channel transistors. Thus, an accurate value of experimentally determined effective carrier velocity is very important to predict the high-speed and RF performance of MOSFETs. However, quantitative measurements of high field carrier velocities in inversion layers are hard to perform, due to the difficulty of extracting inversion charge along the channel [3]. Typically, assuming a linear approximation $Q_{in} = C_{ox}(V_{gs}-V_{th})$, v_{eff} (effective carrier velocity) is extracted from g_m (intrinsic transconductance). The measurement technique is based on $I_{ds}/(WQ_{in})$ where Q_{in} is determined at V_{ds}=0 V. However, this value of Q_{in} at V_{ds}=0 V leads to velocity extraction errors because the actual incremental charge in the saturation region becomes smaller than the Q_{in} at V_{ds}=0 V. Therefore, in this work, a more accurate method to obtain Q_{in} was used and v_{eff} was successfully extracted at various V_{ds}. And we compare the effective velocity of electrons and holes. Applying this technique to deep-sub-100 nm channel lengths, we report observation of electron velocity overshoot.

II. METHOD

In order to get inversion charge, the following equation was used.

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$$|Q_i(V_{gs},V_{ds})| = \int_{V_{FB}}^{V_{gs}} (C_{gs}+C_{gd})dV_{gs}^* - \int_0^{V_{ds}} (C_{gd}+C_{bd})dV_{ds}^* \qquad (1)$$

Fig. 1 shows the schematic image of the first term and second term of equation (1). The first term is total channel charge at V_{ds} = 0 V. The parasitic capacitance (C_{ov}+ C_{if}+C_{of}) of first term was subtracted. [4] The second term is the amount of charge which will be subtracted from the first term as V_{ds} increases [5]. After de-embedding, parameters in equation (1) were extracted using a Si MOSFET small signal equivalent circuit model.

Then effective carrier velocity in the channel is obtained from $I_{ds}/(WQ_{in})$. ΔL and R_{SD} are extracted using an iteration method in Fig. 2 [4]. ΔL and R_{SD} are 15 nm and 170 Ωμm in NMOS and 17 nm and 250 Ωμm in PMOS were obtained at $|V_{gs}-V_{th}|$=0.6 V respectively.

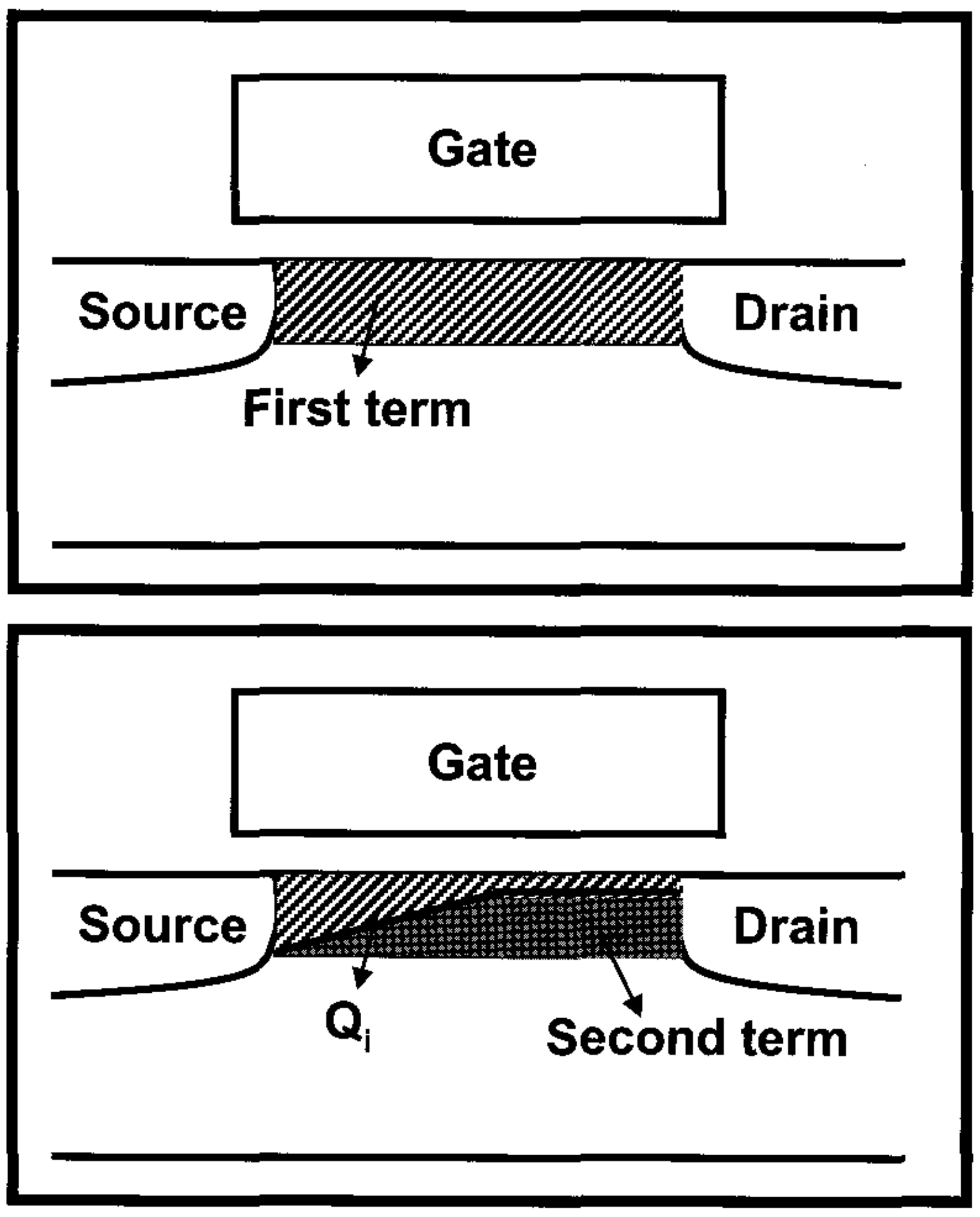


Fig. 1. The schematic images of the first term and second term of equation (1).

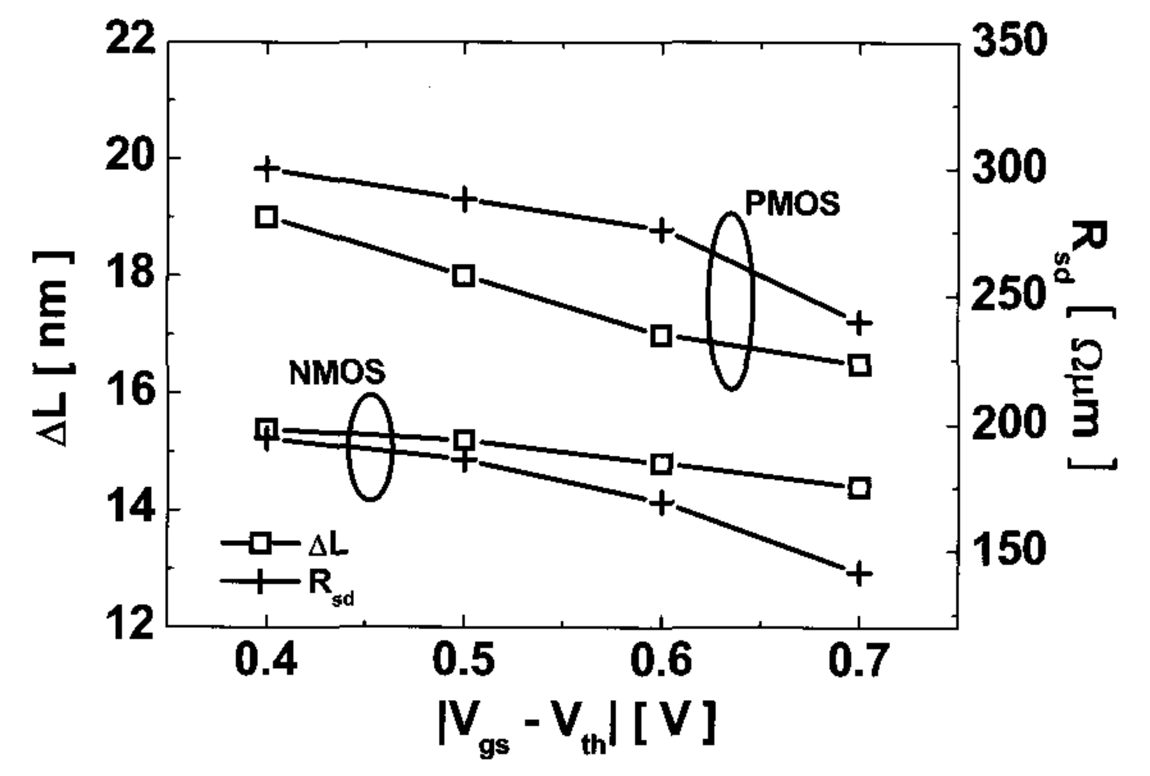


Fig. 2. ΔL and RSD are extracted using an iteration method.

III. RESULTS AND DISCUSSION

S-parameters were measured on MOSFETs in the common source-body configuration with different polysilicon gate lengths. Fig. 3 shows the inversion charge Q_{in} at V_{ds}=0 V for different channel lengths of NMOS and PMOS. This corresponds to the first term of equation (1). Fig. 4 shows the second term in equation (1) of NMOS and PMOS. Fig. 5 explicitly confirms the importance and necessity of considering the influence due to V_{ds}. If Q_{in} is calculated only at V_{ds}=0 V, the effective velocity is found smaller than it actually is. In long channel device, the carriers experienced numerous scattering events between the point of injection into the semiconductor and the point of extraction from the semiconductor. This is equivalent to assuming the total distance through which the carriers travel is much greater than the mean distance between scattering events. Thus the drift velocity of the carriers tends to saturate or approach a field independent

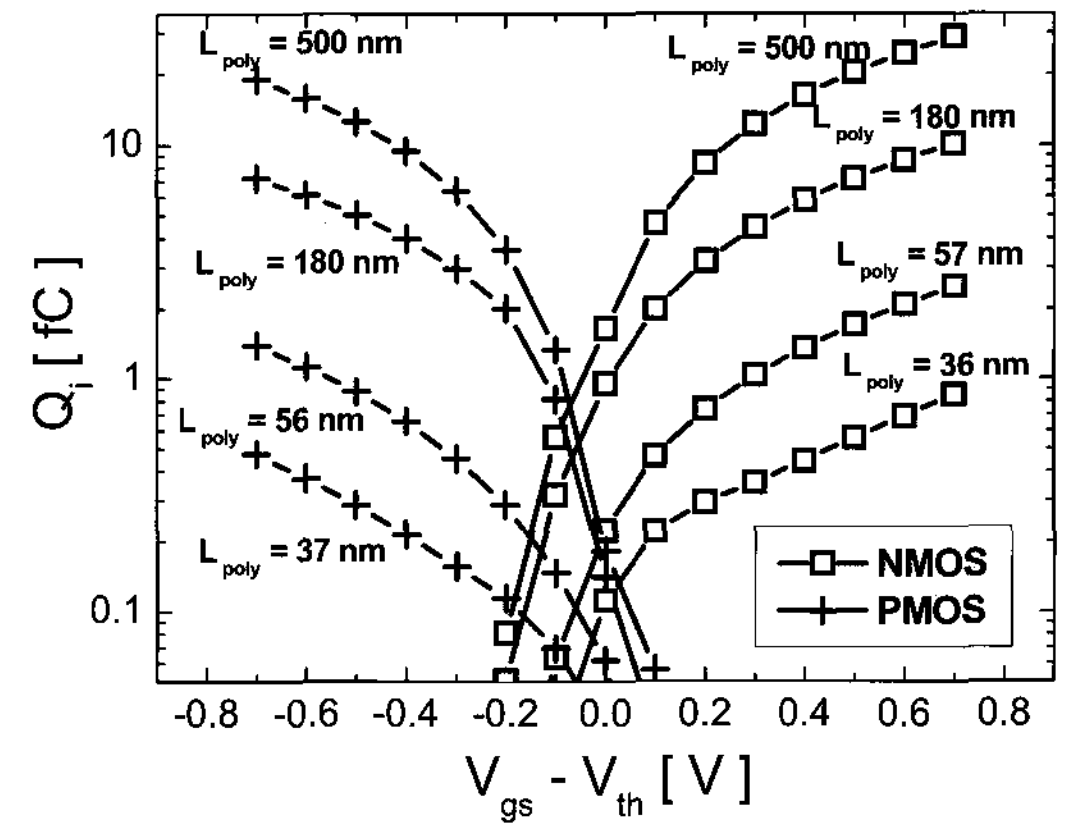


Fig. 3. Total charge in the channel at V_{ds}=0 V. This is the results of the first term of the equation (1).

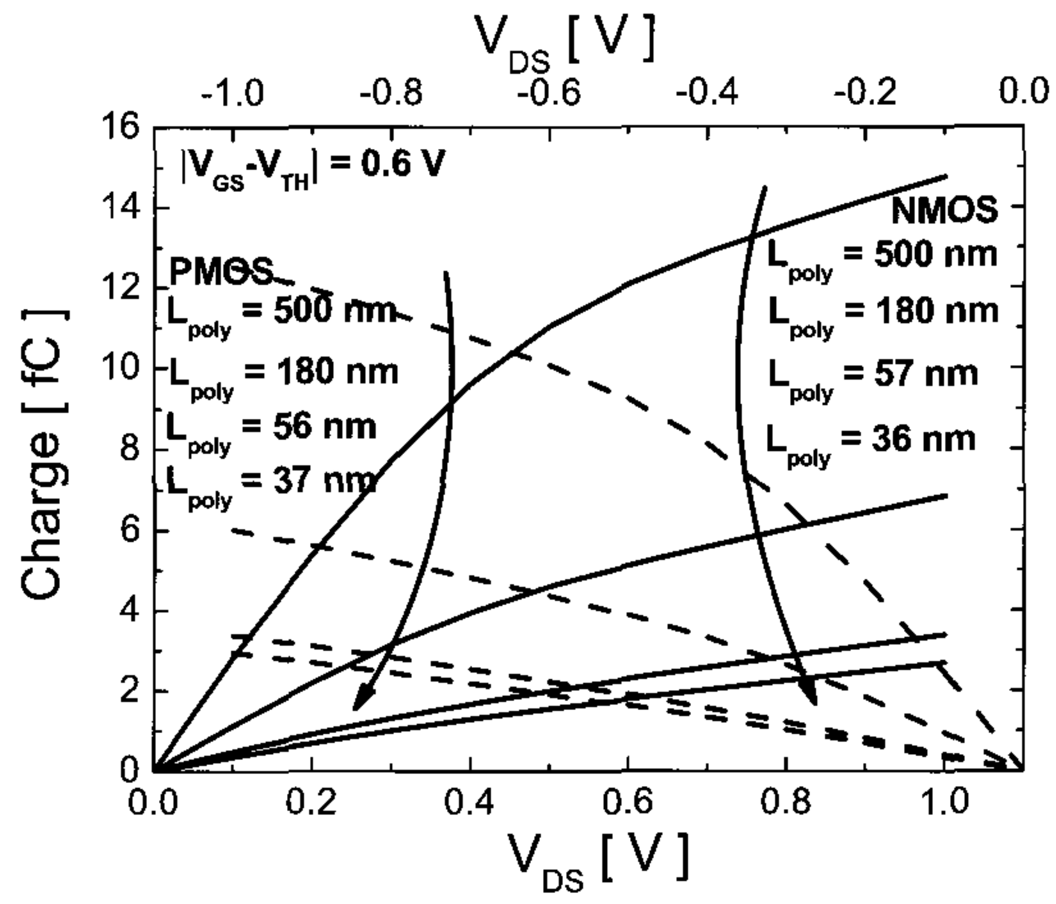


Fig. 4. The second term of the equation (1).

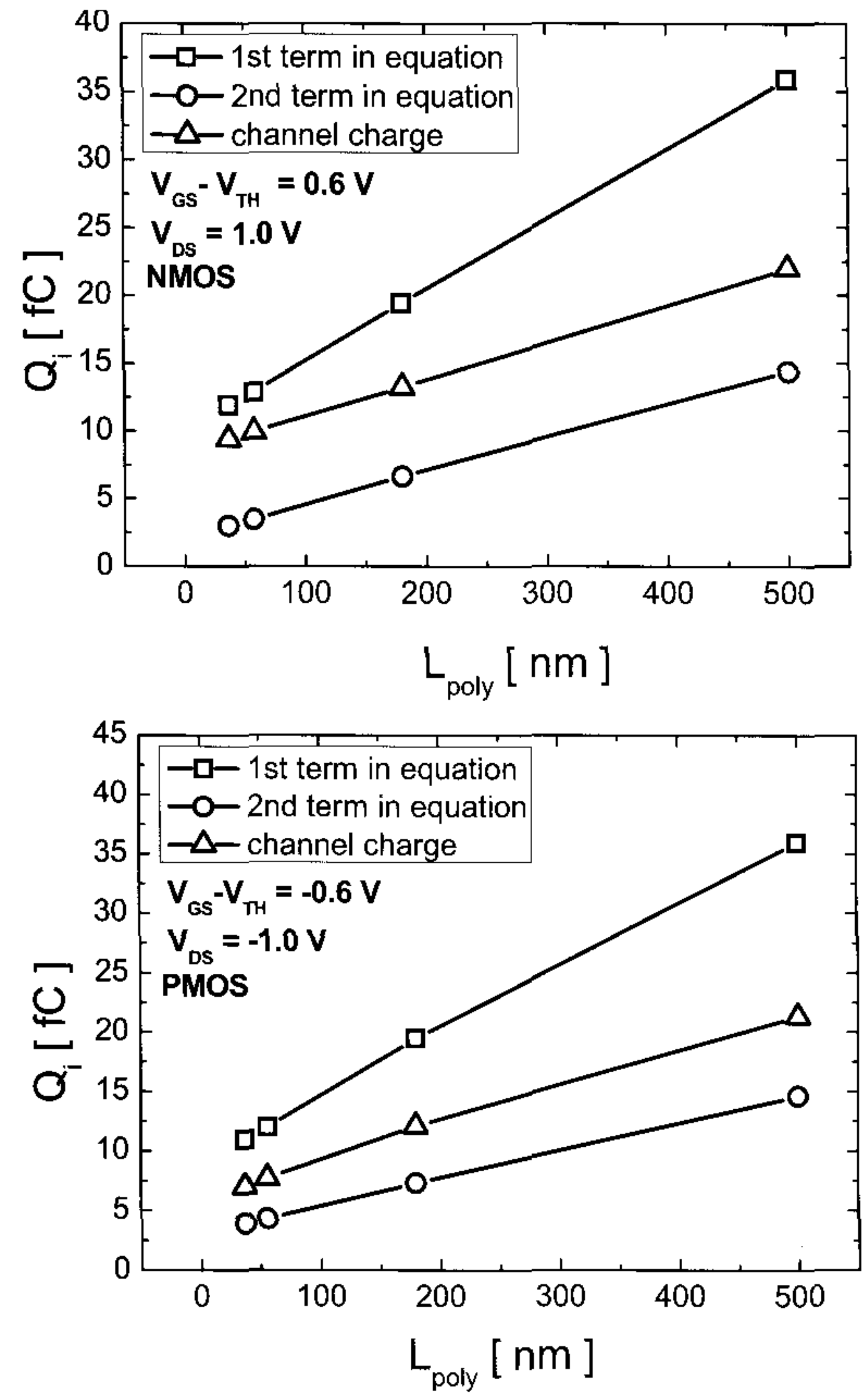
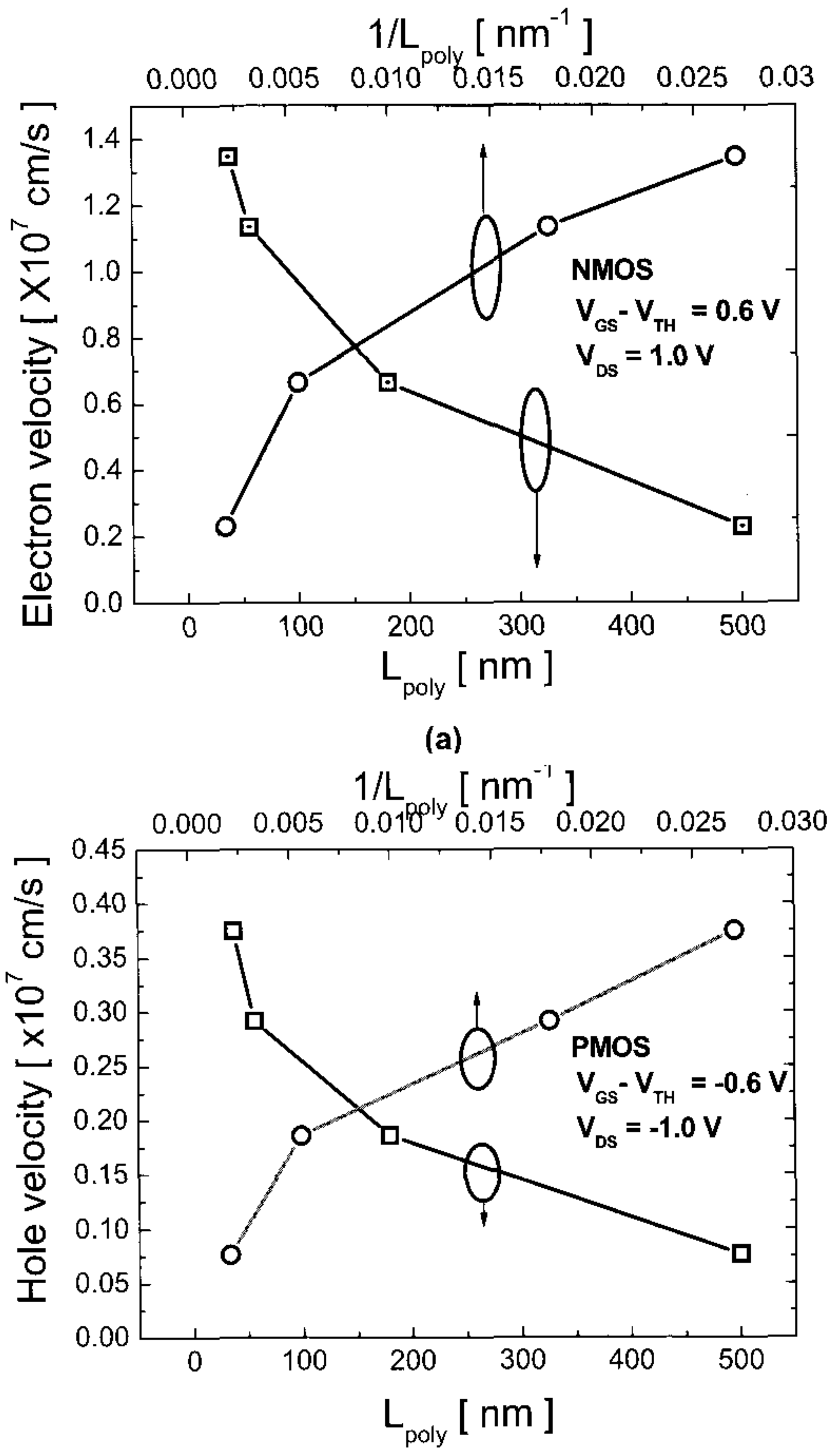


Fig. 5. Channel charge obtained from equation (1) of NMOS and PMOS.

constant value. However, this formalism begins to break down when the carrier travel distance is scaled down. The average carrier velocity can be substantially greater than that expected. In other words, as the longitudinal electric field increases, the electron gas starts to be in disequilibrium with the lattice. There is an insufficient number of phonon-scattering events experienced by the electron during its flight with the result that electrons can be accelerated to velocities higher than the saturation velocity, thus approaching ballistic transport conditions. Extracted effective velocity of electrons and holes are plotted in Fig. 6 (a) and (b) as a function of L_{poly} and $1/L_{poly}$. The linear dependence on $1/L_{poly}$ is observed especially short channel regime. It should be noted the obtained v_{eff} of electrons under L_{poly} of 57 nm exceeds 10^7 cm/s, indicating that the velocity overshoot is observed. And we predict larger electron velocity as device dimensions continue to decrease. On the other hand, no hole velocity overshoot is observed even at 37 nm channel length. The different trend for the ratio of mobility and velocity between electrons and holes is shown in Fig. 7. In contrast to the similar rates of mobility and velocity in long channel device, there is a disparity between mobility and velocity in short channel device. This is probably due to the smaller portion of gradual-channel region in short-channel MOSFETs and also easier generation of hot carriers in NMOSFETs. Fig. 8 shows v_{eff} as a function of V_{ds} for devices with L_{eff} ranging from 36 to 500 nm. It is observed that the effective carrier velocity tends to saturate at long channel device and p-MOSFETs, although electron velocity



(a)

(b)

Fig. 6. Effective carrier velocity as a function of L_{poly}, $1/L_{poly}$.

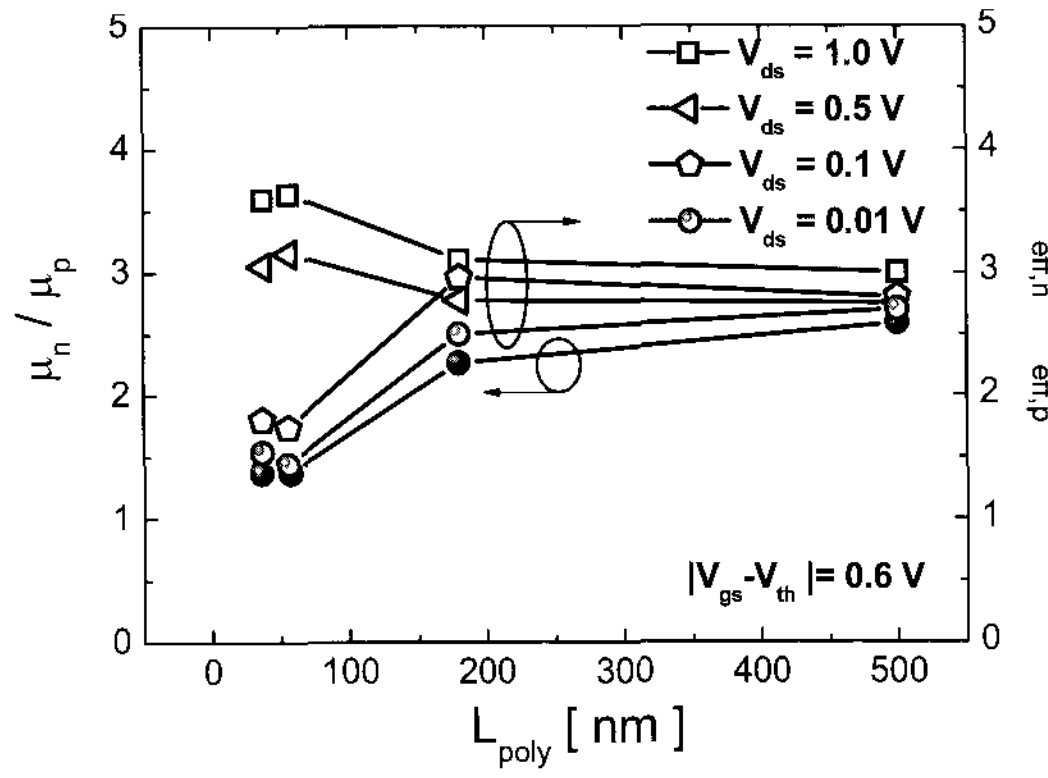


Fig. 7. The difference rate of mobility and velocity between electrons and holes.

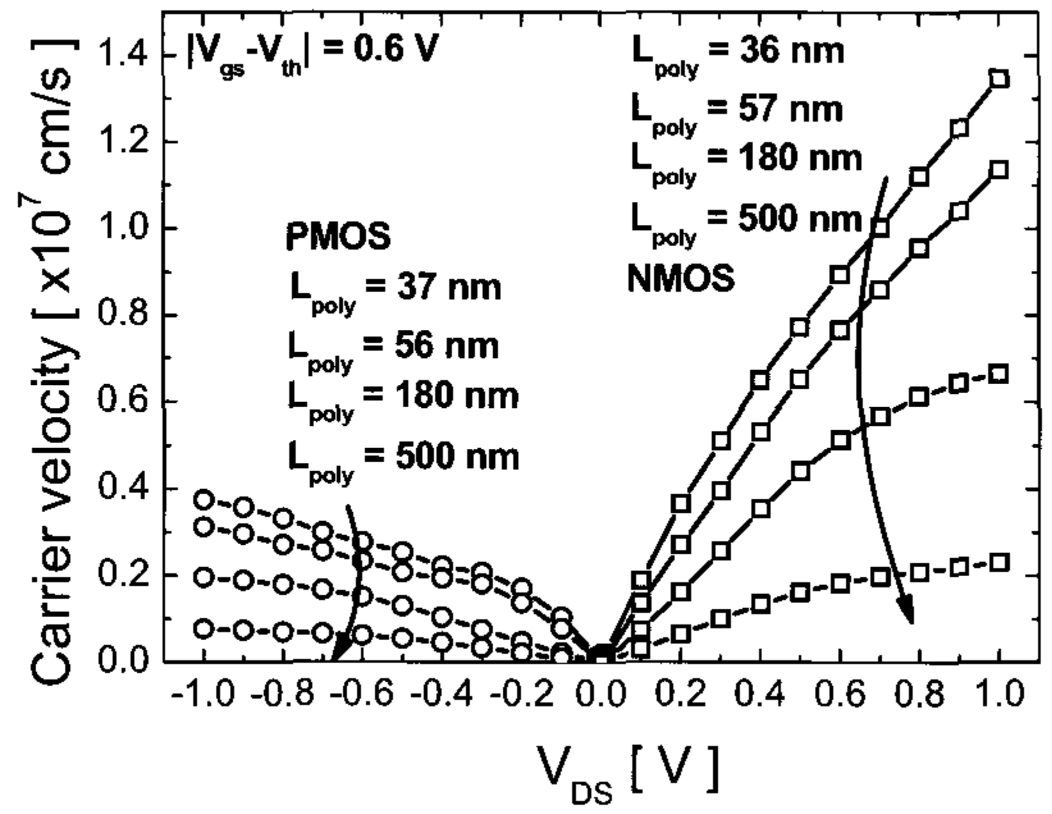


Fig. 8. Effective carrier velocity according to the drain bias in NMOS and PMOS.

overshoot occurs when the gate length is shorter than 60 nm.

IV. CONCLUSIONS

The electron velocity overshoot is observed while no hole velocity overshoot is observed down to 37 nm channel length at room temperature. This indicates more frequent scattering and heavier effective mass of holes compared with electrons. And as the longitudinal electric field increases, there is an insufficient number of phonon-scattering events experienced by the electron during flight with the result that electrons can be accelerated to velocities higher than the saturation velocity, thus approaching ballistic transport conditions.

ACKNOWLEDGMENTS

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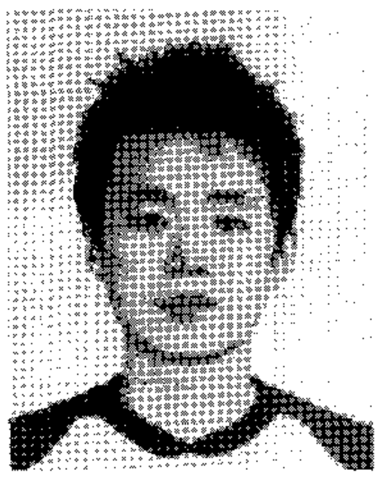

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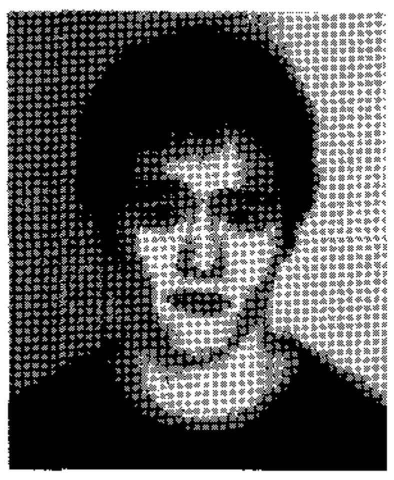

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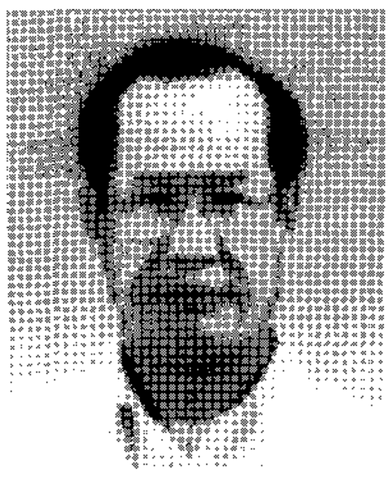

Jong Duk Lee was born in Youngchun, Kyungpook, Korea. He received the B.S. degree in physics from Seoul National University in 1966. He received the Ph.D. degree from the Department of Physics at the University of North Carolina at Chapel Hill in 1975. He served at the Military Communication School as a ROTC officer from 1966 to 1968. He then worked at the Engineering College of Seoul National University as a teaching assistant in the Department of Applied Physics until 1970. He was an Assistant Professor in the Department of Electronics Engineering at Kyungpook National University from 1975 to 1978. In 1978, he studied microelectric technology in HP-ICL at Palo Alto, CA, USA, and soon afterward worked for the Korea Institute of Electronic Technology (KIET) as the director of the semiconductor division. He established the KIET Kumi Facility and introduced the first polysilicon gate technology in Korea by developing 4K SRAM, 32K and 64K Mask ROM's, and one-chip 8-bit microcomputer.

In July 1983, he moved to the Department of Electronics Engineering of Seoul National University, which has been merged to School of Electrical Engineering in 1992, where he is now a Professor. He started to establish the Inter-University Semiconductor Research Center (ISRC) in 1985, and served as the director from 1987 to 1989. He served as the chairman of the Electronics Engineering Department from 1994 to 1996. He worked for Samsung SDI Co., Ltd. as the Head of Display R&D Center for a year on the leave of SNU in 1996. He was the member of the steering committee for IVMC(International Vacuum

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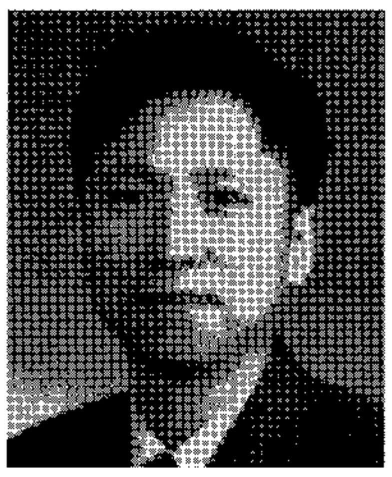

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