Journal of Information Display, vol. 9, no. 1, 2008 

# The Improvement of the Data Overlapping Phenomenon with Memory Accessing Mode

**Jin Wook Yang[*a], Doo Hyung Woo[*a], Dong Hwan Kim[a], and Junsin Yi[*b]**


## Abstract

Mobile phones use the embedded memory in LDI (LCD Driver IC). In memory accessing mode, data overlapping phenomenon can occur. These days, various contents such as DMB, Camera, Game are merged to phone. Accordingly, with more data transmission, there would be more data overlapping phenomenon in memory accessing mode. Human eyes perceive this data overlapping phenomenon as simply horizontal line noise. The cause of the data overlapping phenomenon was analysed in this paper. The data overlapping phenomenon can be changed by the speed of data transmission between the host and LDI. The optimum memory accessing position can be defined. This paper proposes a new algorithm for avoiding data overlapping.


**Keywords** : Memory accessing mode, Data overlapping phenomenon, Hold-type display, Data transmission

## 1. Introduction

Mobile phones mainly use memory accessing modes such as System I/F, MDDI(Mobile Display Digital Interface), etc. rather than the memory non-accessing mode such as Video I/F. [1, 2] In the memory accessing mode, LDI has the same size memory with LCD's resolution. The host does not have any information about the position of the display scan. The display logic of LDI does not have any information about the position of the writing scan either. Therefore the host and the display logic of LDI are supposed to access the memory of LDI independently. The host just writes data into memory whenever there are some changes of data. The display logic of LDI only reads data from memory with the rate of frame frequency. In the memory non-accessing mode input data passes from line buffer to panel because LDI has only a horizontal line buffer and no memory. [3] There are three reasons for using the memory accessing mode. First, mobile phones usually have limited memory. The amount of data transmission depends on the interface. The host must transmit the data periodically without regard to the change of the data in the memory non-accessing mode. But the host does not have to transmit the data if there is no change in the data in the memory accessing mode. To move picture. The memory accessing mode needs less data than the memory non-accessing mode. Second, the memory non-accessing mode consumes more power than the memory accessing mode because there are more logic swings than the memory accessing mode. Therefore the memory non-accessing mode is not suitable for market circumstance which needs low power consumption. Third, the main purpose of mobile phone has been to call someone. There have been few changes of images in the calling mode such as dialing, battery, and watch in the screen. So the memory accessing mode is preferred. However, various contents that need a large amount of data are merged to phones these days. More data transmission causes more data overlapping phenomenon in the memory accessing mode. This paper analysed the cause of the data overlapping phenomenon and proposed a method of preventing this phenomenon.

Manuscript received December 10, 2007; accepted for publication March 25, 2008.
* Member, KIDS
Corresponding Author : Jin Wook Yang
[a]Samsung Electronics LCD Network Mobile LCD development team, San #24, Nongseo-Dong, Giheung-Goo, Youngin-City, Kyunggi-Do, 449-711, Korea.
[b]The department of Information and Communication Engineering, Sungkyunkwan University, 300, Chunchun-dong, Jangan-Gu, Suwon-City, Kyunggi-Do, 440-746, Korea.
**E-mail** : jinwook.yang@samsung.com
**Tel** : 81-031-209-1144 **Fax** : 81-031-209-4876

## 2. Analysis of data overlapping phenomenon

The memory non-accessing mode such as Video I/F makes images clear simply by using over 60Hz frame frequency. The memory accessing mode with a few of data (15

~ 30Hz) can make images clear by driving LCD's frame frequency over 60Hz. This mode can cause data overlapping phenomenon because the memory accessing positions are different between the host and the display logic of LDI. The data overlapping phenomenon is not a serious problem if few changes are made to the data. However, the data overlapping phenomenon is a serious problem if there is a lot of data transmission in this mode. Human eyes perceive the data overlapping phenomenon as a horizontal line noise. LCD is a hold-type display device. If there are some changes to the data, two different images overlap one another during one frame. Fig. 1 explains the relation between the writing scan and the display scan according to the memory accessing position. Y-axis of Fig. 1 corresponds to LCD's gate line and X-axis of Fig. 1 corresponds to time. If there are no changes in the images, the host stops the communication with LDI in the memory accessing mode. The host writes data into memory only if there are changes to the image. At this time, the host has access to memory without regard to the position of the display scan because the host and the display logic of LDI have a seperate access to the memory. For example, the frame data are composed of 8 lines as shown in Fig. 2. Image ⓨ is sent after image ⓧ in Fig. 2. When the data writing scan does not cross over the data display scan like ① in Fig. 1, the state of memory is data ⓐ in Fig. 3 during displaying nth frame. And the state of memory is data ⓑ in Fig. 3 during displaying the (n+1)th frame. The change in the images during the (n+1)th frame is shown Fig. 4. When the data writing scan crosses over the data display scan like ② in Fig. 1, the state of memory is data ⓒ in Fig. 5 during displaying the nth frame. The state of memory is data ⓓ in Fig. 5 during displaying (n+1)th frame. The state of memory is data ⓔ in Fig. 5 during displaying (n+2)th frame. The change in the images during (n+1)th frame is Fig. 6. The change in the images during (n+2)th frame is Fig. 7. If the data writing scan does not cross over the data display scan as in ① in Fig. 1, 1 frame is spent to change image. However, 2frames are spent to change the image if the data writing scan crosses over the data display scan like ② Fig. 1. Frame frequency is usually 60Hz. When using the writing scan ① in Fig. 1, the image is changed at the rate of 60Hz. When using the writing scan ② in Fig. 1, image is changed at the rate of 30Hz. Therefore it is not difficult to find the data overlapping phenomenon in the writing scan ② in Fig. 1. In camera mode, MPU (microprocessor unit) of phone processes the camera events prior to other events. When a camera detects the images in Fig. 8, (n+2)th data can be written into memory before all of (n+1)th data is written into memory. This is a serious problem today. LCD displays image ⓑ in Fig. 10 during when displaying the (n+1)th frame and displays image ⓒ in Fig. 10 when displaying the(n+2)th frame. Image ⓒ is composed of three data. Thus the data overlapping phenomenon is easily recognized when next frame data are written into memory before all of present frame data is written into memory.

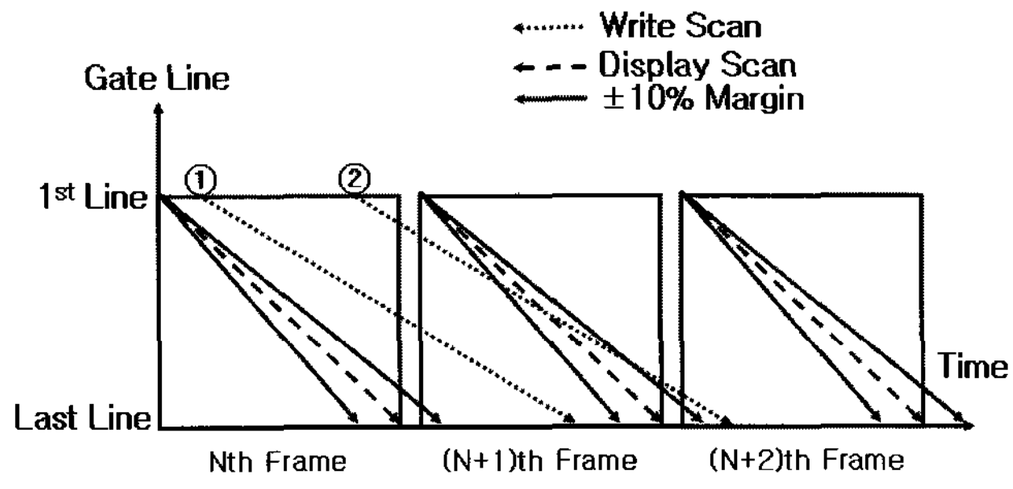


**Fig. 1.** The relation between the writing scan and the display scan according to the memory accessing position.

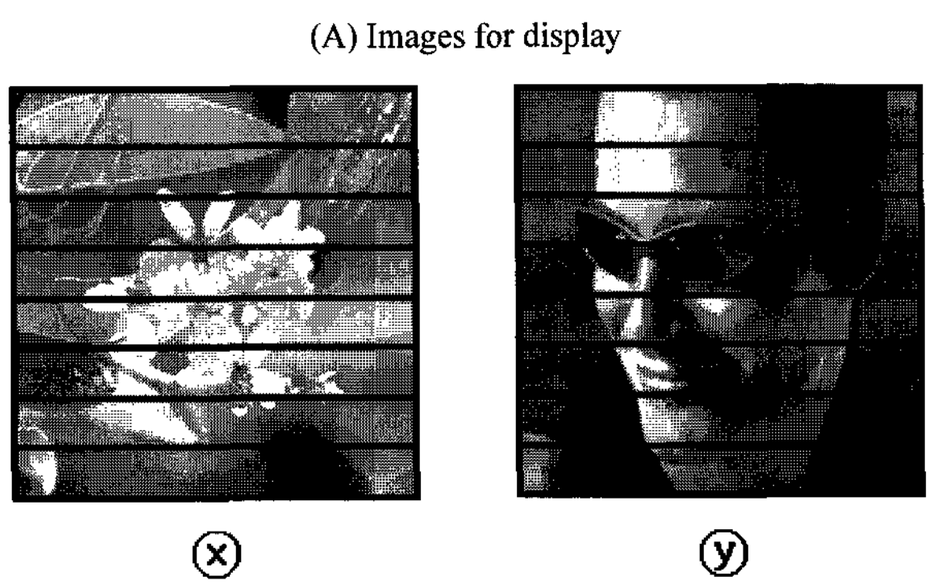


**Fig. 2.** Images for display.


**Fig. 3.** The state of memory when the writing scan does not cross over the display scan.

**Fig. 4.** The change of image during (N+1)th frame when the writing scan does not cross over the display scan.


**Fig. 5.** The state of memory when the writing scan crosses over the display scan.

**Fig. 6.** The change of images during (N+1)th frame when the writing scan crosses over the display scan.

**Fig. 7.** The change of images during (N+2)th frame when the writing scan crosses over the display scan.

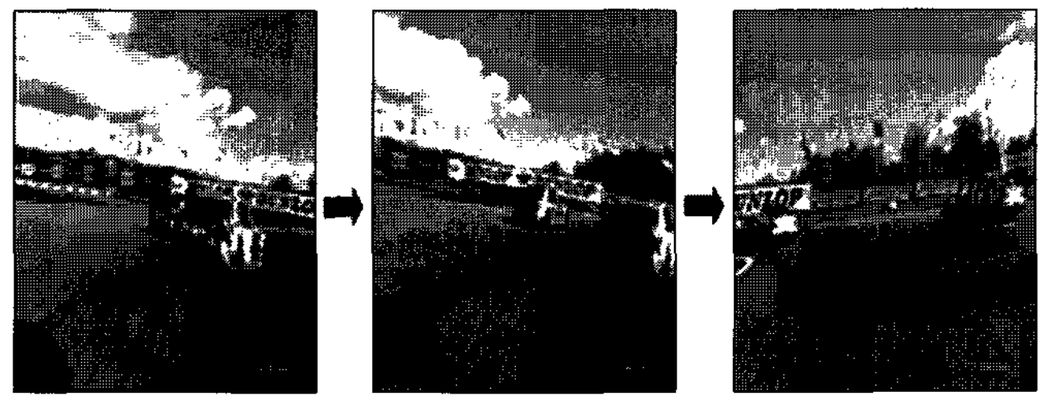

**Fig. 8.** Moving images for camera.

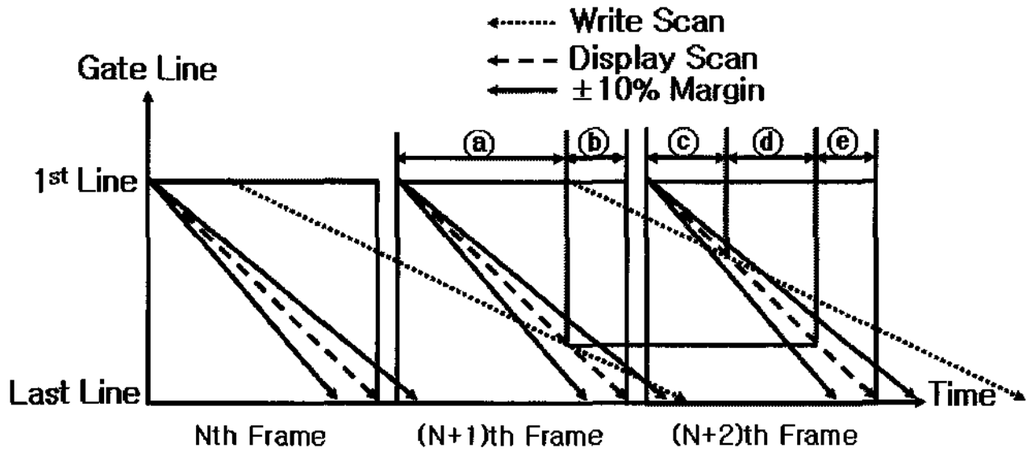


**Fig. 9.** Te relation between the writing scan and the display scan when next frame data is written into memory before all of pres data is written into memory.

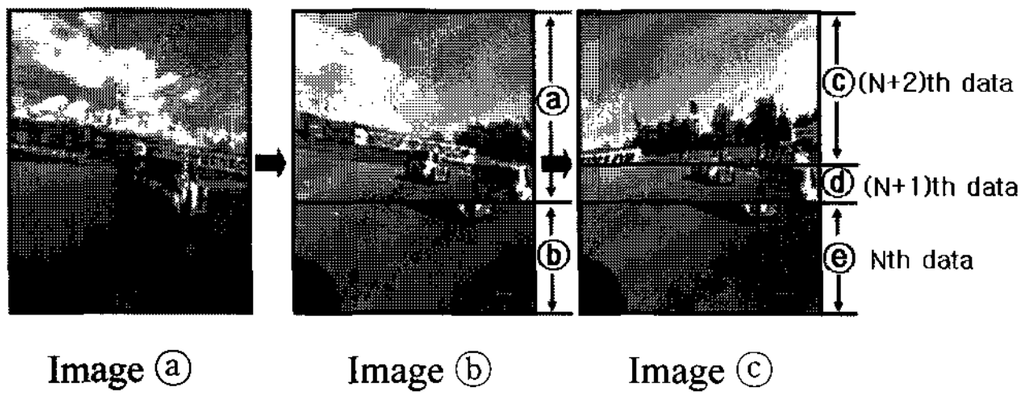


**Fig. 10.** The change of images when next frame data is written into memory before all of present frame data is written into memory.

## 3. Proposed algorithm

FLM (Frame Leading Marker) test signal of LDI has been used to avoid the data overlapping phenomenon so far. FLM is only generated during the porch period. And it is impossible to control the position of FLM. FLM is a monitoring signal to avoid interference with IC's ram read timing for displaying LCD and the internal operation timing for MPU(Microprocessor unit) access. The host must receive this signal and find the optimum memory accessing position to avoid the data overlapping phenomenon in the way of trial and error. If the host is changed, the memory accessing position has to be found again. Moreover, finding the accessing position is not easy for all cases because the host can not check the position of the display scan. The new algorithm can calculate the memory accessing position automatically and modify the memory accessing position according to the host. The host writes the data into memory when it receives the accessing signal from LDI. [4] Fig. 11 shows the relation between the data writing scan and the data display scan in all occasions. Case1 is the case where the writing rate is slower than the display rate. In this case, the interrupt signal should be sent to the host because the data overlapping phenomenon is inevitable. Case2, is the

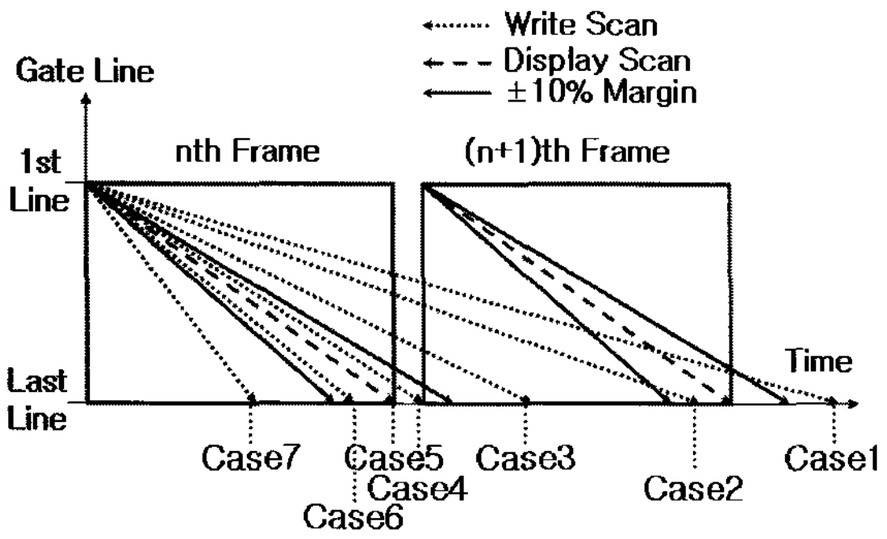


**Fig. 11.** The relation between the data writing rate and the data display rate in all occasions.

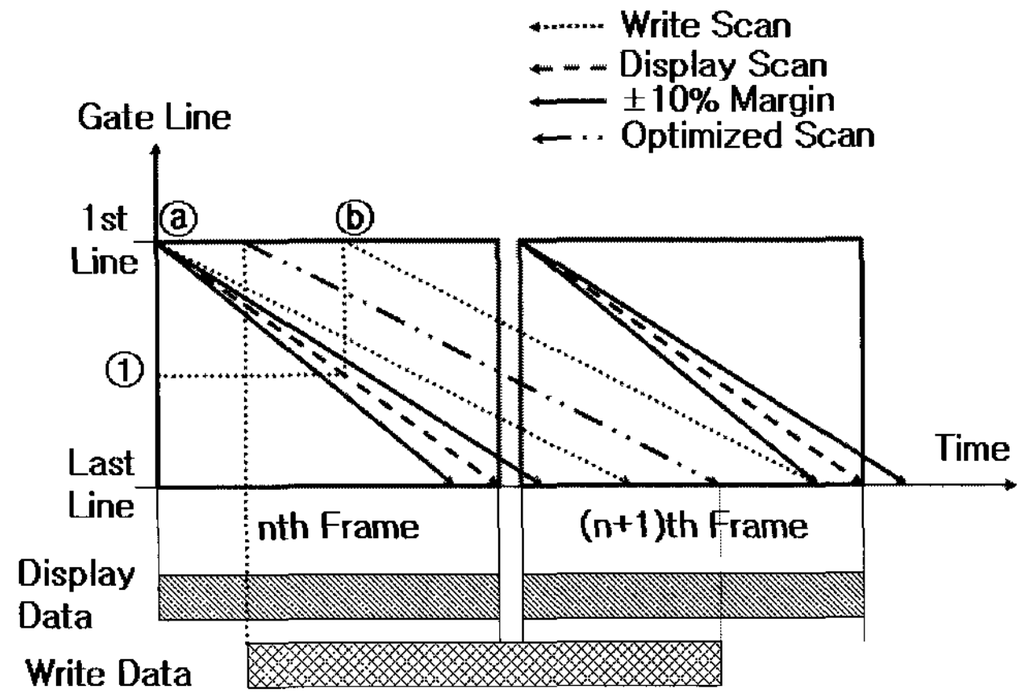


**Fig. 12.** The optimum memory accessing position in Case3.

case where the writing rate is faster than +10% margin scan. In the case, if the margin of LDI is considered, the interrupt signal should be sent to the host. As it is possible that the data overlapping phenomenon may occur. In case3 see Fig. 12, the optimum memory accessing position is the middle of the 1st gate line and gate line ①. The first gate line is the position where the start point of the display scan ⓐ is the same as the starting point of -10% margin scan in the current frame. Gate line ① is the position where the last point of the display scan ⓑ is the same with the last point of +10% margin scan in the next frame.

In case of ⓑ Gate Line (①) = Gate Resolution*2+Porch-Gate Resolution*10%-Write Line

∴ the accessing position in Case3 = ①/2 = (Gate Resolution*2+Porch-Gate Resolution*10%-Write Line)/2

(Write Line means the data writing time is measured in terms of gate line.)

In cases 4～6 of Fig. 13, the optimum memory accessing point is the middle of the position between gate line ② and gate line ③. Gate line ② is the position where the last point of the display scan ⓒ is the same as the last point of -10% margin scan in the current frame. Gate line ③ is the position where the last point of the display scan ⓓ is the same as the last point of +10% margin scan in the next frame.

In case of ⓒ, Gate Line (②) = Gate Resolution + Gate Resolution x 10% - Write Line

In case of ⓓ, Gate Line (③) = Gate Resolution x 2 + Porch - Gate Resolution x 10%-Write Line

∴ The accessing position in case4 ~6 = (②+③)/2 = (Gate Resolution x 3 + Porch - Write Line x 2)/2

The calculation of the accessing position is the same as that for case4 to case6, except that the condition of each case is different. In case7 see Fig. 14, the optimum memory accessing point is the middle of the position between gate line ④ and the first gate line in the next frame. Gate line ④ is the position where the last point of the display scan ⓔ is the same as the last point of -10% margin scan in the current frame. The first gate line in the next frame is the position where the starting point of the display scan ⓕ is the same as the start point of +10% margin scan in the next frame.

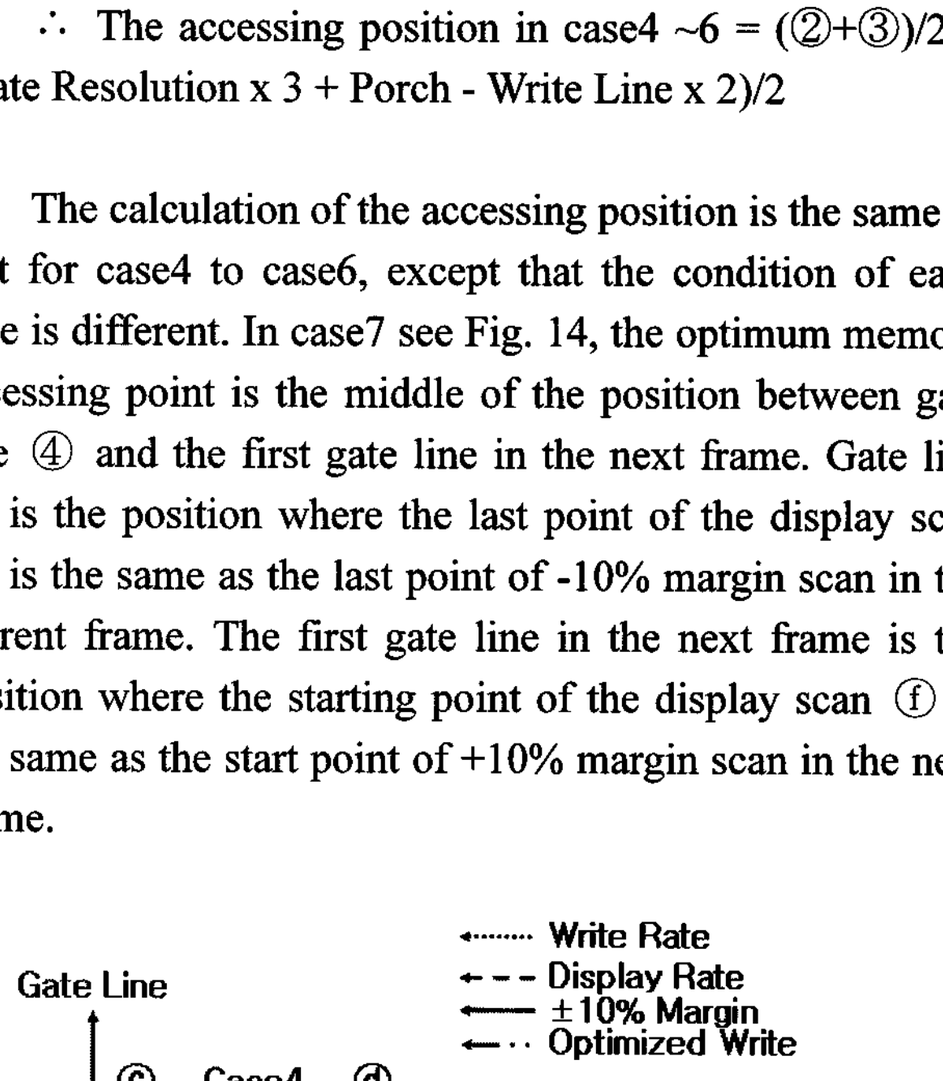


**Fig. 13.** The optimum memory accessing position in Case4~6.

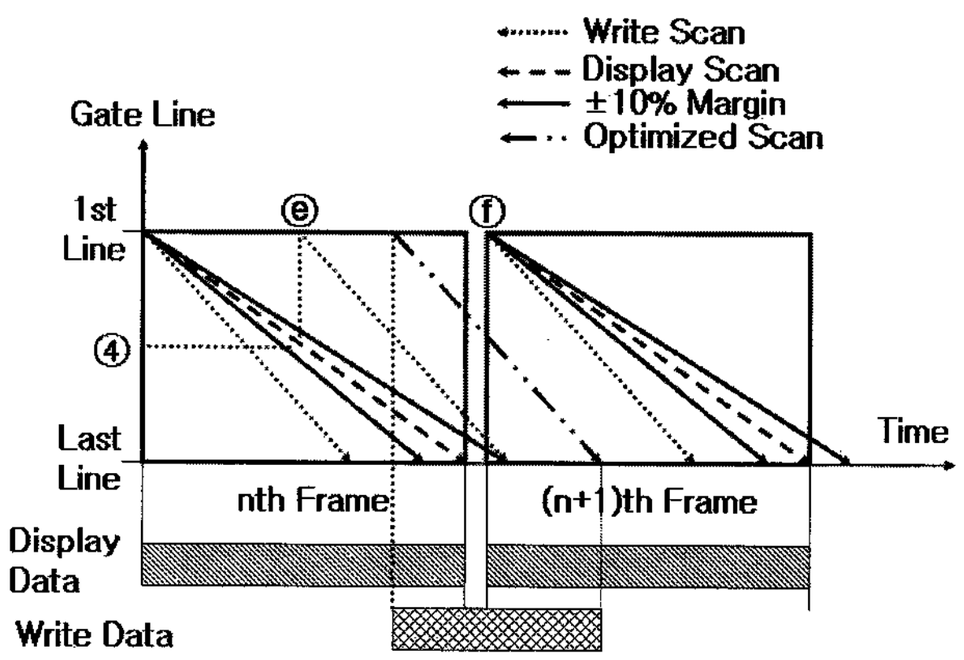


**Fig. 14.** The optimum memory accessing position in Case7.

In case of ⓔ Gate Line (④) = Gate Resolution + Gate Resolution x 10% - Write Line

In case of ⓕ. Next Frame 1st Line = Gate Resolution + Porch

∴ The accessing position in case7 = (④ + Gate Resolution + Porch)/2 = (Gate Resolution x 2 + Porch + Gate Resolution x 10%-Write Line)/2

In cases 3 and 4 the data writing rate is slower than the data display rate. If the memory accessing signal is generated in every frame as shown in Fig. 15, (n+1)th data is written into memory before all of nth data is written into memory. Therefore the memory accessing signal should be sent in every 2 frames or more. In cases 5, 6 and 7, the memory accessing signal can be sent to every frame because the data writing rate is the same as or faster than the data display rate. In addition, it is possible to control the amount of the data transmission by increasing the period of memory access if the data need not be updated frequently. Fig. 16 shows the State Machine based on this algorithm. Fig. 17 shows the block diagram for simulation. Clk_Generator block receives the information about the writing rate and the display rate from setting block, and then generates the writing clock and the display clock. The setting block has the information about writing rate, display rate, LCD's resolution, porch size and user's settings. From setting block, State Machine block receives writing rate, display rate, LCD's resolution, overflow, user's settings and porch size, and then calculates the memory accessing position. This block transmits the accessing position and the interrupt signal to Flag Generator block that generates the memory accessing signal. Flag Generator block receives the optimum memory accessing position from State Machine block, and also receives the display scan position from Ram&Display block. When the accessing position is the same as the display scan position from Ram&Display, Flag block generates an accessing signal. The accessing signal is maintained within one gate line because the time taken to access a signal is set for gate line. When Flag block receives the interrupt signal from the State Machine, it raises the flag signal to high and informs the system of the overflow state. System block writes data into Ram&Display Block in accordance with the writing clock and chip select signal. Ram&Display block writes data into ram sequentially at the rising point of writing clock and reads the ram's data at the rising of display clock.

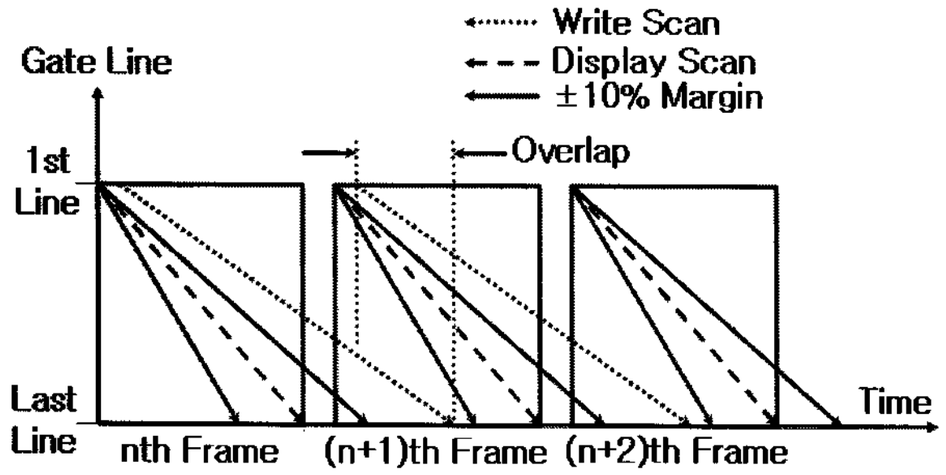


**Fig. 15.** The optimum memory accessing position in Frame.

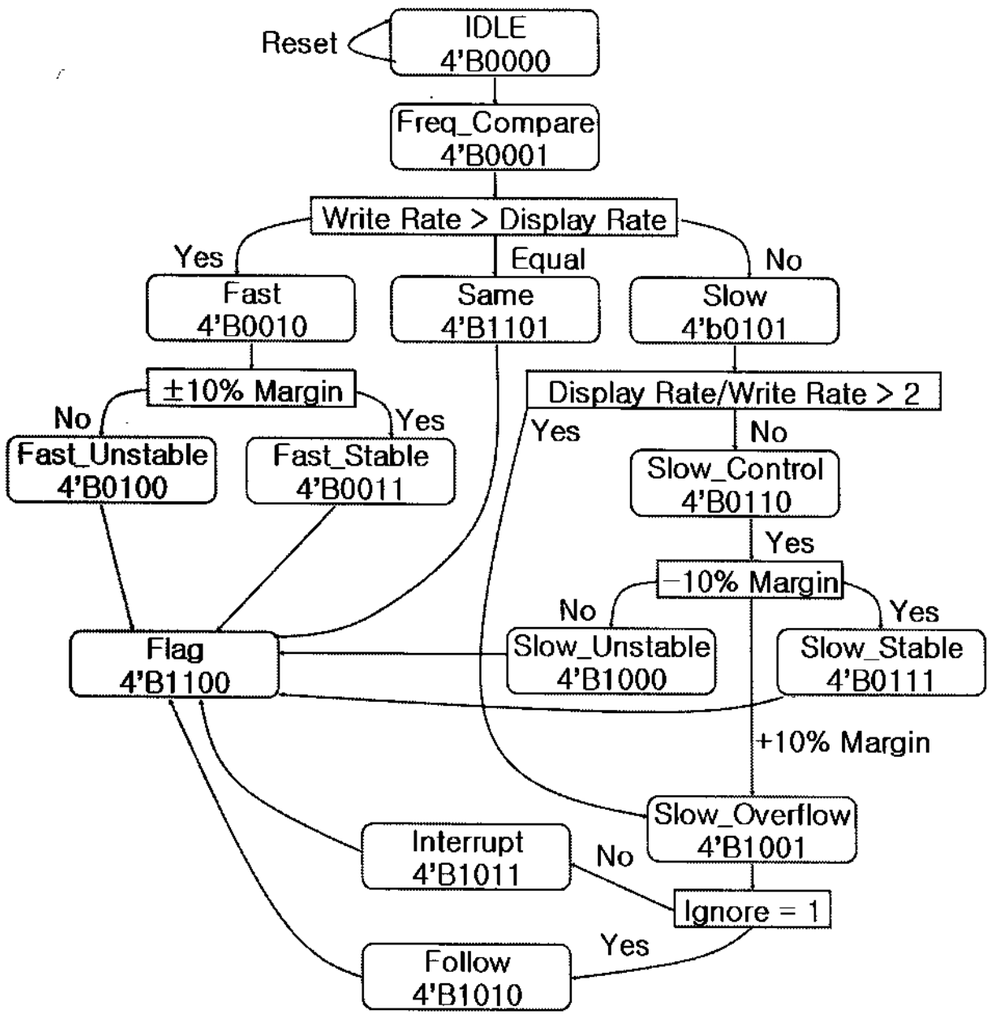


**Fig. 16.** State Machine Chart.

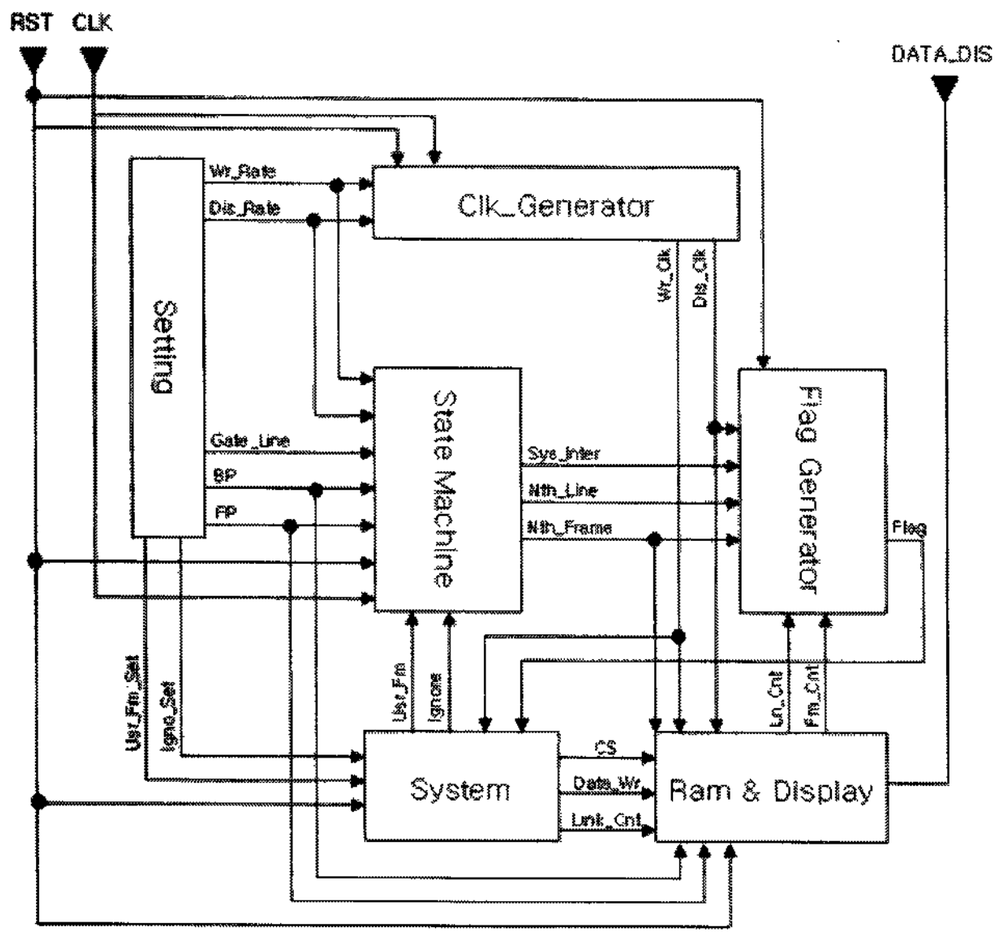


**Fig. 17.** System block diagram for simulation.

## 4. Results and discussions

The algorithm for the accessing signal generation was verified by using a verilog. Fig. 18 shows the result of SM (State Machine) logic's simulation by using the Modelsim tool. The writing rate is 40Hz and the display rate is 60Hz as shown in Fig. 18. The state progresses in the following sequence: 'IDLE→ Freq_Compare→ Slow→ Slow_Control→ Slow_Stable→ Flag State. The calculation of the memory accessing position ends before Flag State in SM chart. The memory accessing position is generated at Flag State. In Fig. 19 the accessing signal is generated at the right position of memory access. After Flag Generator logic receives the accessing position (Gate Line = 30, Frame = 2) and the display scan position, it compares the memory accessing position with the display position and generates the accessing signal. The memory accessing signal is maintained for one gate line time. Fig. 20 shows the results of all occasions. DATA_OUT is the transmitted data from LDI to Panel. DATA_IN is the transmitted data from the host to LDI. FLAG is the accessing signal. NTH_LINE is the accessing position in gate line. NTH_FRAME is the accessing position in frame. In Case1, Flag Logic transmits the interrupt signal to the host and requests the host to modify the data writing rate. Display logic updates image in every 4frames (60/4=15Hz) when the host ignores overflow and needs few data. Flag signal, the accessing signal, is generated in every 4frames. The host has access to memory at the position where Flag signal appears. Case2 is similar with Case1. The accessing signal is generated in every 3 frames because user's frame is set to 3. In case3, 4, Flag signal is generated in every 2 frames. Flag signal prevents writing next frame data before all of present frame data is written into memory. And this signal does not make the writing scan cross over the display scan. Therefore data overlapping phenomenon does not happen. In case5, the date display rate is the same with the data writing rate, so Flag signal can be generated in every frame. In case 6,7,the data writing rate is faster than the data display rate, so it is possible to write data in every frame. Table 1 and Fig. 21 show that the written data extends over 2 frames. As the writing rate is faster, the writing time is shorter. Therefore the accessing position can be moved to the later position of frame. The display data are already updated in the next frame because the accessing position of the host is located behind that of the display logic in LDI.

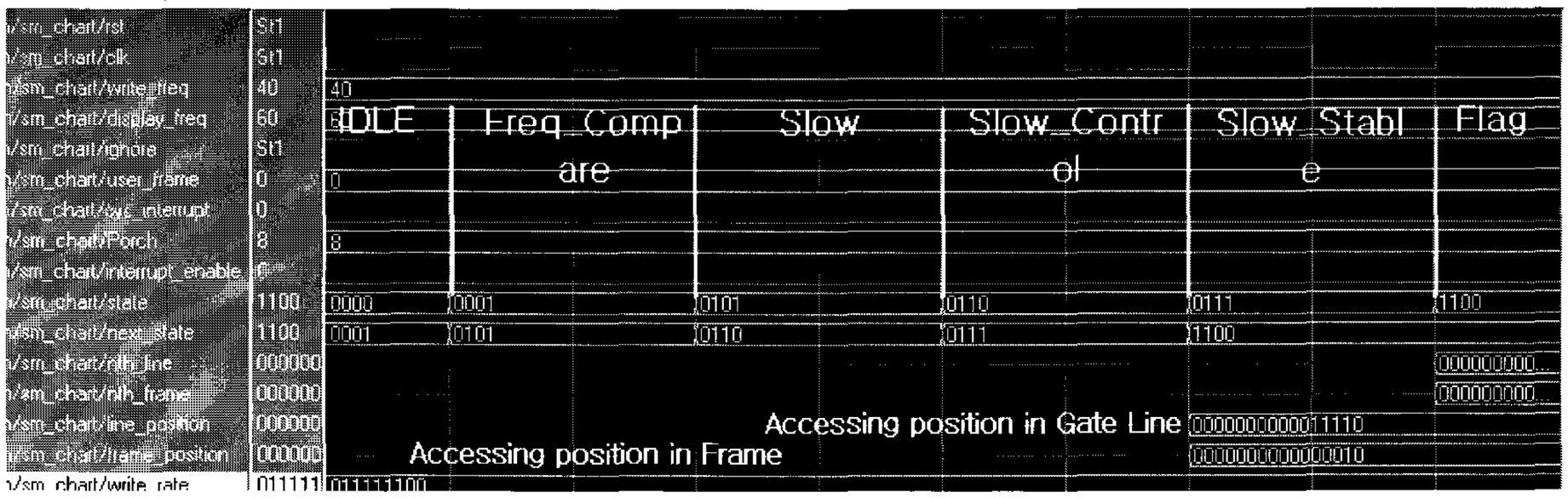


**Fig. 18.** The flow of states in State Machine Logic.

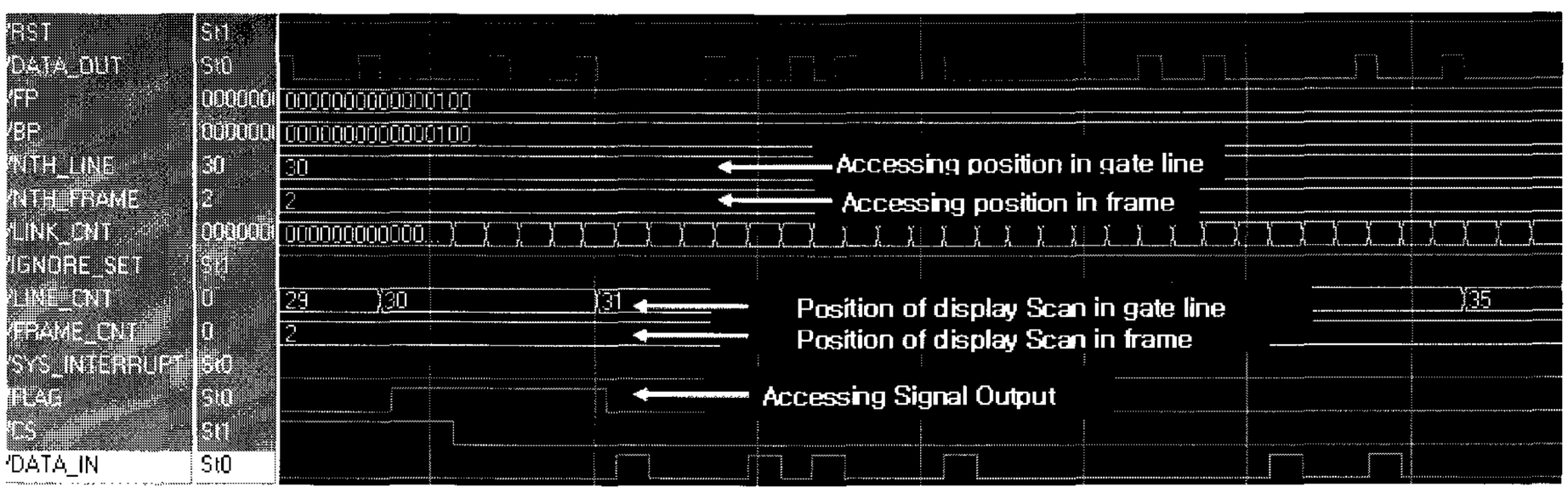


**Fig. 19.** The timing of Flag Generator Logic.

So the data overlapping phenomenon does not happen. Table 2 is the prospective data when the memory accessing signal generation logic is merged to LDI. There are little increases of the current consumption. The area of this logic is very small. The accessing signal generation logic with small resource can remove the data overlapping phenomenon.

**Table 1.** The range of the written data in 160 gate resolution (Display Freq. = 60Hz).

| Writing Freq.(Hz) | The range of the written data (as gate line position) | |
|---|---|---|
| | The starting position | The ending position |
| 40 | 30 | 271 |
| 45 | 44 | 258 |
| 50 | 55 | 247 |
| 55 | 61 | 235 |
| 60 | 76 | 236 |
| 65 | 89 | 236 |
| 70 | 100 | 237 |
| 75 | 105 | 233 |
| 80 | 105 | 229 |
| 85 | 113 | 225 |
| 90 | 116 | 223 |

**Table 2.** The prospective data when the memory accessing signal generation logic is merged to LDI (Tool: Altera, Cyclone II [EP2C5F256C6]).

| | The accessing signal generation Logic | Normal QVGA Total Logic in LDI |
|---|---|---|
| The number of Gate Logic | 1392 | About 68000 |
| The rate of area in LDI | 0.2% | About 10% |
| Logic current | 0.02uA | About 0.83uA |
| Analogue current | 86uA | About 4.3mA |
| Dynamic range | 2 | - |

(∴ Dynamic range = Maximum Write Rate / Display Rate)

## 5. Conclusions

This paper analysed the cause of the data overlapping phenomenon in memory accessing mode and proposed the new algorithm to avoid this phenomenon. The new algorithm assigns the accessing signal to the host when there are data transmissions from the host to LDI. The accessing position is decided by the relation between the data writing rate and the display rate. Based on the result of design and verification of algorithm, the data overlapping phenomenon

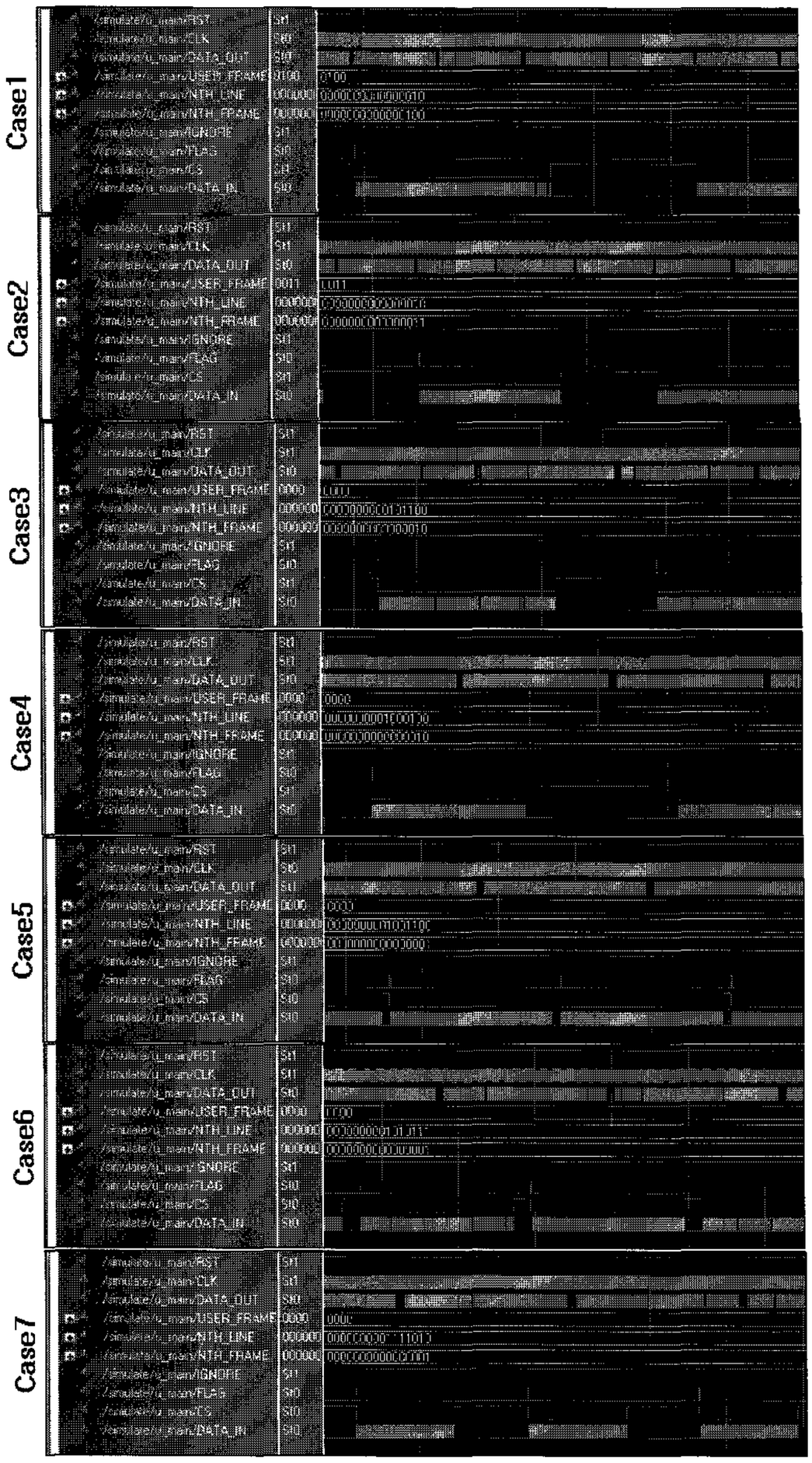


**Fig. 20.** The simulation results of the memory accessing signal.

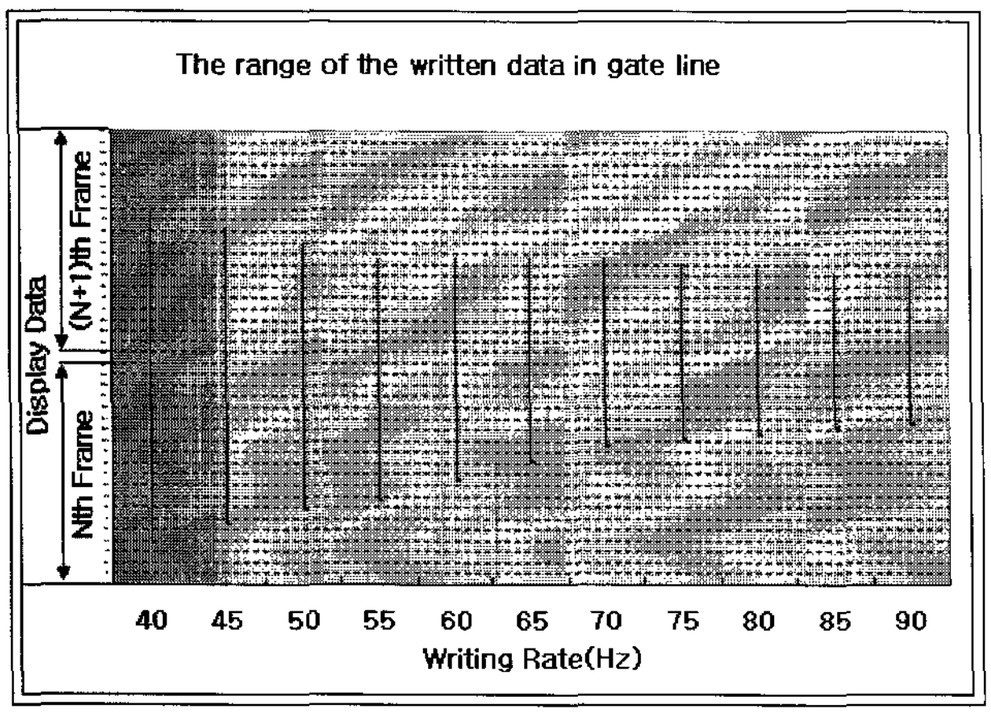


**Fig. 21.** The range of the written data in gate line.

could be prevented in all occasions. SM Logic and Flag Logic were newly established. By using these two additional logics, it is possible to design the memory accessing logic.

## References

[1] Flat Panel Display Interface Standard Version 1.0 VESA, August 18, 1996

[2] Mobile Display Digital Interface Standard Version 1.0 VESA, July 23, 2004.

[3] S. S. Kim and S. D. Lee, *Display Engineering* I(Chung bum , Seoul , 2000), p.226

[4] J. W. Yang, Y. S. Park and J. I. Han, Improvement of the data overlapping in asynchronous data transmission mode, Patent No.P2006-0095977, September 9, 2006