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The Stress Analysis of Semiconductor Package

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반도체 패키지의 응력 해석

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Abstract

In the semiconductor IC(Integrated Circuit) package, the top surface of silicon chip is directly attached to the area of the leadframe with a double-sided adhesive layer, in which the base layer have the upper adhesive layer and the lower adhesive layer. The IC package structure has been known to encounter a thermo-mechanical failure mode such as delamination. This failure mode is due to the residual stress on the adhesive surface of silicon chip and leadframe in the curing-cooling process. The induced thermal stress in the curing process has an influence on the cooling residual stress on the silicon chip and leadframe. In this paper, for the minimization of the chip surface damage, the adhesive topologies on the silicon chip are studied through the finite element analysis(FEA).

Key Words : IC Package(직접회로 패키지), Adhesive Layer(접착 층), Adhesive Topology(접착 위상화), Finite Element Analysis(유한 요소 해석), Thermo-Mechanical Failure(열-기계적 파손)

Notation

E	Young's modulus
σ_b	Bending stress
M_b	Bending moment
ε_x	Strain of adhesive layer
ρ	Density of changed adhesive area
ρ_0	Density of fully adhesive area

1. Introduction

The semiconductor chip undergoes a considerable temperature change in the functional operation process or package manufacturing process. Then the residual thermal stresses result from the differences of thermal expansion coefficient of each component.

These thermal stresses induce the complicate stress states and results in the delaminations and failure modes

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between adhesive layers. In the recent trend of miniaturization and simplification of IC package, the thickness of package and each component is thinned. However, the stability of internal thermal stress within the package and environmental reliability are getting more important[1~4]. Fig. 1 shows the package configuration of semiconductor. The failure zones in the package are the layers between package and silicon chip, between silicon chip and leadframe and between leadframe and package. Many studies have been made on the delamination between leadframe and package, but the failure studies between silicon chip and leadframe are made in the recent[5]. For the reduction of delamination between silicon chip and leadframe, the reliable adhesive technique has been required. In this adhesive layer, the epoxy and polyimide are used. Using these adhesive materials, the thermal residual stresses are induced at the adhesive layers, which are due to the differences of thermal expansion coefficient of each component by cooling it from high temperature of adhesion to normal temperature. Thus the residual stress can be known to be a main factor resulting in layer failure. In order to improve the reliability of adhesion layer, we have to predict the magnitude and influence of residual stress and present the stable adhesion process and methodology. The stress analyses of delamination are made by Weitaman[7], Delale[8] and Lee[9].

This paper presents the topological adhesion methodology to reduce the thermal stresses between silicon chip and leadframe in the curing temperature(150℃), through the finite element analysis. In other words, the adhesion pattern between slilicon chip and leadframe is investigated through thermal analysis and thermal stress analysis. For the finite element model of semiconductor IC package, the 3 dimensional solid elements are used.

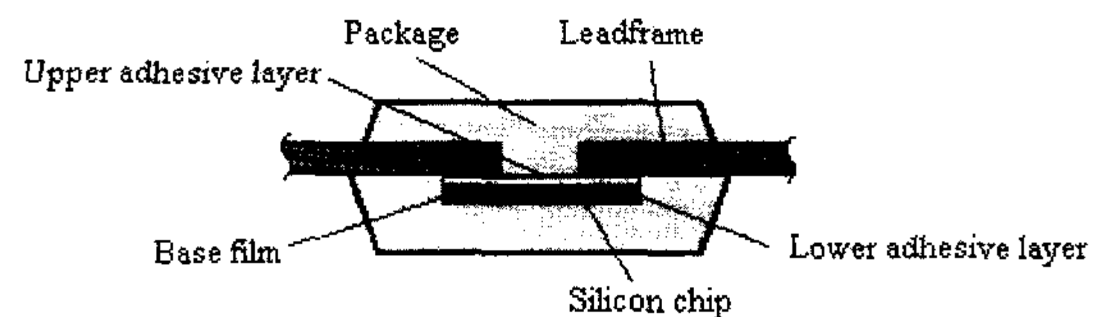
2. Theoritical Consideration and Adhesive Configuration

In the IC package, the top surface of chip is directly attached to the area of the leadframe with a double-sided adhesive layer, which the top and bottom of base layer have the upper adhesive layer and the lower adhesive layer. Under the thermal loading, the deformation of adhesive layer directly has an influence on the behavior of silicon chip. Thus, for the minimization of thermal stress on the adhesive surface of silicon chip, the adhesive configuration pattern in Fig. 1 (b) has to be investigated. Under the operational temperature, the behavior of silicon chip is symmetrical about the centerline. The bending behavior of silicon chip due to the stretching and contracting deformations of adhesive layer is shown in Fig. 2. The A-B component is an adhesive layer and the bottom is a silicon chip.

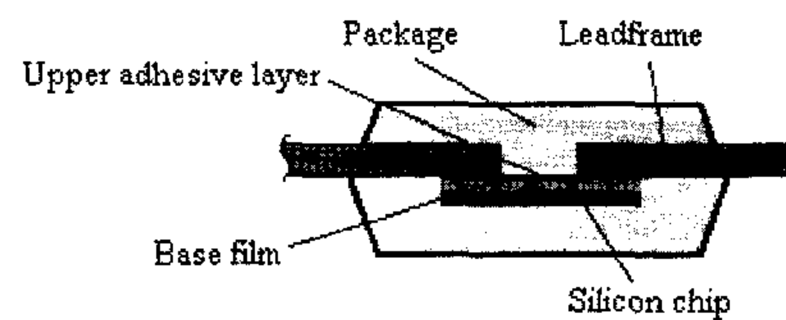
For the virtual bending moment M_b, the longitudinal strain ε_x on the surface of silicon chip and the bending moment are given by,

$$\varepsilon_x = \frac{1}{E}\left(-\frac{M_b y}{I}\right),\quad M_b = -\frac{EI}{y}\varepsilon_x \tag{1}$$

Setting the maximum strain $\varepsilon_x \approx \Delta L / L_0$ at the adhesive

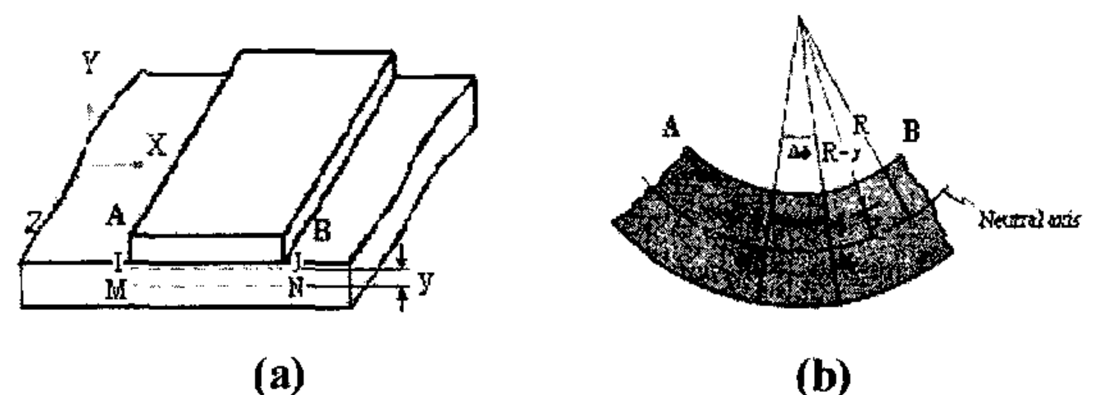


(a) Conventional adhesive layer configuration



(b) Investigated adhesive configuration

Fig. 1 Schematic diagrams of semiconductor IC packages



(a) (b)

Fig. 2 Deformation of silicon chip due to bending moment

face ($y=d/2$), the bending moment may be rewritten as,

$$M_b = -\frac{2EI}{d}\left(\frac{\Delta L}{L_0}\right) \tag{2}$$

on the neutral axis of silicon chip, where L_0 is the adhesive length, d is the thickness of silicon chip, ΔL is the maximum deformation of adhesive layer along the longitudinal direction. In other words, the more the deformation of adhesive layer has, the more the bending stress has.

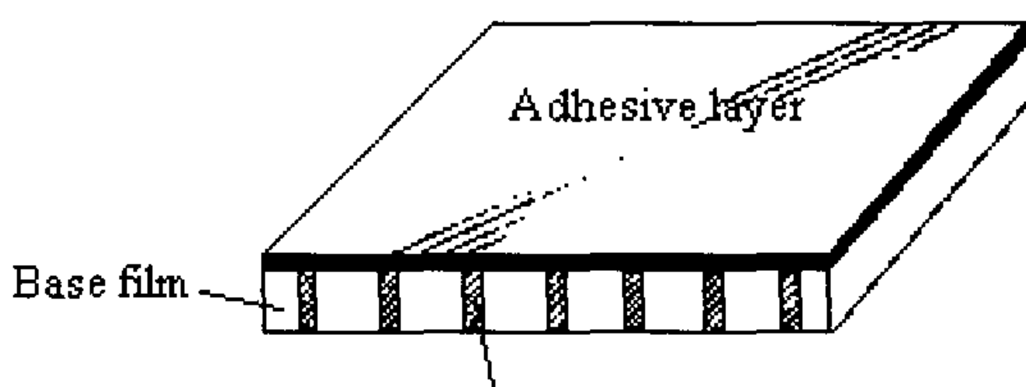
$$\sigma_b = \frac{M_b(d/2)}{I_{zz}} = E(\varepsilon_x)_{max} \tag{3}$$

From Eq. (3), $(\varepsilon_x)_{max}$ is the strain of adhesive layer. The reduction of the strain of adhesive layer can decrease the stress on the chip. Thus the strain on the chip can be changed through the density of adhesive area on it.

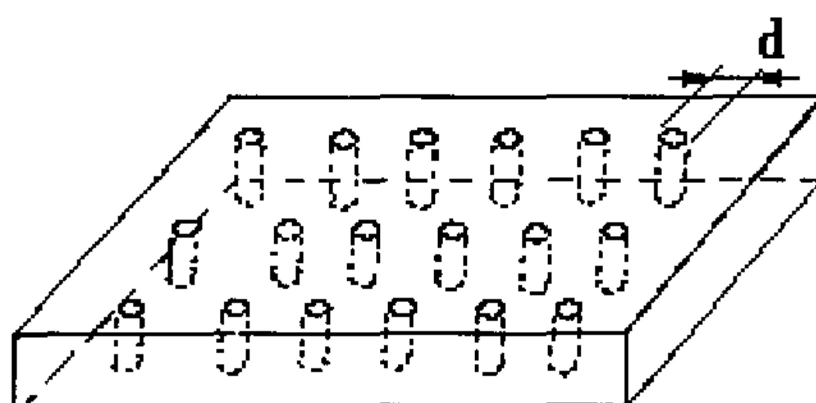
$$(\sigma_b)_{max} = E(\varepsilon_x)_{max}\left(\frac{\rho}{\rho_0}\right) \tag{4}$$

where ρ is the density of changed adhesive area in Fig. 1 (b) and ρ_0 is the density of fully adhesive area in Fig. 1 (a). The topology of ρ is shown in Fig. 3. In the paper, the thermal stresses in the package have been investigated in terms of the density of adhesive area.

The diameter (d) of pass-through area of each adhesive hole changes from 0.1mm to 0.3mm. And the thickness of base film is 32μm that is the thickness of lower adhesive layer plus original base film. The base film has eighteen holes that pass through the adhesive material from the upper adhesive layer.



(a) adhesive configuration



(b) 3-D base film

Fig. 3 3-dimensional configuration of Investigated adhesive layer

3. Simulation

3.1 Finite element model of package

The 3-dimensional linear finite element modeling(Fig. 4 and 5) was used to estimate the thermal stress distribution on the silicon chip. The MSC/NASTRAN was adopted to calculate various stresses[4-5]. A quarter model composed of 23626 nodes and 41524 solid elements is used for the

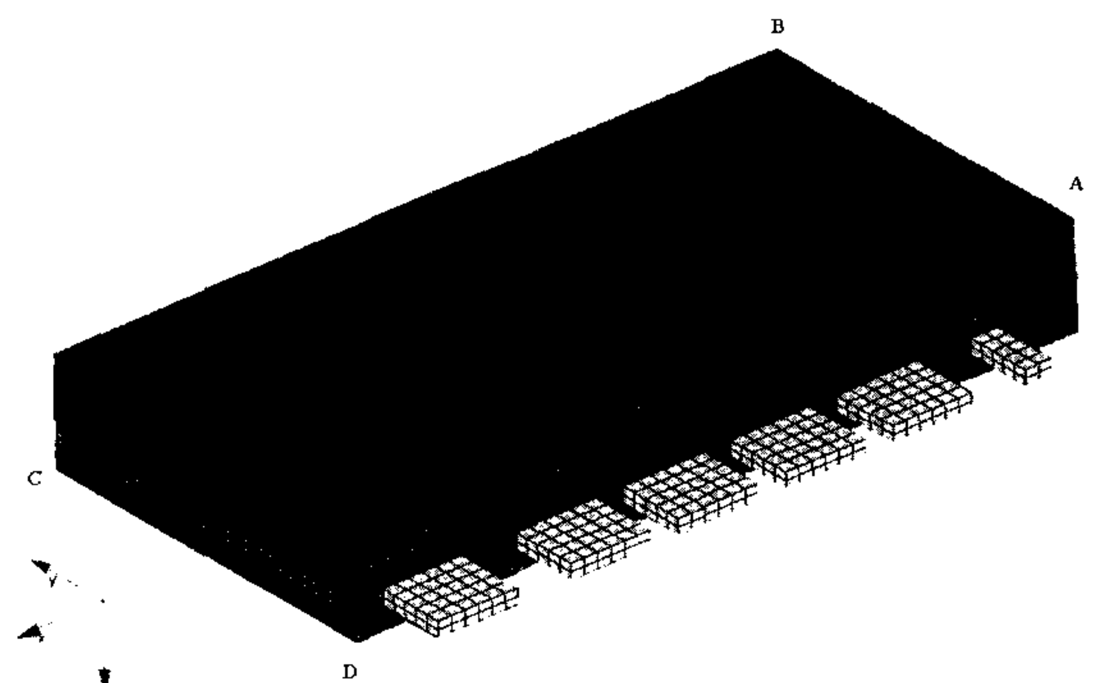


Fig. 4 Schematic diagrams of 3-dimensional semiconductor IC package

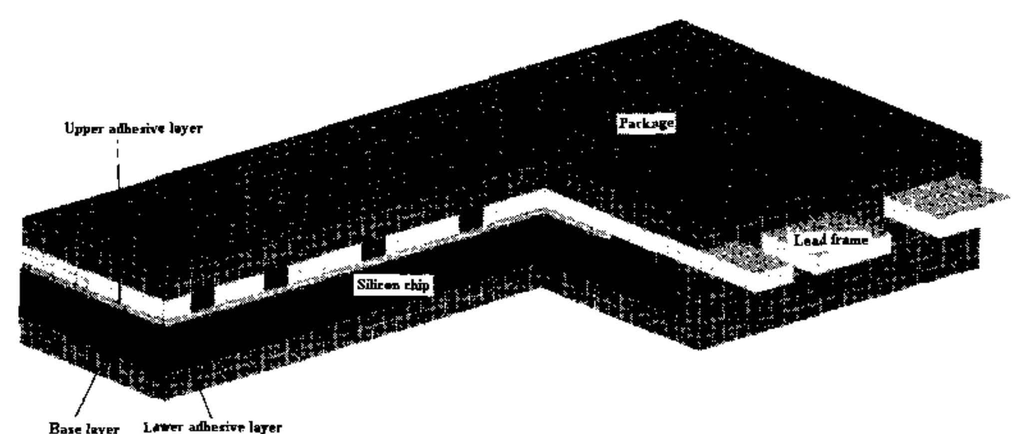


Fig. 5 Components of semiconductor IC package

finite element analysis in this study. First is to analyze the temperature boundary in the packages. In the thermal analysis, the convection passing through of the package and leadframe and the conduction of components within the package was taken into account[4]. Second is to analyze the thermal stress restrained to the above temperature in the package[4]. The mechanical boundary conditions of behavior are imposed on the symmetric face (B-C) and longitudinal face(C-D). The stresses are estimated from the thermal displacement imposed on the package by curing it at 150℃. But the package production of hyper-temperature over 150℃(210℃~260℃) shows various manufacturing defects.

The thermal and mechanical properties[5] of the package components are shown in Table 1 and Table 2. In Table 2, σ_y is a yielding strength and σ_u is an ultimate strength.

Table 1 Material properties

	Silicon chip (silicon)	Package (epoxy)	Lead-Frame (alloy 42)	Adhesive layer (polyimide)	Base film (polyimide)
C.T.E (ppm/℃)	2.6	11	4.5	50	25
Conductivity coefficient (W/m℃)	110	0.735	10.5	0.35	0.35
Elastic modulus (GPa)	188	23	145	2	2
Poisson's ratio	0.14	0.23	0.27	0.41	0.41
Mass Density (ton/m^3)	3.17	2.07	8.05	1.37	1.37
Thickness (mm)	300	1000	120	17	25

Table 2 Component strengths

	σ_y (MPa)	σ_u (MPa)
Silicon	-	68
Polyimide film	49	162
Alloy 42(INVAR)	276	448

3.2 Thermal Stress Distribution on the Silicon Chip

From Eq. (3), thickening the passivation can decrease the local stress concentration, thermal-mechanically. But in this study, the adhesive topology of layer was investigated on the base of constant thickness of adhesive layer and passivation. Fig. 6 shows the thermal stress contours on the silicon chip under the curing temperature. Fig. 7 ~ Fig. 9 show the trend of maximum Von-Mises stress, maximum shear stress and maximum normal stress to the densities of adhesive areas. The 0% is the full adhesion on the silicon chip without topological densities. Fig. 7 ~ Fig. 9 show very steep stress decrease from 0% to 3%. And then from over 3%, the stress curves show increase trend. The adhesion areas of 3%, 6%, 12%, 18% and 26% are respectively 0.22mm^2, 0.42mm^2, 0.84mm^2, 1.26mm^2 and 1.89mm^2. Each hole is uniformly distributed on the silicon chip. From Fig. 5 ~ Fig. 9, the thermal stress seems to be reduced with the decrease of adhesive area on the silicon chip. It can be known that the densities of adhesive area have influences on the thermal stress distributions on the silicon chip and the thermal expansion on the chip is greater with the increase of adhesive area.

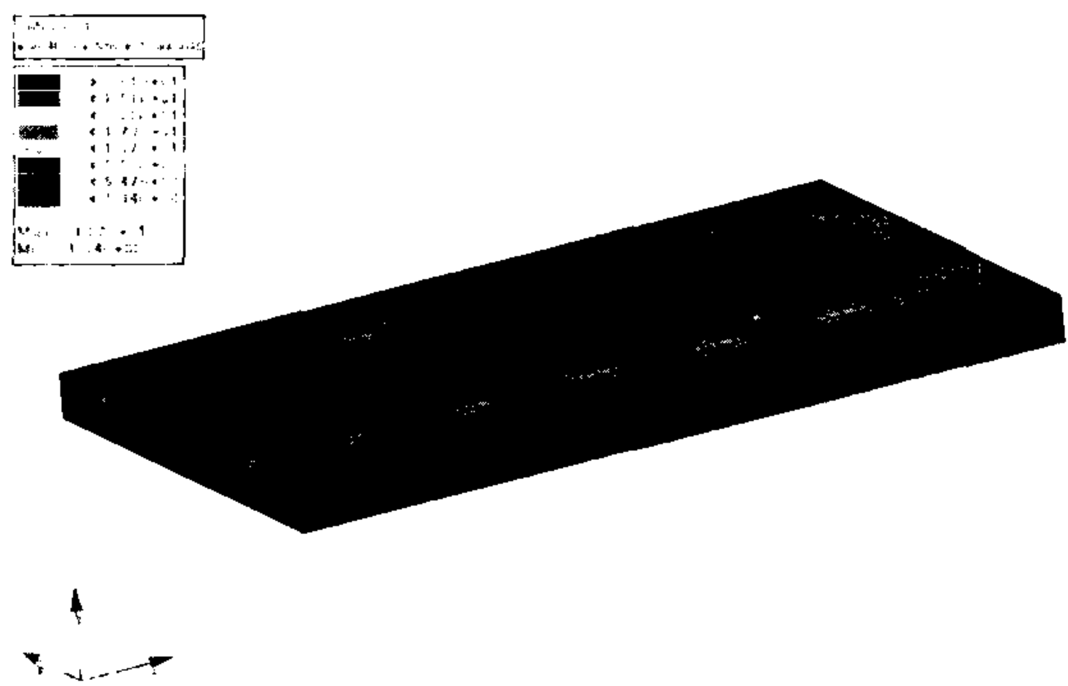
Thus, the topological adhesive area is very important in securing the thermal structural rigidity and reliability of IC package under the thermal effects. In the design of the semiconductor IC package, the adhesive topology of layer must be taken into account.

4. Conclusion

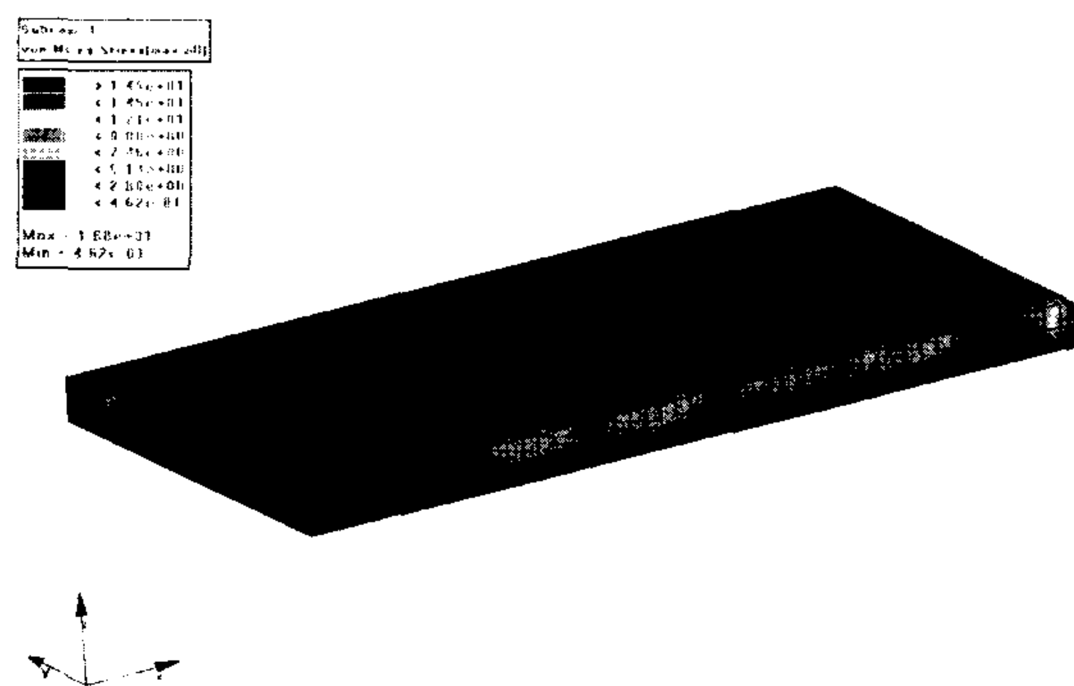
For the investigation of failure mode, the thermal analysis and thermal stress analysis of semiconductor IC package are made under the adhesive curing temperature. The thermal stress in the package is concentrated on the adhesive layers due to the different thermal expansion of materials and results in the bending behavior of package. This stress has an influence on the delamination of layer due to the cooling residual stress in the package.

The passivation layer has to be thickened in order to

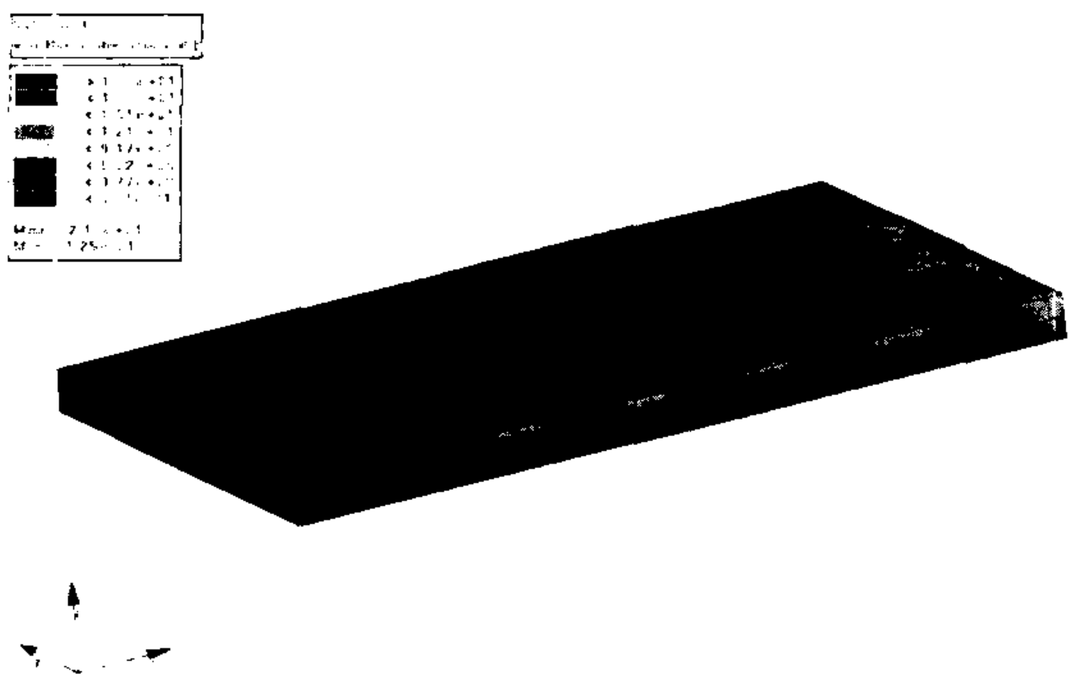
prevent reliability degradation associated with the failure during thermal cycling. This is responsible for avoiding the local stress concentration. In this study, for the reduction of residual stress, the adhesive topology in the layer with passivation thickness can be known to be an important factor on the thermal stress of the adhesion layer. The 3% ~ 6% adhesive area on the silicon chip on the basis of (b), (c) in Fig. 6 can reduce the thermal stress up to 33%. This reduction of residual stress helps to improve the reliability of adhesive layers and the functional operation of IC package.



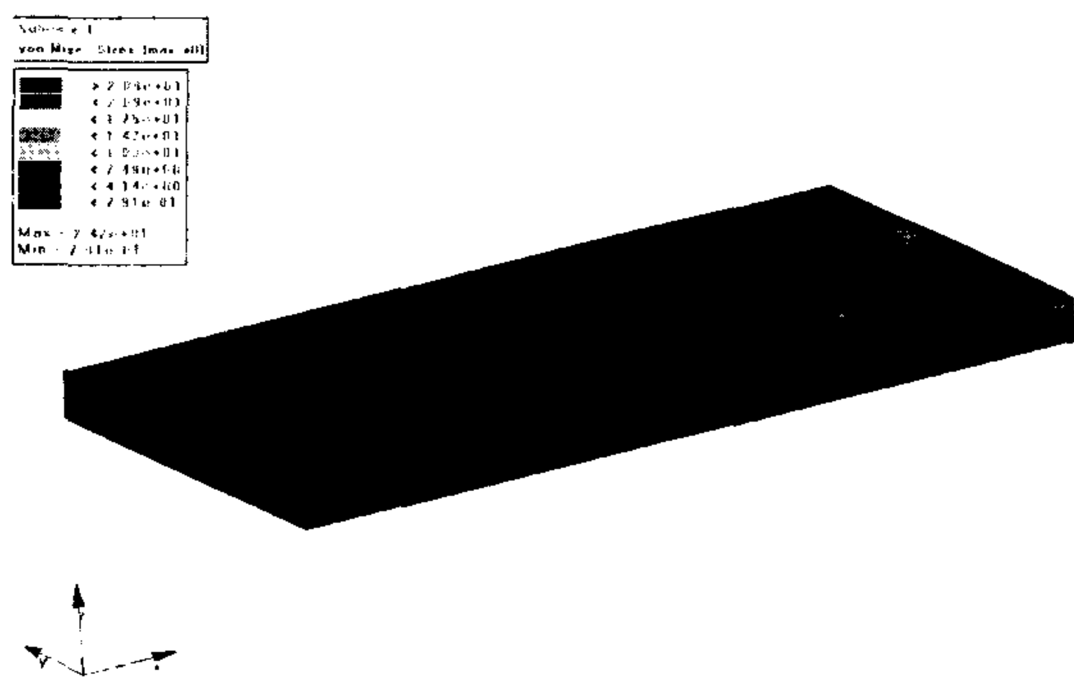
(a) Stress contours on the full adhesive layer(0%)



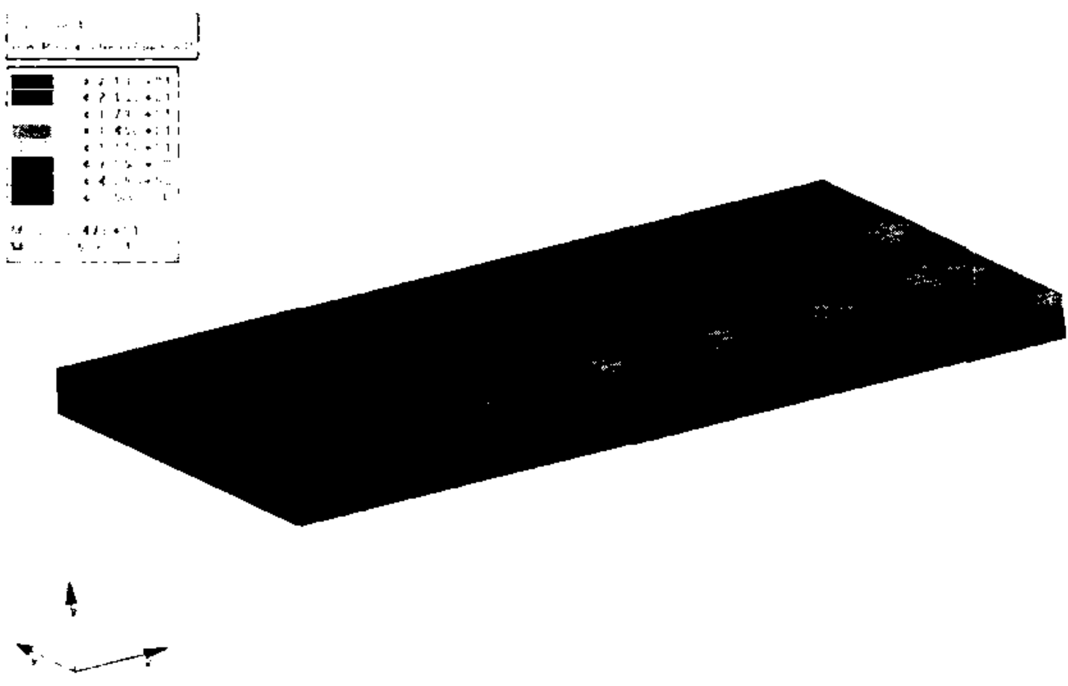
(b) Stress contours on the 3% adhesive layers



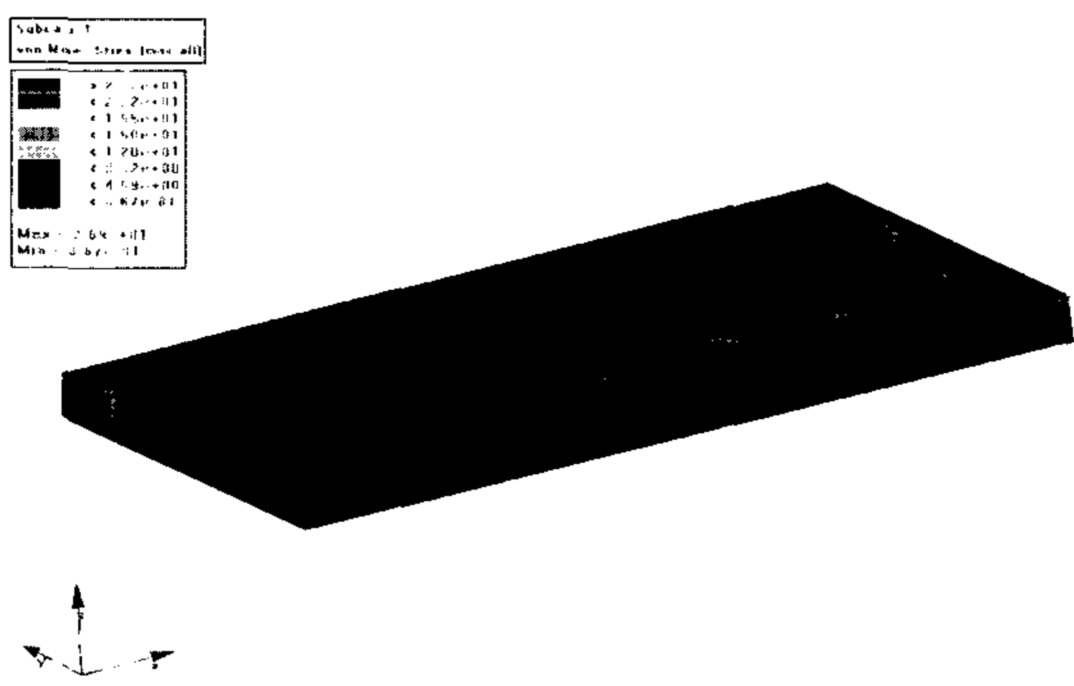
(c) Stress contours on the 6% adhesive layers



(d) Stress contours on the 12% adhesive layers



(e) Stress contour on the 18% adhesive layers



(f) Stress contour on the 26% adhesive layers

Fig. 6 Von-Mises stress contour of silicon chip

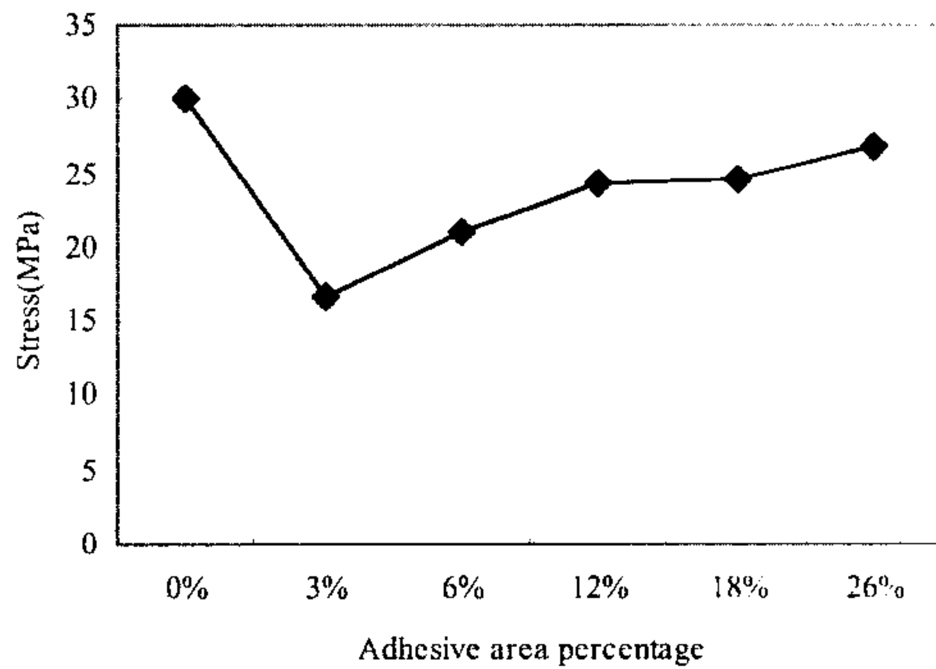


Fig. 7 Max. Von-Mises stress on the silicon chip

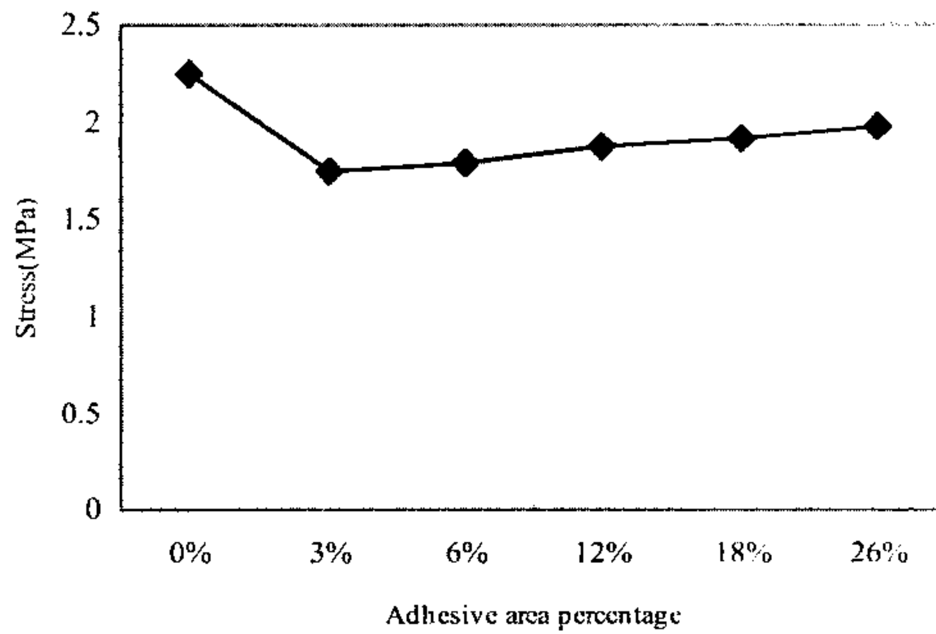


Fig. 8 Max. Shear stress on the silicon chip

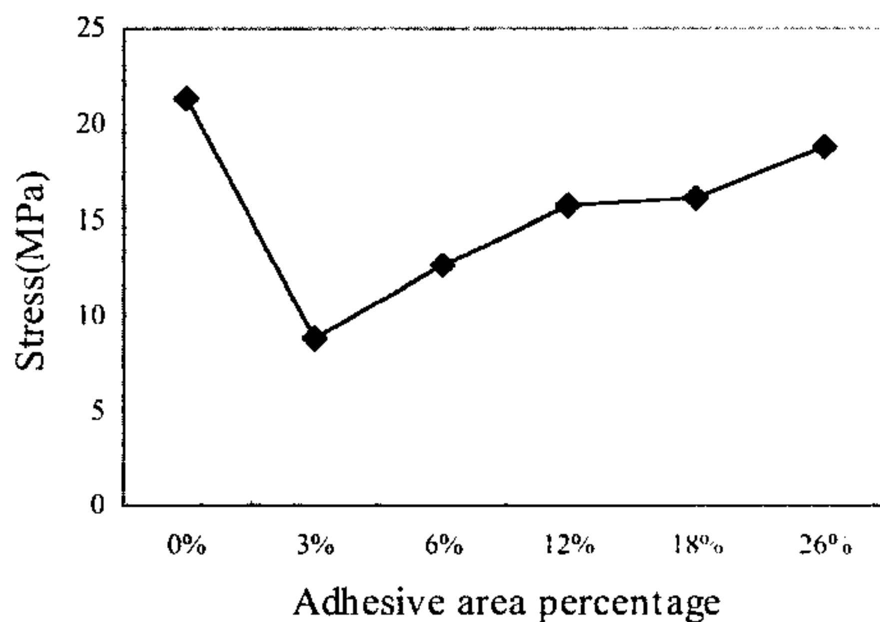


Fig. 9 Max. Normal stress on the silicon chip

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