

# Design of Connectivity Test Circuit for a Direct Printing Image Drum

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**Abstract**—This paper proposes an advanced test circuit for detecting the connectivity between a drum ring of laser printer and PCB. The detection circuit of charge sharing is proposed, which minimizes the influences of internal parasitic capacitances. The test circuit is composed of precharge circuit, analog comparator, level shifter. Its functional operation is verified using 0.6 $\mu$ m 3.3V/40V CMOS process parameter by HSPICE. Access time is 100ns. Layout of the drum contact test circuit is 465 $\mu$ m x 117 $\mu$ m.

**Index Terms**—Direct Image Printing, Image Drum, Test Circuit, Charge-sharing scheme, Laser Printer

## I. INTRODUCTION

The growth estimates of the market size for short-run digital colour printing are very promising. This explains the efforts of many major players in this business in trying to develop a successful combination of a product concept and a colour technology, which can fill the gap between the traditional offset presses and the low-volume laser and inkjet printers[1].

The first innovation and the heart of the image development process is formed by the so-called Direct Imaging (DI) unit which is schematically shown in figure 1. The printing surface of a DI-drum is 317 mm wide and has a resolution of 600 dpi. This requires about 5000 drum-tracks. The term ‘Direct Imaging’ refers to the imaging principle: electronic circuits inside the drum generate a toner image ‘directly’ in a one-step process (see figure 1). This distinguishes DI from most commonly used electrophotographic printing processes that all use a latent electrostatic image on a photosensitive image carrier whereby a toner image is formed in several successive steps (such as charging, exposure, developing).

In Direct Imaging, 5000 conducting tracks on the surface of each DI drum are controlled by means of a large number of ASIC’s that convert a digital image into either 0 or 40V voltage at appropriate times. When a

track is powered with 40V, toner locally adheres to the surface[1][2].

This paper proposes an advanced test circuit for detecting the connectivity between a drum ring and PCB. The detection circuit of charge sharing is proposed, which minimizes the influences of internal parasitic capacitances. The test circuit is composed of analog comparator, 3.3V to 40V level-up shifter and 40V to 3.3V level-down shifter. Its functional operation was verified and implemented using 0.6 $\mu$ m 3.3V/40V CMOS process parameter by HSPICE. Layout was performed using the 0.6 $\mu$ m 3.3V/40V standard CMOS process.

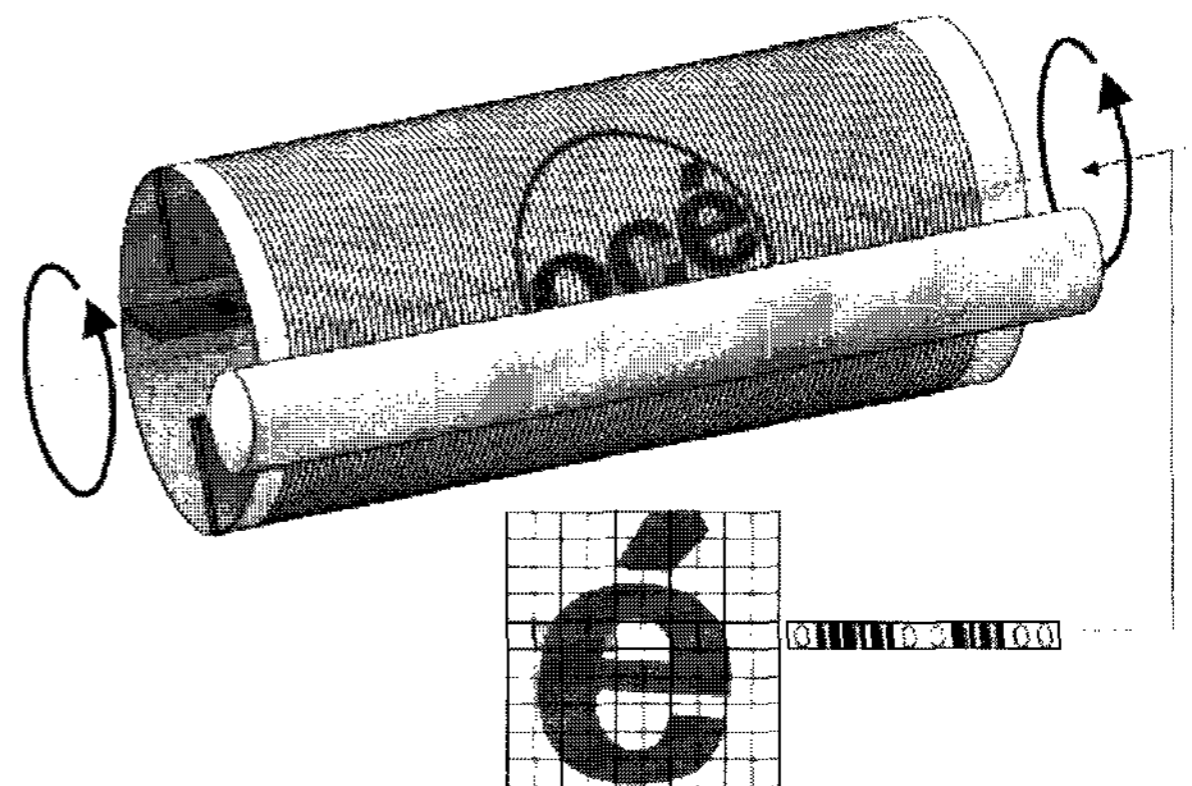


Fig. 1. Direct Imaging printer

## II. Conventional drum contact test circuit

Figure 2 shows a driver IC for controlling the DI drum. The driver IC supplies the parallel data from PC's serial data and tests the electrical connectivity of 5000 drum conduct rings. The driver IC's that power the drum-tracks contain special circuits to enhance the testability of the drum parts, the drum production. These tests include parametric tests among which is a drum-track capacitance measurement.

Figure 3 shows conventional test circuit for controlling a connectivity of DI drum[4]. In figure 3 the measurement principle is explained schematically. During ‘normal’ driving operation both switches p and n are used to switch the track to either 0 or 40V.

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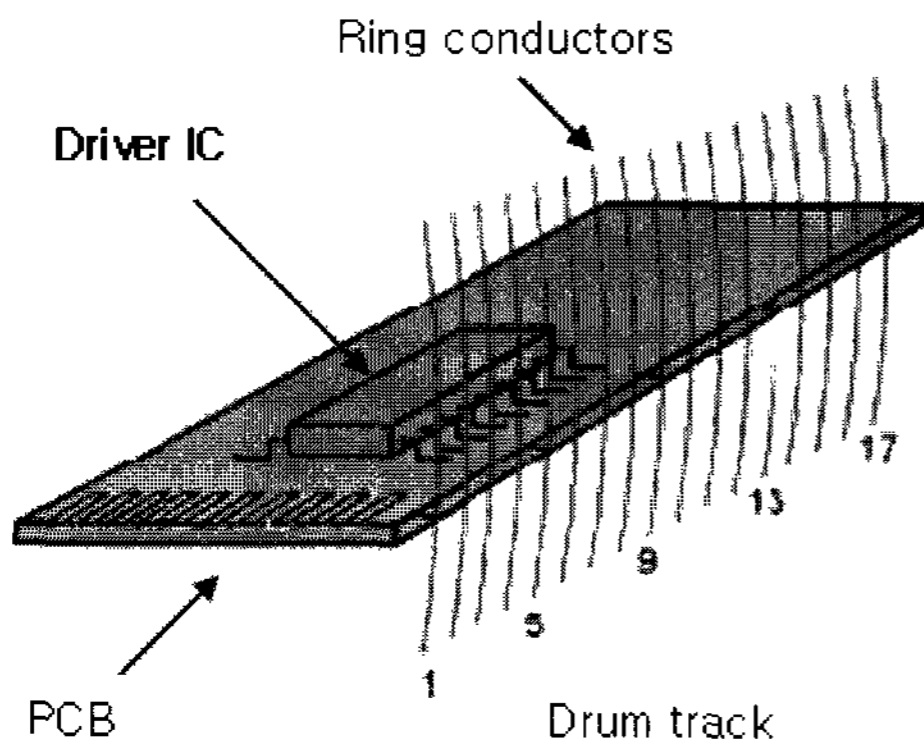


Fig. 2. Driver IC of the Direct Imaging process

One single test line that can be connected via a test switch  $t_s$  to every ASIC-output makes it possible to connect each track to an off-chip electronic integrator circuit. During a capacitance measurement a specific track is charged to 40V while the neighbouring tracks are grounded. Subsequently switch  $p$  is opened and the track is discharged through the integrator by closing switch  $t_s$ . This makes it possible to measure the amount of accumulated charge ( $Q_{\text{track}}$ ) and thus the capacitance ( $C_{\text{track}} = Q_{\text{track}}/40\text{V}$ ) of the drum-track. In case of a 'clean' drum this capacitance mainly consists of track-to-track capacitances (approximately 30 pF to neighbouring tracks). There is no theoretical formula to calculate the exact capacitance due to fringing effects. We have used a Finite Element Method to determine the value numerically. Due to the conductivity and dielectric properties of the toner deposited toner will increase the total capacitance. This increase in capacitance can be easily determined by measuring the capacitance of all tracks without toner first and using this as a baseline which is afterwards subtracted from measurement signals.

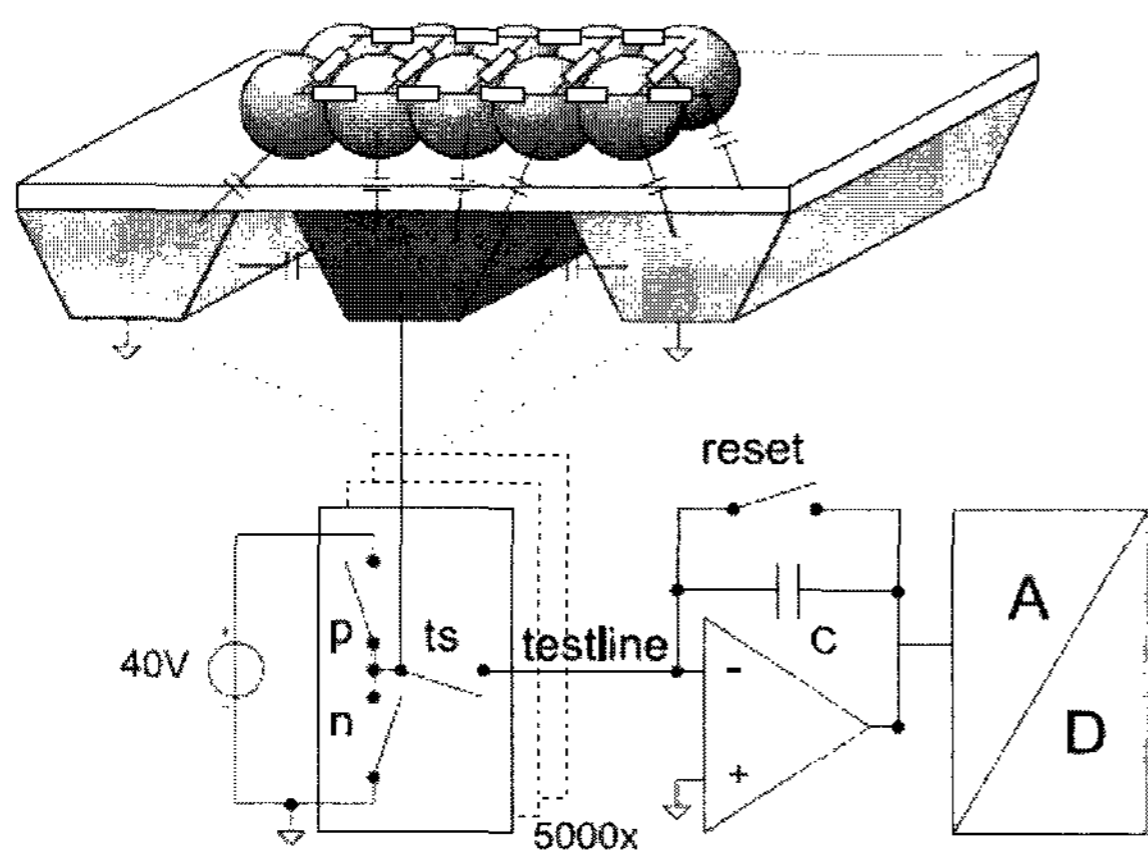


Fig. 3. Conventional test circuit by capacitance measurement.

But actually, the conventional test circuit has some problem. This circuit needs a high performance operational amplifier and analog-to-digital converter. Also, this requires about 5000 drum-track test circuits. Therefore, the conventional test circuit causes a non-efficiency in layout and power consumption of driver IC.

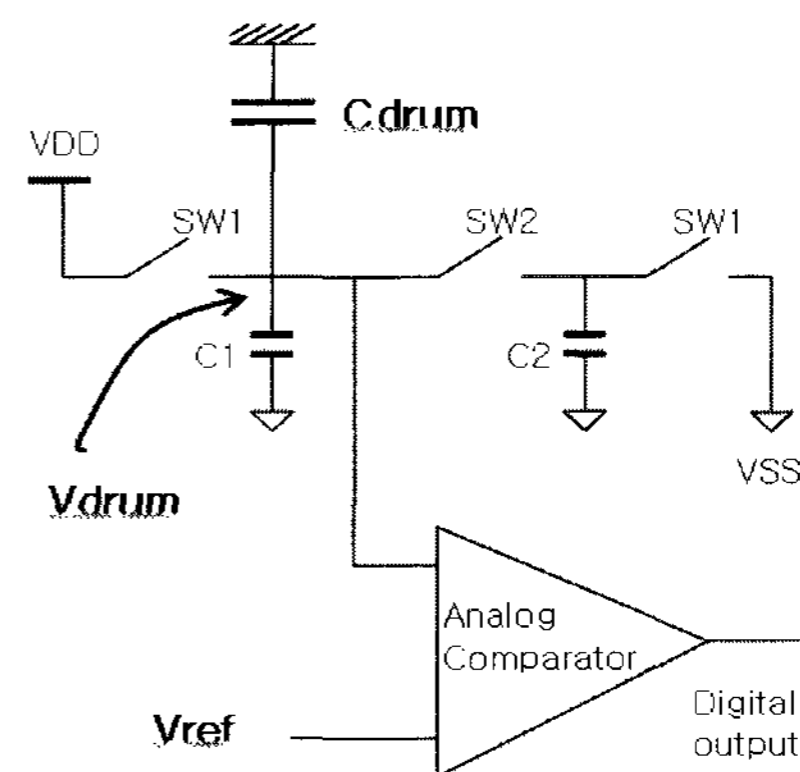
### III. Proposed drum contact test circuit

This paper designed an advanced drum contact test circuit based on a charge-sharing scheme shown in figure 4(a). 'C<sub>drum</sub>' is drum ring conductor capacitance value and the C<sub>1</sub>, C<sub>2</sub> are internal capacitance value of driver IC. Generally, C<sub>drum</sub> is more than C<sub>1</sub> or C<sub>2</sub>. C<sub>2</sub> is about 2 times value of C<sub>1</sub> in this paper.

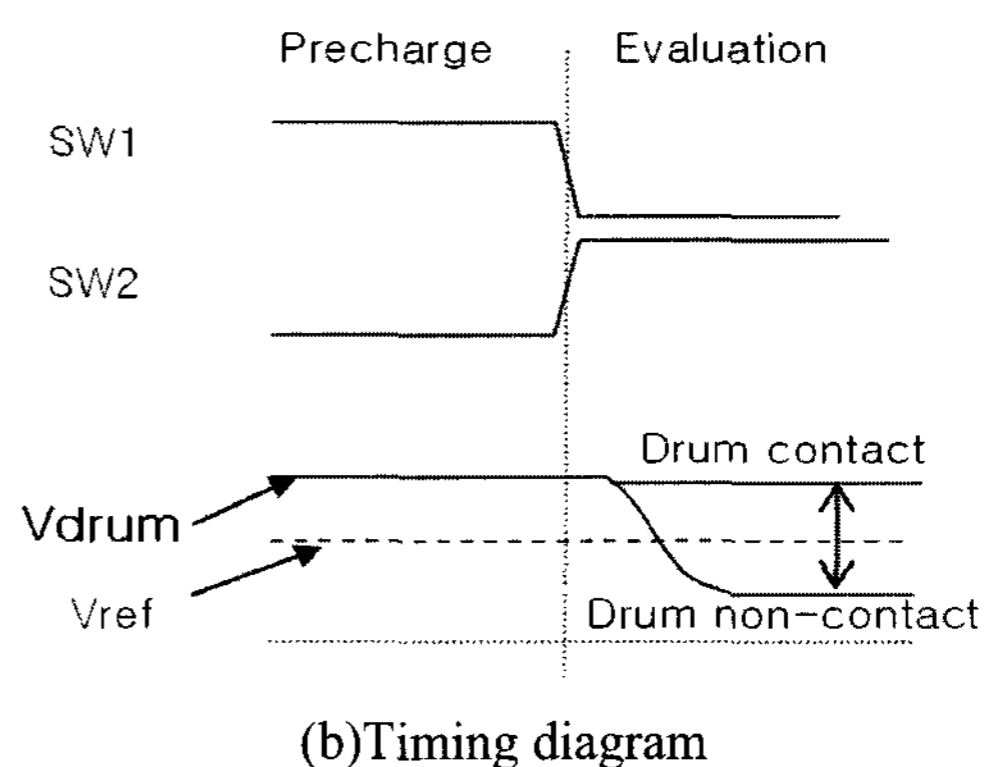
The proposed sensor detection circuit has two operating phases shown in figure 4(b)[3]. In the precharge mode, all nodes are precharged. In the evaluation mode, SW1 is off and SW2 is turn-on. In case of contact between PCB and drum ring conductor, because C<sub>drum</sub> has maximum value, C<sub>drum</sub> tries to keep the voltage level, thus 'V<sub>drum</sub>' is slightly decreased. Therefore V<sub>drum</sub> is about V<sub>dd</sub>(40V). In case of non-contact, C<sub>drum</sub> has minimum value and V<sub>drum</sub> depends on C<sub>1</sub> and C<sub>2</sub>. V<sub>drum</sub> is following,

$$V_{\text{drum}} = \frac{C_1}{C_1 + C_2} * V_{\text{dd}} \quad (1)$$

If C<sub>2</sub> is 2 \* C<sub>1</sub>, V<sub>drum</sub> is decreased to 1/3V<sub>dd</sub>. Ideally, the voltage difference between drum ring contact and non-contact is about 2/3V<sub>dd</sub>. Thereby, the comparator easily discriminates a contact and non-contact.



(a) Charge-sharing scheme (C<sub>drum</sub> >> C<sub>1</sub>, C<sub>2</sub>)



(b) Timing diagram

Fig. 4. Principle of charge-sharing circuit

In this paper, we propose the pi-model of drum structure for an accurate electrical analysis. Figure 5 and 6 show drum ring conductor structure and RC model with 3

rings. PCB includes the driver IC and is connected to a drum ring conductor.

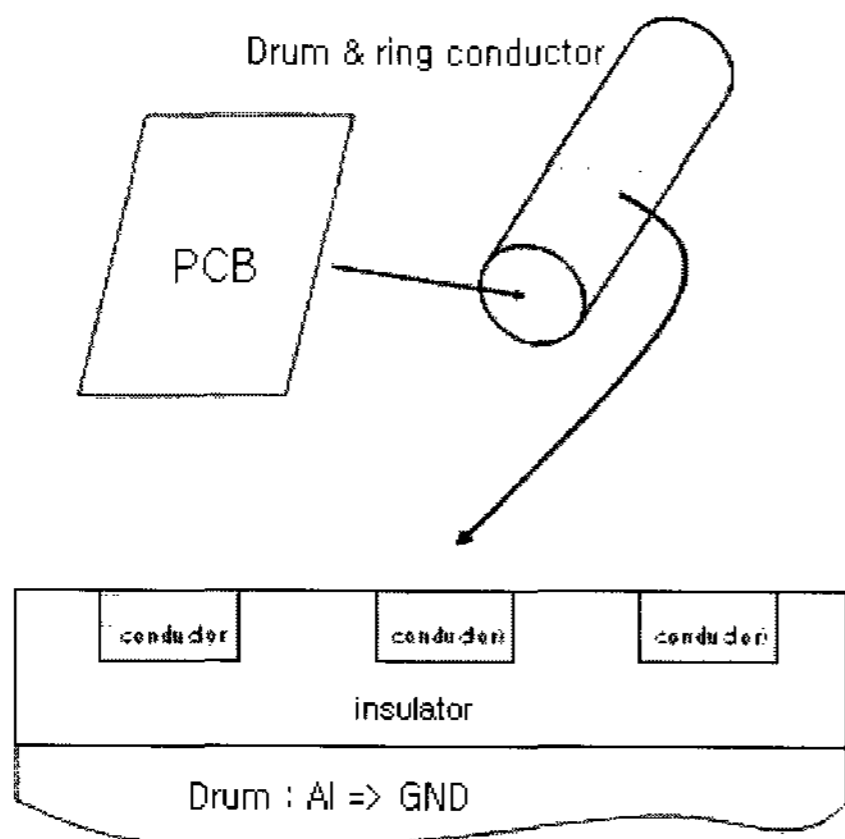


Fig. 5. Drum ring conductor structure

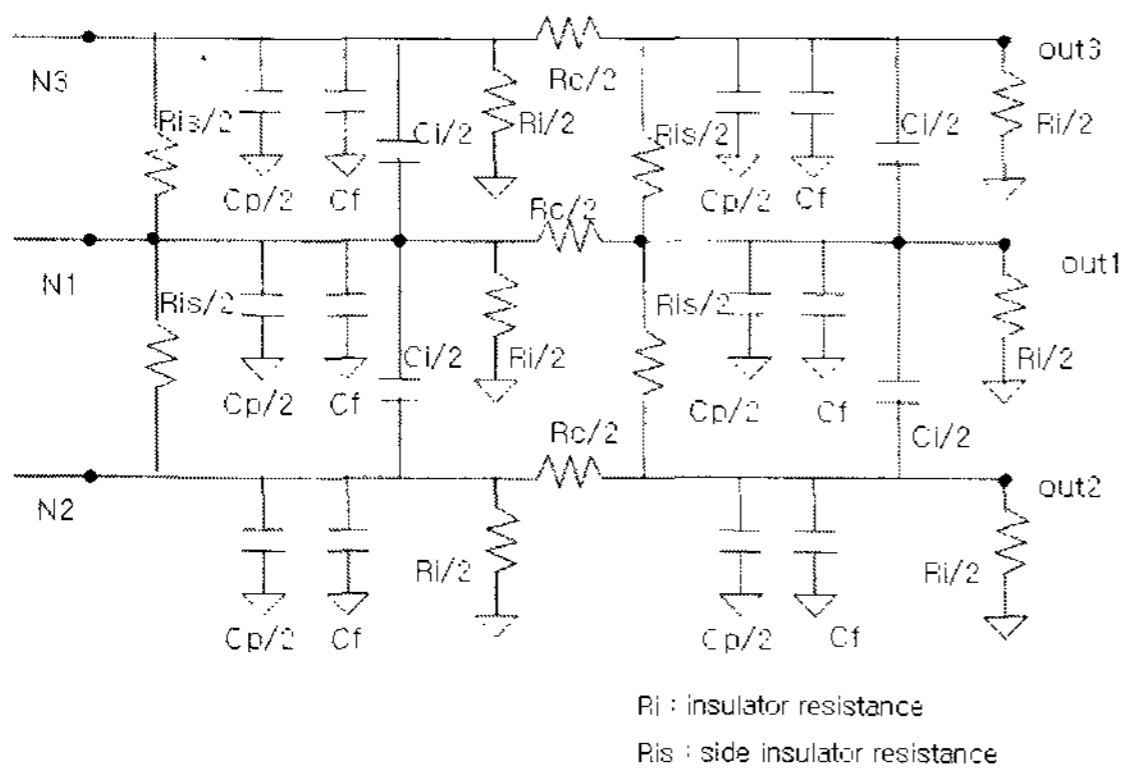


Fig. 6. Drum ring conductor RC model

Figure 7 shows the drum contact test circuit. The 'prech' block includes a charge-sharing sensing circuit with precharge and evaluation operation. The 'levup' and 'levdn' block are used for 3.3V to 40V interface of microprocessor. Figure 8 and 9 show 'levup' and 'levdn' circuit. 'PCHB' signal controls precharge and evaluation operation in a charge-sharing sensing circuit. 'SENSE' signal controls an analog comparator enable operation. One circuit tests the connectivity of 16 rings by 16x1 mux 'DEC16'. Figure 10 shows an analog comparator 'acomp'.

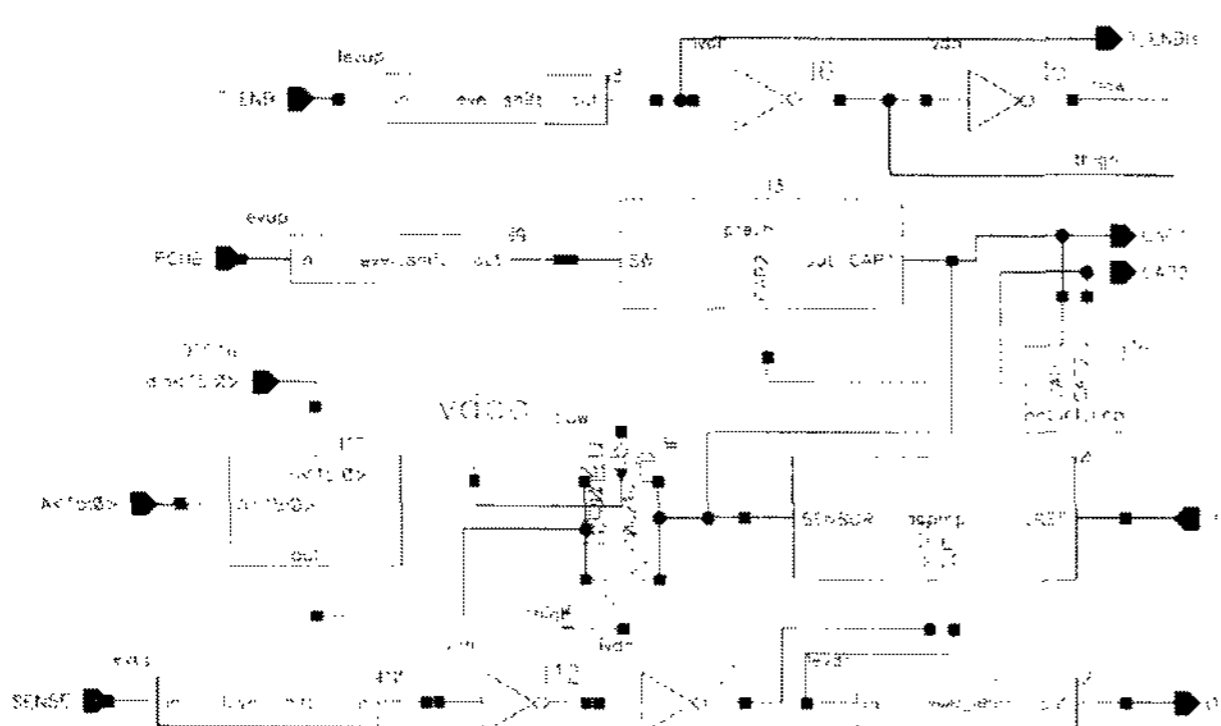


Fig. 7. Implementation of ring contact test circuit with charge-sharing scheme

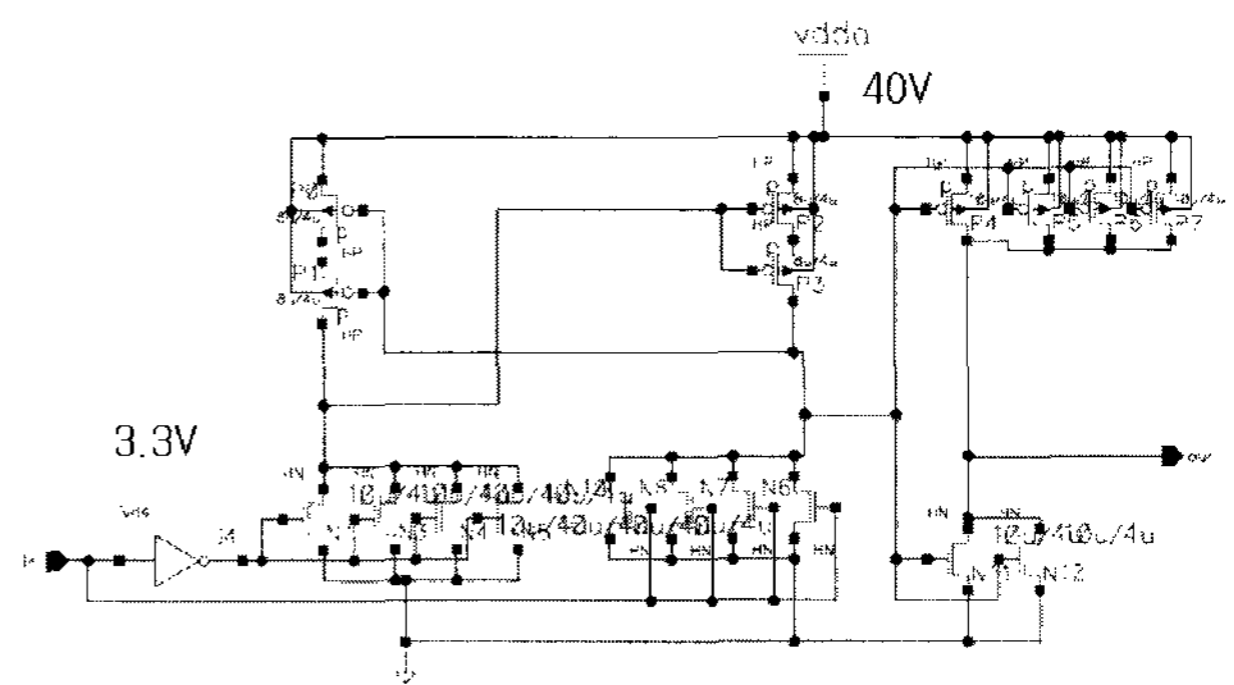


Fig. 8. level-up shift circuit

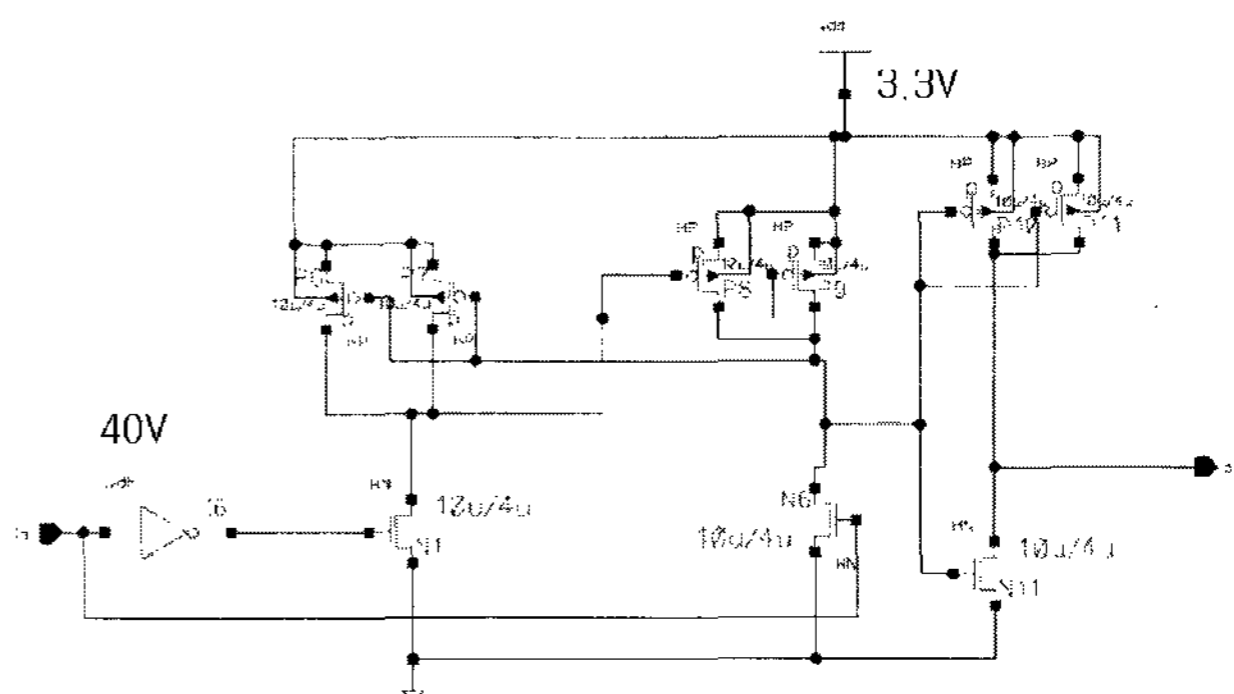


Fig. 9. level-down shift circuit

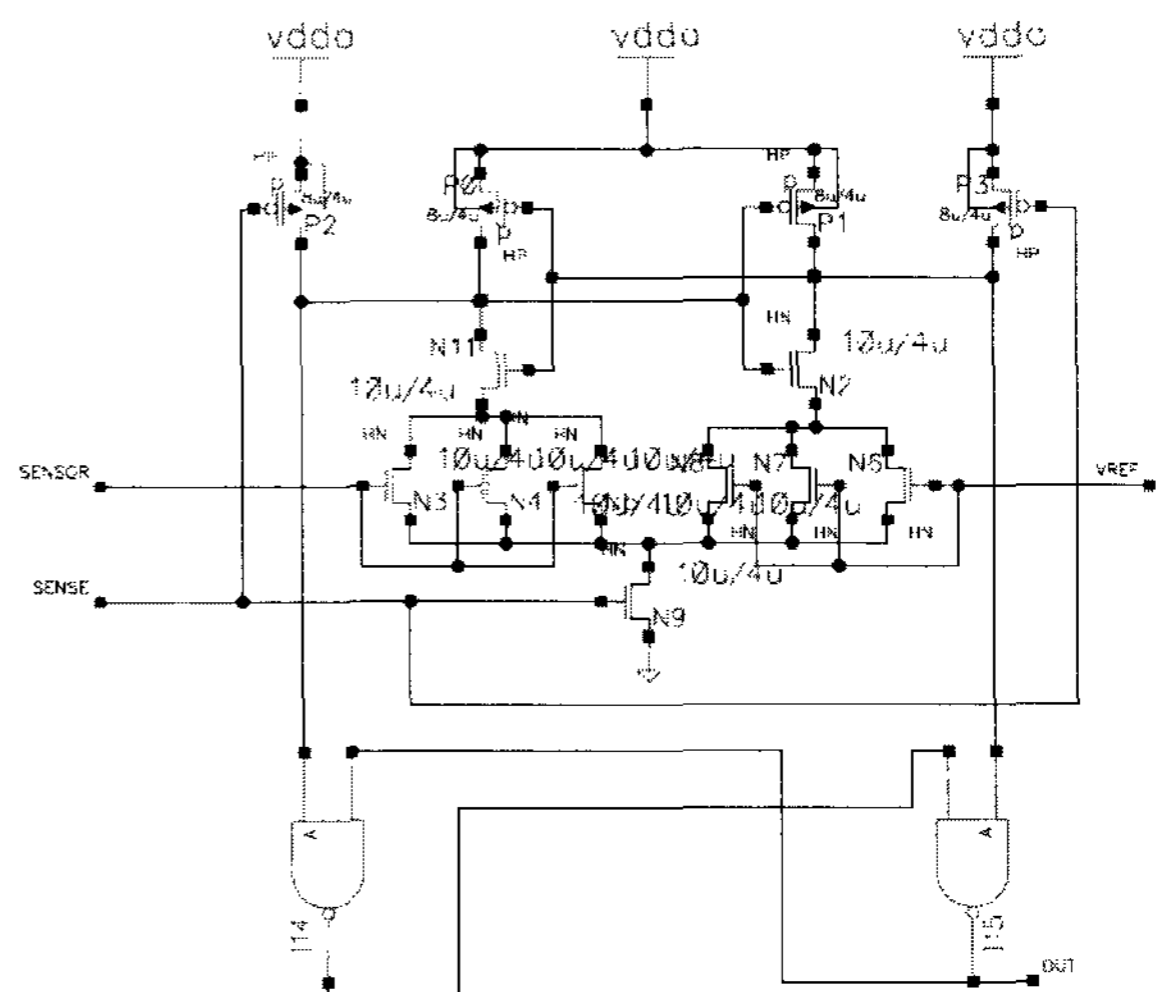


Fig. 10. Comparator(acomp)

To confirm the effect of proposed circuit, we extracted each parasitic capacitance from the optimized layout. An improvement can be seen by HSPICE simulation of the cell with condition of 0.6μm worst parameter and 3.0V power supply after layout extraction(see Figure12). Figure 11 shows simulation result. The voltage difference between the contacted point and the non-contacted point is 4.8V. Thereby, the comparator easily discriminates the drum contact and drum non-contact. As a result, we can get high-quality test result without the influence of the reference voltage(Vref) variation according to conventional circuit. The enhancement of layout area and power consumption is expected from the advanced circuit. Figure 12 shows layout of drum contact test circuit. Area is 465μm x 117μm.



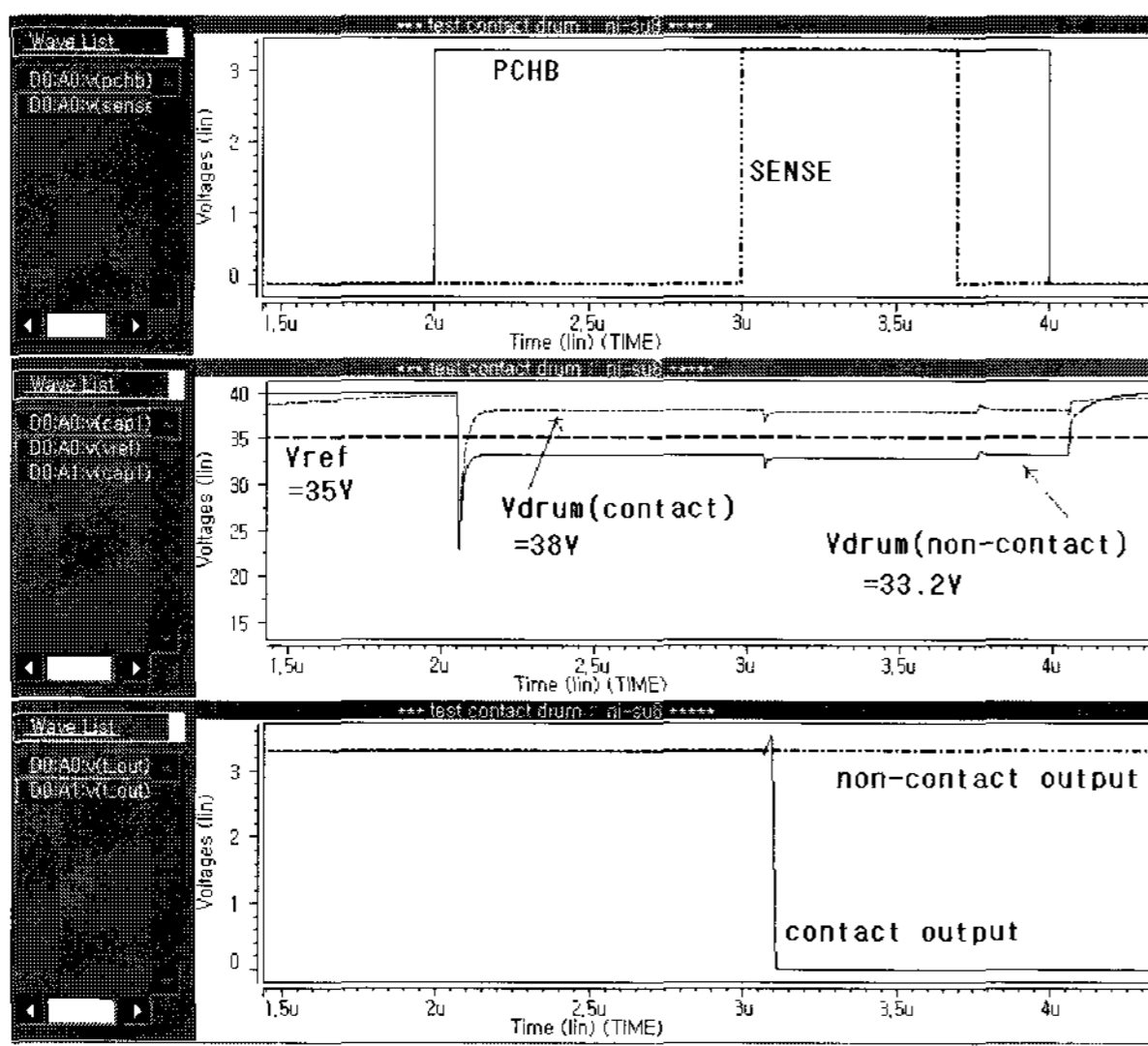


Fig. 11. Simulation result  
(0.6 $\mu$ m 3.3V/40V worst process)

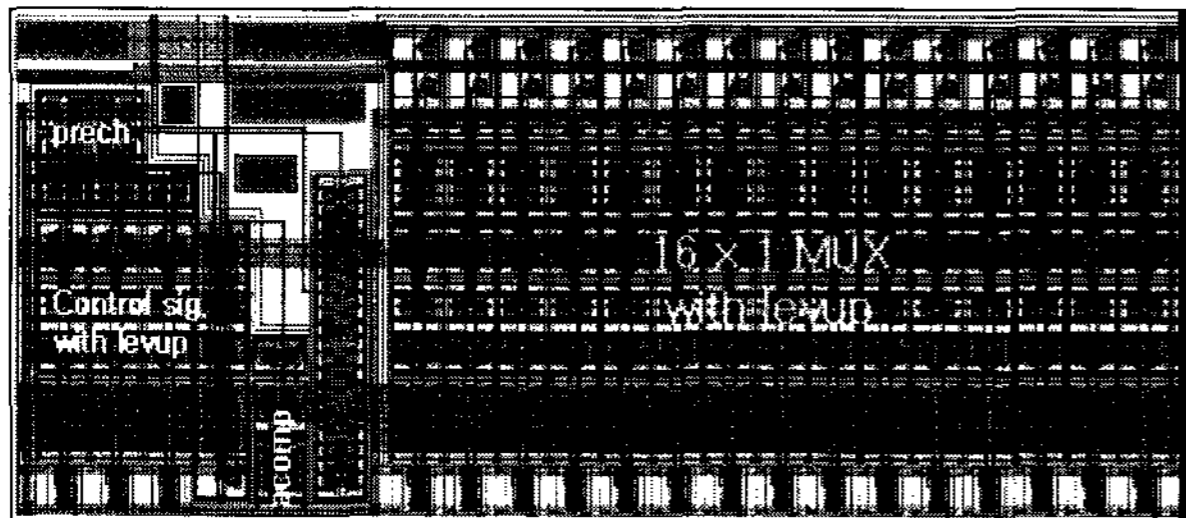


Fig. 12. ring contact test circuit layout (465 $\mu$ m x 117 $\mu$ m)

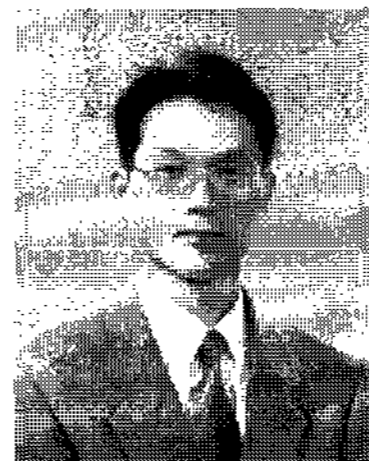
### III. CONCLUSIONS

The conventional connectivity test circuit has some problem in direct image printing method. It needs a high performance operational amplifier and analog-to-digital converter. Also, this requires about 5000 drum-track test circuits. Therefore, the conventional test circuit causes a non-efficiency in layout and power consumption of driver IC.

This paper proposes an advanced test circuit for detecting the connectivity between a drum ring and PCB. The detection circuit of charge sharing is proposed, which minimizes the influences of internal parasitic capacitances. The test circuit is composed of analog comparator, 3.3V to 40V level-up shifter and 40V to 3.3V level-down shifter. Its functional operation was verified and implemented using 0.6 $\mu$ m 3.3V/40V CMOS process parameter by HSPICE. Layout was performed using 0.6 $\mu$ m 3.3V/40V standard CMOS process. The voltage difference between the contacted point and the non-contacted point is 4.8V. Thereby, the comparator easily discriminates the drum contact and drum non-contact. As a result, we can get high-quality test result without the influence of the reference voltage( $V_{ref}$ ) variation according to conventional circuit. The enhancement of layout area and power consumption is expected from the advanced circuit. Figure 12 shows layout of drum contact test circuit. Area is 465 $\mu$ m x 117 $\mu$ m.

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(SM'02) was born in Seoul, Korea, on April 25, 1968. He received the BS, MS and PhD degrees in electronics engineering from Yonsei University, Seoul, Korea, in 1990, 1992 and 2006. He was Senior Engineer of the ASIC Division at the SAMSUNG Electronics Co., from 1992 to 1997. From 1998 to 2006, he joined the faculty of Yongin-Songdam College, Yongin, Korea, where he was assistant professor in the Information Science and Telecommunication Department. In 2006, he joined the faculty of Hanshin University, Osan, Korea, where he is currently associate professor in the Information and Communication Department. His research interests include CMOS sensors, multimedia communication SOC design and high-speed interface mixed circuit design.