Pipelined Implementation of JPEG Baseline Encoder IP

Kyung-Hyun Kim, Seung-Il Sonh, *Member, KIMICS*

Abstract—This paper presents the proposal and hardware design of JPEG baseline encoder. The JPEG encoder system consists of line buffer, 2-D DCT, quantization, entropy encoding, and packer. A fully pipelined scheme for JPEG encoder is adopted to speed-up an image compression. The proposed architecture was described in VHDL and synthesized in Xilinx ISE 7.1i and simulated by modelsim 6.1i. The results showed that the performance of the designed JPEG baseline encoder is higher than that demanded by real-time applications for 1024x768 image size. The designed JPEG encoder IP can be easily integrated into various application systems, such as scanner, PC camera, color FAX, and network camera, etc.

Index Terms—JPEG, Baseline, Encoder, Compression, Pipeline Method. Entropy Encoder, 2-D DCT, Image

I. INTRODUCTION

JPEG(Joint Photographic Expert Group[1]) related LSI chips are now being used in a wide range of multimedia applications, including digital still cameras and video capture systems[2]. JPEG itself specifies both the codec, which defines how an image is compressed into a stream of bytes and decompressed back into an image, and the file format used to contain that stream. Currently, high-quality image applications are performed on hand-held terminal[3]. A plenty of hand-held devices have embedded digital camera functionality. Such a digital camera system consists of an image sensor, image signal processor, image compressor/decompressor, video encoder/decoder, memory controller, interface circuitry to peripherals, and other devices[1].

CCD (Charge-Coupled Device) and CMOS (Complementary Metal Oxide Semiconductor) image sensors are two different technologies for capturing images digitally. Each has unique strengths and weaknesses giving advantages in different applications. Renewed interest in CMOS was based on expectations of lowered power consumption, camera-on-a-chip integration, and lowered fabrication costs from the reuse of mainstream logic and memory device fabrication[4].

Compression algorithms have made it possible to deliver various multimedia services over bandwidth-constrained wired and wireless networks[5]. It plays a important role especially when running applications in real-time, thus reducing the strain on streaming buffers.

JPEG baseline is the mode widely used in both software and hardware implementations of JPEG compressor[6]. Image encoding hardware is required for more and more data-intensive image transmission applications, such as high-resolution color image scanners, digital cameras with million-pixel resolution and so on. In order to overcome the long transmission latency and huge amount storage, image compression is required for these high-resolution image-processing devices[7]. For applications such as PC camera, digital still camera, and scanners with compression capability embedded, a dedicated architecture with hardware-optimized configuration is a cost-effective solution. With the recent advances in video applications such as video teleconferencing, HDTV, home entertainment systems, interactive visualization and multimedia, there is an increasing demand for even higher bandwidth computing and communication systems[8].

We studied an implementation of JPEG encoder in order to solve problems mentioned above. In this paper, we propose an efficient VLSI architecture for implementing the JPEG baseline compression standard algorithm. The proposed JPEG architecture fully exploits pipeline scheme to achieve high-speed and high-throughput.

This paper is organized as follows. In section II, overview of the JPEG compression standard is described. The proposed architecture for JPEG encoder is explained in section III. Simulation and results are shown in section IV. Finally, conclusions are given.

II. Overview of the JPEG Compression Standard

JPEG baseline encoder system is composed of three major parts, the 2-D Discrete Cosine Transform(DCT), the quantizer and the entropy encoder, as shown in Fig. 1.

JPEG baseline encoding is for images with 8-bit samples and uses Huffman coding only.

Manuscript received September 11, 2007.

Kyung-Hyun Kim and Seung-Il Sonh are with the Department of Information and Communications, Hanshin University, Osan, 447-791, Korea (Tel: +82-31-370-6819, Fax: +82-31-372-8198, Email: saisonh@hs.ac.kr)

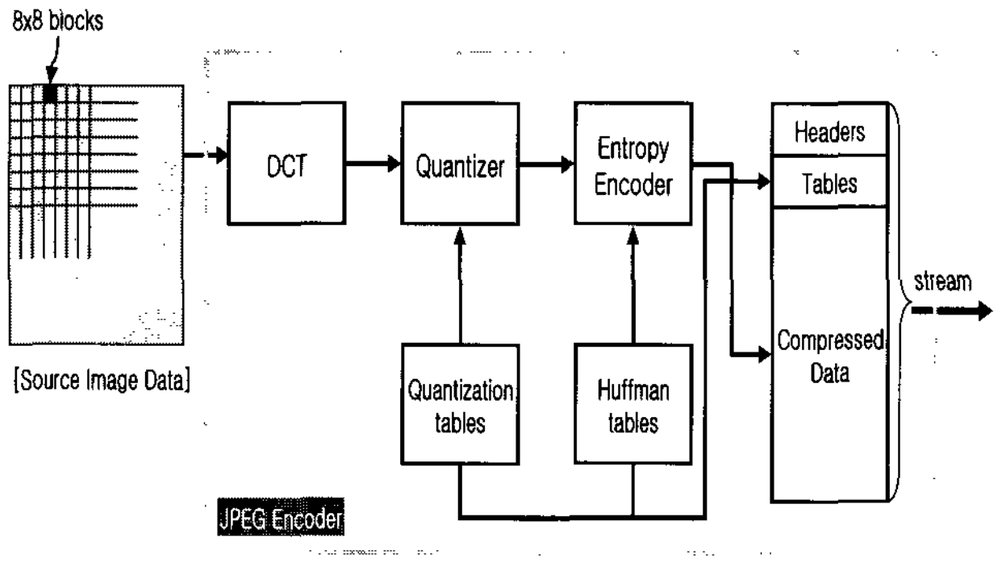


Fig. 1 Block diagram of JPEG encoder

In the JPEG encoding process, the input component's samples are grouped into 8x8 blocks, and each block is transformed by the forward DCT (FDCT) into a set of 64 values referred to as DCT coefficients. One of these values is referred to as the DC coefficient and the other 63 as the AC coefficients.

Each of the 64 coefficients is then quantized using one of 64 corresponding values from a quantization table. Applications may specify values which customize picture quality for their particular image characteristics, display devices, and viewing conditions.

After quantization, the DC coefficient and the 63 AC coefficients are prepared for entropy encoding, as shown in Fig. 2. The previous quantized DC coefficient is used to predict the current quantized DC coefficient, and the difference is encoded. The 63 quantized AC coefficients undergo no such differential encoding, but are converted into a one dimensional zig-zag sequence, as shown in Fig. 2.

The quantized coefficients are then passed to an entropy encoding procedure which compresses the data further. If Huffman encoding is used, Huffman table specifications must be provided to the encoder.

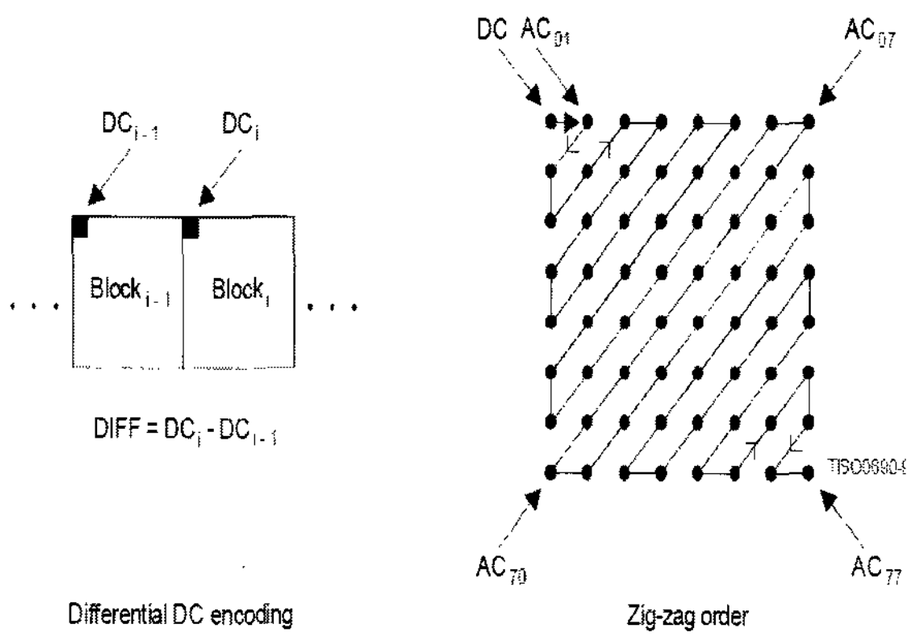


Fig. 2 Preparation of quantized coefficients for entropy encoding

The ordering of data units and the construction of minimum coded units(MCU) is defined as follows. JPEG defines the term MCU to be the smallest group of interleaved data units. For non-interleaved data the MCU is one data unit. For interleaved data the MCU is the sequence of data units defined by the sampling factors of the components in the scan. We will implement encoding for the color image. Color image is composed of 3-component, RGB or YCbCr. And the interleaved scheme is adopted in our design. When components are interleaved, each component Ci is partitioned into rectangular regions of Hi horizontal data units by Vi vertical data units, as shown in fig. 3. In fig. 3, MCU1 consists of data units taken from first from the top-left-most region of C1, followed by data units from the same region of C2, and likewise C3. MCU2 continues the pattern as shown.

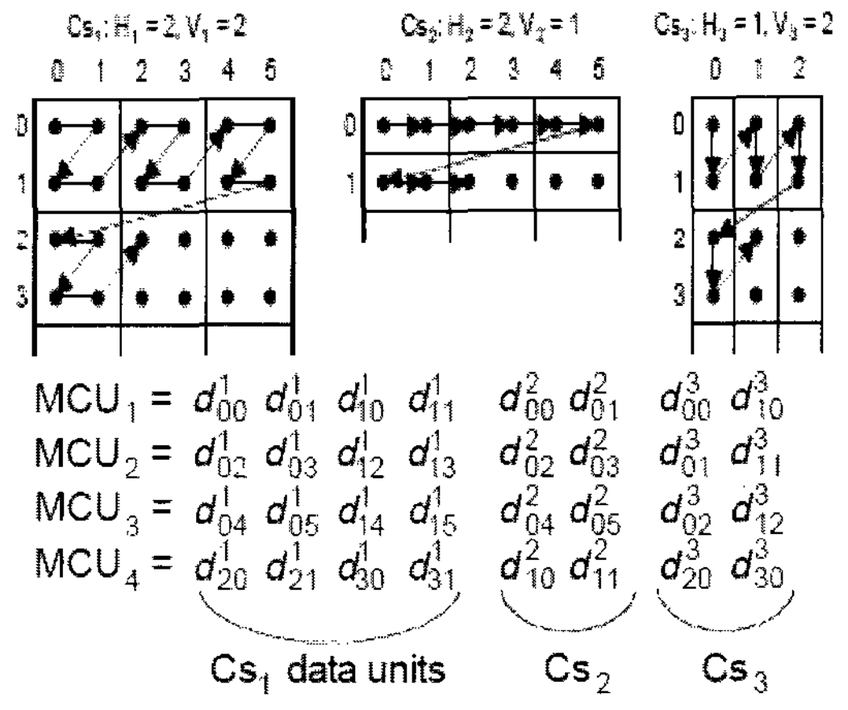


Fig. 3 Interleaved data encoding order based on MCU

JPEG frame header is present at the start of a frame. This header specifies the source image characteristics, the components in the frame, and the sampling factors for each component, and specifies the destinations from which the quantized tables to be used with each component are retrieved[1].

Markers serve to identify the various structural parts of the compressed data formats. Most markers start marker segments containing a related group of parameters. All markers are assigned two-byte codes. That is, they start with an X'FF byte followed by a byte which is not equal to 0 or X'FF. For example, start of frame marker for JPEG baseline encoder is assigned in X'FFC0 value. JPEG baseline encoder format begins with an SOI(Start of Image) marker, contains one frame, and ends with an EOI(End of Image) marker. RST marker is a conditional marker which is placed between entropy-coded segments only if restart is enabled. There are 8 unique restart markers(m=0…7) which repeat in sequence form 0 to 7, starting with zero for each scan, to provide a modulo-8 restart interval count. A frame begins with a frame header and contains one or more scans. DNL specifies the marker segment for defining the number of lines. This segment provides a mechanism for defining or redefining the number of lines in the frame at the end of the first scan. ECS means the entropy-coded segment. Fig. 4 shows the format of JPEG compressed frame.

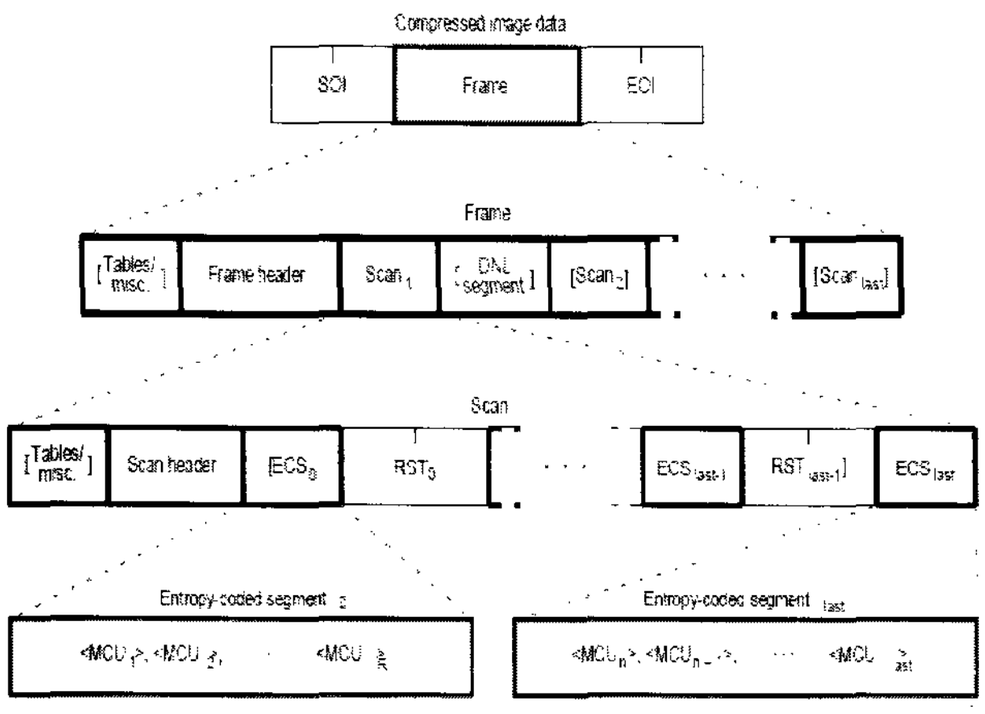


Fig. 4 The format of JPEG compressed frame

III. The Proposed Architecture

In this paper, the designed JPEG baseline encoder is fully implemented in pipelined scheme. Each of 8-bit pixels can be sequentially processed regardless of frame size. Architecture of JPEG baseline encoder designed in this paper is shown in fig. 4. Image signal processor(ISP) manipulates Bayer input stream received from CMOS image sensor(CIS) and executes an image signal processing so as to retrieve the original image and provides the output stream of RGB or YCbCr. The proposed JPEG encoder receives YCbCr data stream from ISP because YCbCr 4:2:2 or 4:2:0 sampling formats are used in JPEG encoding process.

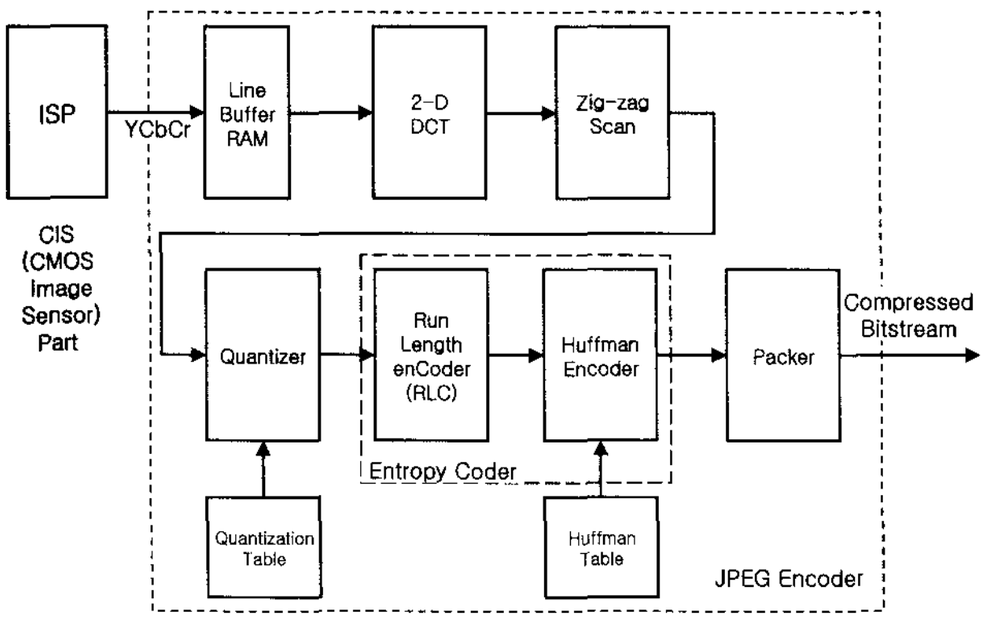


Fig. 4 Block diagram of the designed JPEG baseline Encoder

In order to rearrange the processing order in JPEG encoder for ISP input stream, line buffer RAM is required. In the line buffer RAM, inputted data are classified into Y, Cb, and Cr components to make JPEG encoding easy. The 2-D DCT block consists of a level shifter, 2 one-dimensional DCT circuits, and transpose buffer memory. The first DCT calculation is executed row-wise and the second DCT calculation column-wise[8]. The image pixels are level shifted to a signed representation by subtracting 2^{p-1}, where p is the precision parameter. JPEG baseline encoder uses p=8. Next, after reading in zig-zag scan order, quantization for DCT coefficients is performed in pipelined scheme using the non-restoring division algorithm[10]. The Entropy encoder is composed of RLC(Run Length Coding) and Huffman encoder. DC and AC components are differently processed in the entropy encoder. DC component uses a differential coding but AC components apply a run length encoding. In addition, Huffman encoder uses different Huffman tables for DC and AC components. Finally, the packer combines JPEG header and compressed image data and outputs the valid bitstream. Header and X'FF marker insertion block of the packer is designed to generate completely JFIF-compliant bitstream[11].

IV. Simulation and Results

The JPEG encoder was verified using both C software model and VHDL design. The VHDL language is commonly used to model hardware implementation of a top-down design methodology. In this paper, the JPEG encoder IP is simulated with model_sim 6.1i behavioral and timing simulation tool. Fig. 5 shows the simulation result for JEPG baseline encoder. JPEG encoder starts with an activation of line_buf_out_data_valid signal. After buffering LIFO during 4-clcok cycle, first 1-DCT is executed and after 6-clock delay, the results of 1-DCT computation are stored in transpose memory during 64-clock cycle. The operation of second 1-DCT is almost the same as first 1-DCT. After the completion of the second 1-DCT and transpose memory buffering, quantization for the coefficients is executed in 16-stage pipeline. Finally, the entropy-encoded results are outputted in compressed bitstream. The outputs of compressed bit streams are aligned to 32-bit wide.

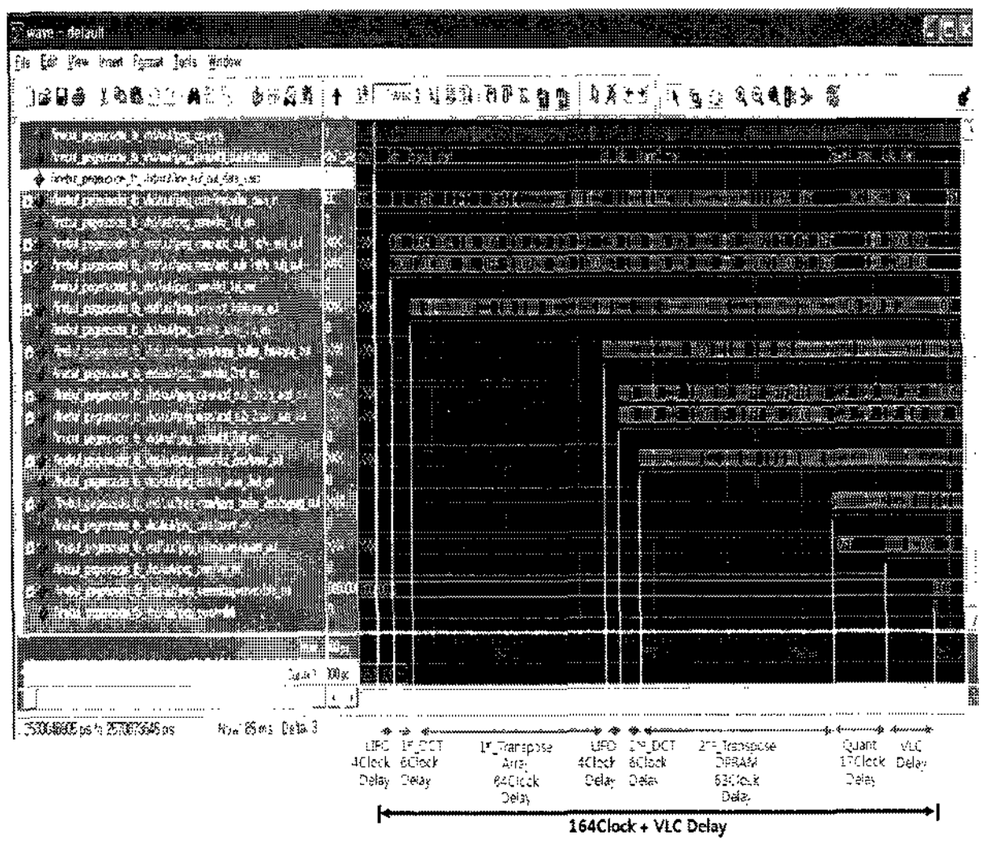


Fig. 5 Simulation result for JPEG encoder

Fig. 6 explains the pipeline operation of the proposed JPEG encoder. Each of 8x8 blocks is processed in the pipeline scheme. The second 8x8 block can be executed after 1-DCT completion of the first 8x8 block.

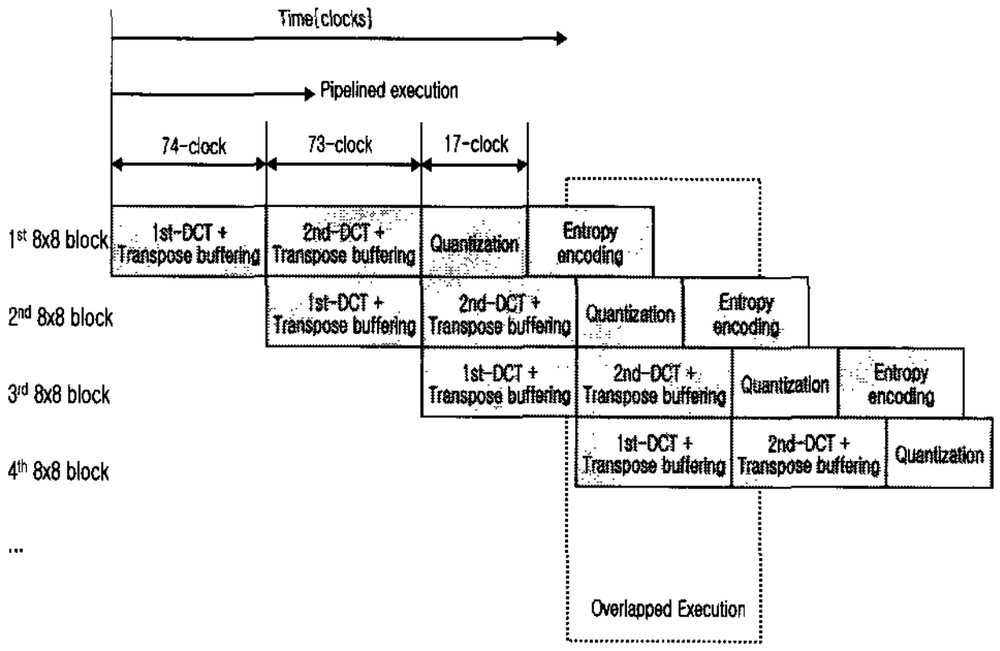


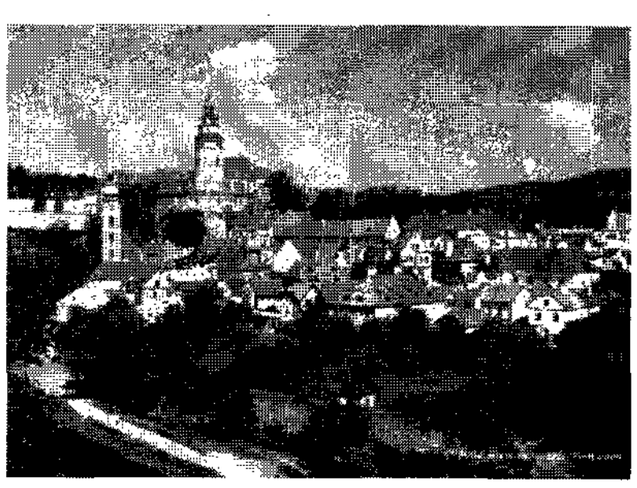
Fig. 6 Operation sequence of JPEG encoder

The JPEG encoder IP designed in this paper can consecutively compress the frames received from ISP module.

Fig. 7 compares the decompressed images from software compression and the designed JPEG hardware compression for 320x240-size resolution. The decompression results from Software and hardware compression show that the picture resolution is equal.

(a) Original

(b) software



(c) The designed JPEG IP

Fig. 7 Comparison results restored from software and the designed JPEG IP compression

The JPEG baseline encoder IP proposed is summarized at the table 1. The operating frequency of IP core is 60MHz at Xilinx Spartan xc3s1000 that is so low-cost FPGA(Field Programmable Gate Array) chip.

Our JPEG encoder supports 4:2:2 or 4:2:0 sampling formats which are used to compress the images generally.

JPEG encoding cycles for QVGA(320x240) LENA test image are approximately 154,000 clock-cycle. The compression time of JPEG encoder is almost equal for images because all the 8x8 blocks have to run DCT, quantization, and entropy encoding always. The JPEG encoder IP can compress over 389 frames for QVGA image and over frames for VGA(640x480) image and over 37 frames for XGA(1024x768). The JPEG encoder IP is designed to support various resolutions. Therefore, the designed JPEG encoder IP guarantees over 30 fps for high-resolution XGA image.

Table 1. Results of the JPEG encoder IP

Items	Our design
Operating frequency	60MHz
Sampling format	4:2:2, 4:2:0 (YCbCr)
Execution cycle for 320x240	Approximately 154,000 clock-cycle
Compression(320x240)	.Lena image -Raw file : 225KB -Compressed data : 10KB
Support of Over 30 fps	XGA(1024x768)
Device	Xilinx xc3s1000
# of gates	100,296
Characteristics	-Pipelined execution -Programmable image size

V. CONCLUSIONS

This paper presented the proposal and hardware implementation of architectures for JPEG baseline encoder. JPEG baseline encoder system consists of three major parts, the 2-D DCT, the quantizer and the entropy encoder. The entropy encoder is subdivided into run length encoder and Huffman encoder. The designed JPEG IP is implemented in pipeline scheme in order to process the high-speed compression. Therefore, the designed JPEG baseline encoder can process real-time image data compression.

The proposed JPEG encoder IP is suitable for applying in multimedia areas that need low cost and fast time-to-market.

ACKNOWLEDGMENT

This Work was supported by Hanshin University Research Grant in 2008.

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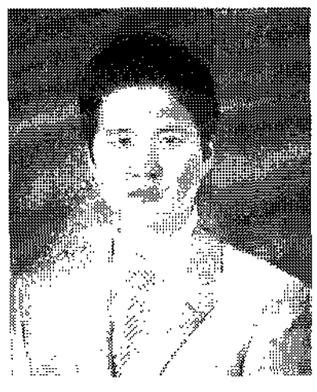
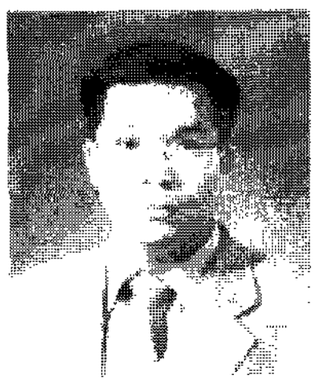


Kyung-Hyun Kim

Received the B.S. degree in information and communications from Hanshin University, Korea, 2007. He has been an M.S. student in the department of information and communication at Hanshin University since 2007. His research interests include ASIC design and video CODEC.



Seung-Il Sonh

Received the B.S., M.S. degrees and Ph.D in electronics engineering from Yonsei University, Korea, in 1989, 1991, and 1998, respectively.
He has been with the department of information and communication at Hanshin University since 2002 and he is now an associate professor. His research interests include ATM switching system, MAC protocol, camera ISP and video CODEC.