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Solid Phase Crystallization Kinetics of Amorphous Silicon at High Temperatures

Won-Eui Hong, Bo-Kyung Kim, Jae-Sang Ro*

Department of Materials Science and Engineering, Hongik University, Seoul 121-791, Korea

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Abstract

Solid phase crystallization (SPC) of amorphous silicon is usually conducted at around 600°C since it is used in the application of flat panel display using thermally susceptible glass substrate. In this study we conducted SPC experiments at temperatures higher than 600°C using silicon wafers. Crystallization rate becomes dramatically rapid at higher temperatures since SPC kinetics is controlled by nucleation with high value of activation energy. We report SPC kinetics of high temperatures compared to that of low temperatures.

Keywords: Solid phase crystallization, Polycrystalline silicon, Kinetics, Nucleation

1. Introduction

Sold phase crystallization (SPC) is a simple method in producing a polycrystalline phase by annealing amorphous silicon (a-Si) in a furnace environment. Extensive researches on SPC have been conducted over the past 20 years. Modified methods based on SPC such as metal induced crystallization (MIC) and metal induced lateral crystallization (MILC) have been developed. Main motivation of these crystallization techniques is to fabricate low-temperature-polycrystalline-silicon thin-film-transistors (LTPS-TFTs) on a thermally susceptible glass substrate for the applications of active matrix liquid crystal display (AMLCD), or, active matrix organic light emitting diode (AMOLED). It, however, takes too long time for complete crystallization when SPC is done at 600°C, a typical crystallization temperature. Catalytic reaction of MIC, or, MILC has been proven to be effective in lowering the crystallization temperature, but not in reducing the crystallization time significantly. Moreover, these methods are not free from metallic contamination, which seriously causes to be the source of leakage current of TFT devices. Unless a suitable gettering technique is implemented it is not easy to utilize them in the production line.

*Corresponding author. E-mail : jsang@wow.hongik.ac.kr

Studies on SPC have been naturally focused to the low temperature regime. Recently, fabrication of polycrystalline silicon (poly-Si) TFT circuits from a high-temperature-polycrystalline-silicon (HTPS) process on steel foil substrates was reported[1-3]. Although steel is not adequate for transmissive displays due to an opaque nature it can be used for emissive and reflective ones. Since a thin steel substrate is flexible it can also use a roll to roll process. Crystallization at lower temperatures is no longer required when using a steel foil. Solid phase crystallization of a-Si films proceeds by nucleation and growth. After nucleation polycrystalline phase is propagated via twin mediated growth mechanism. Elliptically shaped grains, therefore, contain intra-granular defects such as micro-twins[4,5]. Both the intra-granular and the inter-granular defects reflect the crystallinity of SPC poly-Si. We will discuss SPC kinetics of high temperatures compared to that of low temperatures.

2. Experimental

500 nm-thick thermally grown SiO_2 was deposited on 100 mm Si wafers. Then, 50 nm-thick amorphous silicon films were deposited at 350°C in a plasma-enhanced-chemical-vapor-deposition (PECVD) reactor. After the film deposition a-Si films were isothermally annealed as a function of time at temperatures ranging

from 600°C to 1000°C in a nitrogen ambient using a quartz tube furnace. The degree of crystallization was determined as a function of annealing time using Raman spectroscopy. Dark field transmission electron microscopy (TEM) was employed in measuring the average grain size of SPC poly-Si.

3. Results and Discussion

In order to investigate the temperature dependence of the crystallization kinetics and grain size, we conducted SPC experiments using silicon wafers that had the structure of a 50 nm-thick a-Si/500 nm-thick SiO_2/silicon wafer. Crystallization was carried out using a tube furnace at temperatures ranging from 600°C to 1000°C. In addition, Raman spectroscopy was used to determine the nominal incubation and crystallization time. Table 1 shows nominal incubation time and crystallization time as a function of crystallization temperature. While the crystallization process was completed in 20 hrs at 600°C, it was over in 25 sec at 1000°C. Since SPC kinetics is controlled by the nucleation rate, and the amount of activation energy needed to nucleate silicon crystals is very high[6], the crystallization rate is dramatically increased when the crystallization temperature is raised.

Moreover, in the case of furnace annealing, the sample was found to be unable to reach the setting temperature of 1000°C within 25 sec. As indicated in Fig. 1, we measured the resistance of silicon as a function of annealing time at 650°C. As soon as we put the sample into a furnace the value of resistance was measured to be more than 6000 kΩ. It continuously decreases due to generation of intrinsic carriers and reaches to thermal equilibrium value after around 4 min. This means that the temperature of the sample reaches to the setting temperature after 4 min due to very slow heating rate of a furnace. Therefore SPC kinetics should be carefully analyzed when using a conventional furnace or even when using an of rapid thermal annealing (RTA) system.

Table 1. Nominal incubation and crystallization time vs. crystallization temperature

	Nominal incubation time	Nominal crystallization time
600°C	~ 4 hrs	~ 20 hrs
650°C	< 10 min	~ 3 hrs
700°C	< 2 min	~ 20 min
750°C	< 1 min	~ 6 min
800°C	< 20 sec	~ 3 min
850°C	< 20 sec	~ 2 min
900°C	< 15 sec	~ 1 min
950°C	< 10 sec	~ 40 sec
1000°C	< 5 sec	~ 25 sec

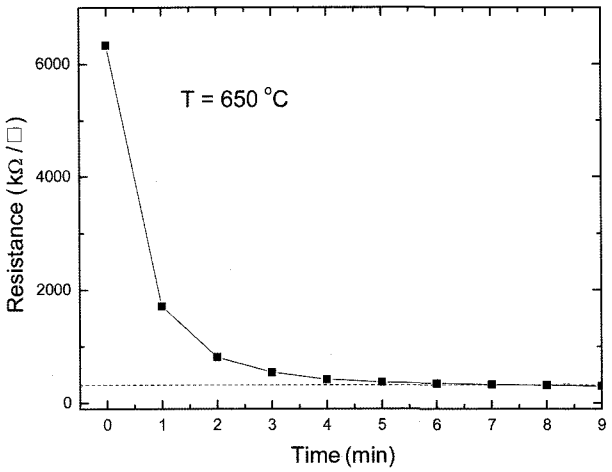

Fig. 1. Sheet resistance of silicon vs annealing time at 650°C.

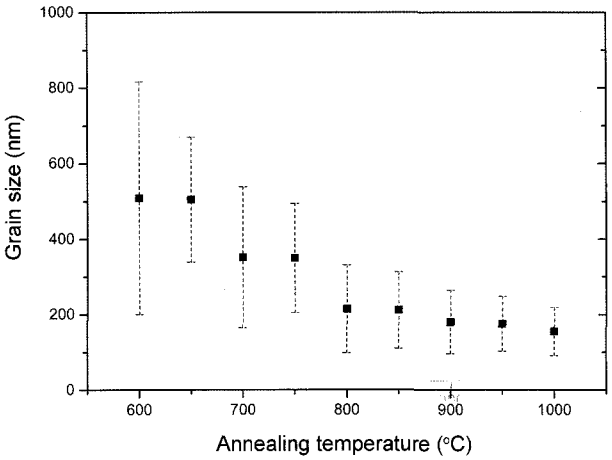

Fig. 2. Grain size vs. annealing temperature.

As indicated in Fig. 2, the average grain size was measured as a function of crystallization temperature. Dark field TEM was used to calculate the average grain size of the 100 large grains that were selected. Since the grains of SPC poly-Si are elliptical in shape, we measured the lengths of the long and short axes respectively. The grain size was then calculated using the equation $(\pi ab)^{1/2}/2$, where a and b are the lengths of the long and short axes respectively. The grain size was found to decrease as the annealing temperature was increased from 600°C to 800°C. However, it was discovered to be less sensitive to annealing temperature at temperatures beyond 800°C. As crystallization kinetics becomes very rapid and the heating rate of a conventional furnace is slow, a phase transition to polycrystalline silicon may occur

in the course of heating-up. Such a phase transition to polycrystalline silicon may occur in the course of heating-up even in the case of RTA, which exhibits the highest heating rate of the conventional heat treatment methods, because the heating rate is only about 100°C/sec. Thus, the desired microstructure formed at a high temperature cannot be reflected.

Since SPC kinetics is controlled by the nucleation rate, and the activation energy needed to nucleate silicon crystals has a high value of 3.9 eV[6], the crystallization rate is dramatically increased when the crystallization temperature is raised. Moreover, in the case of furnace annealing, the sample was found to be unable to reach the setting temperature of 1000°C within 25 sec as we discussed earlier. Fig. 3 indicates an Arrhenius plot of an incubation time. The dotted line represents the measured data while the solid straight line denotes the estimated data using the nucleation activation energy of 3.9 eV with the measured data under 650°C. The measured and estimated incubation time are summarized in Table 2 at crystallization temperatures ranging from 600°C to 1300°C. It can be seen that the incubation time becomes less than 1 msec at temperatures above 1000°C.

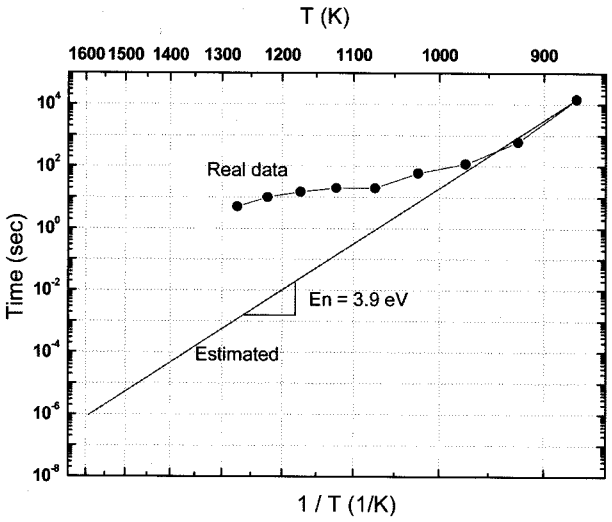

Fig. 3. Arrhenius plot of an incubation time. The dotted line corresponds to the real data and the solid line represents the estimated ones using the nucleation activation energy of 3.9 eV with the measured data under 650°C.

Table 2. Measured and estimated incubation time vs. crystallization temperature

	Measured incubation time	Estimated incubation time
600°C	~ 4 hrs	4 hrs
700°C	< 2 min	1.16 min
800°C	< 20 sec	912 ms
900°C	< 15 sec	25.01 ms
1000°C	< 5 sec	1.2 ms
1050°C	N/A	314.5 μs
1100°C	N/A	90.5 μs
1150°C	N/A	28.4 μs
1200°C	N/A	9.64 μs
1250°C	N/A	3.52 μs
1300°C	N/A	1.37 μs

4. Conclusions

SPC kinetics is controlled by the nucleation rate and the activation energy needed to nucleate has a high value of 3.9 eV. Thus the rate of crystallization becomes dramatically rapid at higher temperatures. Due to rapid kinetics at high temperatures and also due to slow heating rate when using a conventional furnace the microstructure of SPC poly-Si at high temperatures may not truly reflect the one at that temperature. The SPC kinetics and the microstructure of poly-Si at high temperatures should be carefully analyzed.

Acknowledgements

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