A New Semi-Empirical Model for the Backgating Effect on the Depletion Width Modulation in GaAs MESFET's

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Abstract—**A simple and efficient way of modeling backgating in GaAs MESFET's is presented through depletion width modulation of Schottky junction and channel-substrate interface. It is shown semi-empirically that such a modulation of depletion widths causes serious troubles in designing precision circuits since backgating drastically reduces threshold voltage of MESFET as well as drain current. Finally, some of the results are compared with reported experimental results. This model may serve as a starting point for rigorous characterization of backgating effect on various device parameters of GaAs MESFET's.**

Index Terms—**GaAs MESFET, semi-insulating substrate, backgating effect, depletion width modulation, threshold voltage**

I. INTRODUCTION

The 'backgating effect' refers to the phenomenon that the drain current of MESFET decreases when a negative voltage is applied to a nearby electrode or to the backside of the substrate [1-3]. Such an effect can cause undesirable coupling or cross talk between adjacent devices that can limit the integration scale of GaAs IC's. The cause of this undesirable effect was thought to be due to deep-level impurities near the substrate [2-3], and hence the insertion of several kinds of buffer layers in epitaxial structures was proposed to reduce it and improve RF performance [4]. However, the negative backgate bias could modulate the space charge region below Schottky gate [5]. The experimental results of [5] reveal that a small portion of gate of the MESFET that is in direct contact with the semi-insulating substrate enhances backgating effect. Hence any misalignment during photolithography could result in the tip of the gate metal of the MESFET touching the undoped GaAs resulting sudden rise in leakage current. More interestingly, backgating is one of the possible sources that cause significant discrepancies when one tries to compare one foundry process to others as Stoneham [6] reported. So it has to be well characterized and taken into account in order to apply a physical model to devices fabricated in varieties of foundries. A purely qualitative approach to understand these effects is less than adequate for the circuit designer who really needs a quantitative model.

In this paper, we have tried to present a quantitative model to describe the effect of a backgate voltage not only on the depletion region around the channel-substrate junction (which is normally considered in modeling the backgating effect) but also on the depletion region due to Schottky-junction at the gate of a GaAs MESFET. The work is based on the experimental observation reported by Wu et al [5]. The present work has mainly focused on building up a semi-empirical model for the backgating effect on the modulation of the depletion region below the Schottky-gate. The MESFET is assumed to be fabricated on a semi insulating substrate. For the completeness, we have also included the effect of the backgate voltage on the channel-substrate junction. Finally, adverse effect of backgating on various device parameters such as threshold voltage reduction and drain current suppression is analytically modeled. Some of the results

Manuscript received Mar. 4, 2008; revised Mar. 11, 2008.
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of this model are compared with reported experimental results. An encouraging correspondence between them lends to the credibility of the model.

II. THEORETICAL MODEL

The schematic structure of GaAs MESFET operated in linear region is shown in fig.1. Negative voltage (V_{bg}) is applied to the ohmic contact on the backside of the substrate (backgate) to study backgating effect. Fringe portion of the Schottky gate is assumed to be in direct contact with the substrate as shown in the inset of the same figure. Active region of MESFET is an n-GaAs that can be obtained by implanting Si into GaAs substrate. However, uniform doping in the channel is assumed for simplicity of the model. Generally, there is a threshold voltage (V_{thbg}) associated with the onset of backgating above which drain current is substantially reduced with further increase in backgate voltage. Wu *et al.* [5] extracted depletion width of Schottky junction from the measured C-V characteristics at 1MHz for different substrate voltages. This effect can be included in Schottky depletion width as an additional voltage applied to the gate. The additional voltage (say $f(V_{bg})$) can be obtained from measured depletion width

$$f(V_{bg}) = \begin{cases} 0 & \text{for } V_{bg} \le V_{thbg} \\ (d_{measured})^2\left(\dfrac{qN_d}{2\varepsilon_s}\right) - V_{bi} + V_{gs} & \text{for } V_{bg} > V_{thbg} \end{cases} \quad (1)$$

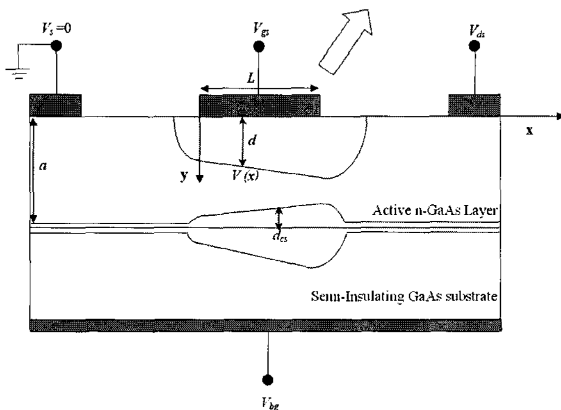


Fig. 1. Schematic diagram of a GaAs MESFET operated in the linear region. The inset of the figure shows the top view of the MESFET where the hatched section is the fringe portion of the gate that is in direct contact with the substrate.

where $d_{measured}$ is the experimental value of the Schottky depletion width for different backgate voltages at $V_{gs} = 0$ [5], ε_s is the permittivity of GaAs, q is the electron charge, N_d is the donor concentration, V_{bi} is the built-in potential of Schottky junction, $V_{gs} \le 0$ is gate-source voltage and V_{bg} is the absolute value of voltage applied to backgate.

We performed second order interpolation of $f(V_{bg})$ in Eqn. (1) with the measured Schottky depletion width from [5] using the following relation

$$f(V_{bg}) = \begin{cases} 0 & \text{for } V_{bg} \le V_{thbg} \\ \alpha_1(V_{bg} - V_{thbg}) + \alpha_2(V_{bg} - V_{thbg})^2 & \text{for } V_{bg} > V_{thbg} \end{cases} \quad (2)$$

where α_1 and α_2 are two empirical parameters dependent on the substrate properties which can be obtained from experimental or from simulation results.

Once $f(V_{bg})$ is modeled it can be easily introduced in Schottky depletion width as

$$d = \left[\frac{2\varepsilon_s}{qN_d}\left(V_{bi} - V_{gs} + f(V_{bg}) + V(x)\right)\right]^{1/2} \quad (3)$$

where $V(x)$ is the channel potential at any point in x-direction.

For the sake of completeness, we considered modification of depletion width at channel-substrate junction by backgate voltage also. It was generally agreed that when backgate voltage is below certain threshold voltage (V_{thbg}) substrate maintains its high resistance as a good insulator with most of the voltage dropping across it. But when the backgate voltage is greater than the threshold, impact ionization of deep traps occurs resulting a net decrease of the substrate resistivity with the excess voltage ($V_{bg} - V_{thbg}$) drops across the channel-substrate junction thus widening the depletion region and narrowing the channel opening [7]. The voltage across the channel-substrate junction can be modified as

$$V_{cs} = \begin{cases} V_{bics} & \text{for } V_{bg} \le V_{thbg} \\ V_{bics} + (V_{bg} - V_{thbg}) & \text{for } V_{bg} > V_{thbg} \end{cases} \quad (4)$$

where V_{bics} is the built-in potential across channel-substrate junction.

The depletion width in the channel side of the channel-substrate junction can be obtained by solving the one- dimensional Poisson's equation with appropriate boundary conditions [7], which is approximately given by

$$d_{cs} = \left[\frac{2\varepsilon_s}{qN_d} \left(\frac{N_{sub}}{N_{sub} + N_d} \right) (V_{cs} + V(x)) \right]^{1/2} \tag{5}$$

where N_{sub} is the total negative charge concentration due to trapping of electrons by the EL2 levels in the substrate [2].

Clearly, the effective channel-opening for the carriers in the active region of MESFET is $a_{eff} = a - d - d_{cs}$.

The pinch-off voltage of the device for $V_{ds} = 0$ is given by

$$V_{po} = \frac{qN_d}{2\,\varepsilon_s} \left(a - d_{cs}(L)\Big|_{V_{ds}=0} \right)^2 = \frac{qN_d}{2\,\varepsilon_s} \left(a - \sqrt{\frac{2\varepsilon_s V_{cs}}{qN_d} \left\{ \frac{N_{sub}}{N_d + N_{sub}} \right\}} \right)^2 \tag{6}$$

The threshold voltage of the MESFET including the backgating is

$$V_{th} = \left\{ V_{bi} + f(V_{bg}) \right\} - \left\{ \frac{qN_d}{2\,\varepsilon_s} \left(a - \sqrt{\frac{2\varepsilon_s V_{cs}}{qN_d} \left\{ \frac{N_{sub}}{N_d + N_{sub}} \right\}} \right)^2 \right\} \tag{7}$$

It may be noted that by neglecting the deep level traps (i.e. $N_{sub} = 0$) and backgating effect (i.e. $V_{bg} = 0$), the threshold voltage equals to $V_{bi} - \frac{qN_d a^2}{2\,\varepsilon_s}$ which represents the threshold voltage of the conventional MESFET's $(V_{th,con})$ [8].

The saturated drain current of GaAs MESFET with the inclusion of the backgating effect is given by (see appendix)

$$I_{ds,sat} = \frac{Z\mu_n q^2 N_d^2 a^3}{6\varepsilon_s (L - L_s)} \left[3\left(\frac{V_{sat}}{V_{po}} \right) - 2\left(\left(\frac{V_{sat} - V_{gs} + f(V_{bg}) + V_{bi}}{V_{po}} \right)^{\frac{3}{2}} - \left(\frac{V_{bi} - V_{gs} + f(V_{bg})}{V_{po}} \right)^{\frac{3}{2}} \right) - 2\left(\frac{N_{sub}}{N_d + N_{sub}} \right) \left(\left(\frac{V_{sat} + V_{cs}}{V_{po}} \right)^{\frac{3}{2}} - \left(\frac{V_{cs}}{V_{po}} \right)^{\frac{3}{2}} \right) \right] \tag{8}$$

The normalized saturated drain current can be defined as

$$I_{norm} = \frac{I_{ds,sat}}{I_{ds,sat}\Big|_{V_{bg}=0}} \tag{9}$$

where $I_{ds,sat}\Big|_{V_{bg}=0}$ represents the drain current at zero backgate bias.

III. RESULTS

We extracted $f(V_{bg})$ from Eqn. (1) using the measured depletion width of [5] and performed second order interpolation of $f(V_{bg})$ using Eqn. (2). We got the best fit with the extracted $f(V_{bg})$ for $\alpha_1 = -0.051$ and $\alpha_2 = 0.05$. Fig.2 shows the comparison between the extracted and interpolated data. Once α_1 and α_2 are obtained, the Schottky depletion width can be modified according to Eqn. (3). If the substrate properties are known, the depletion width in the channel side of the channel-substrate junction can be easily evaluated. The threshold voltage variation as a function of backgate bias is shown in figure 3. Various parameters used in this calculation have been taken from [3]. It can be observed that when the backgate bias is more than V_{thbg}, the threshold

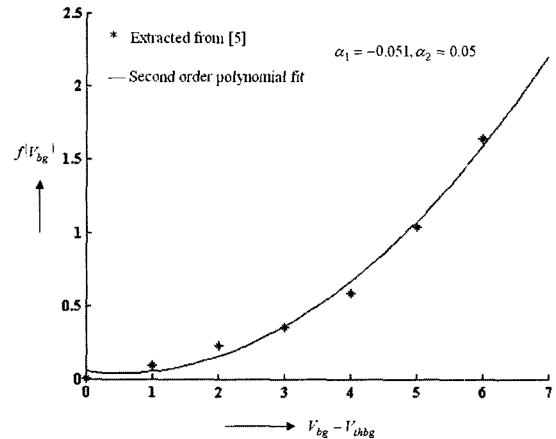


Fig. 2. Second order interpolation of $f(V_{bg})$ to include the effect of the backgating on the Schottky-junction depletion-width modification of a GaAs MESFET. The function $f(V_{bg})$ is extracted from the measured depletion width for different backgate bias in [5] with V_{thbg} as 3V.

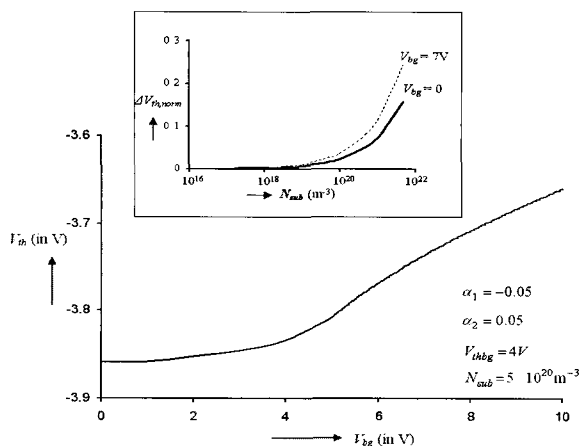


Fig. 3. The effect of backgate voltage on the threshold voltage of a MESFET. Inset of the figure shows the dependence of the normalized shift in the threshold voltage $V_{th,norm}$ on the degree of substrate compensation (Nsub) for different back bias voltages (Vbg).

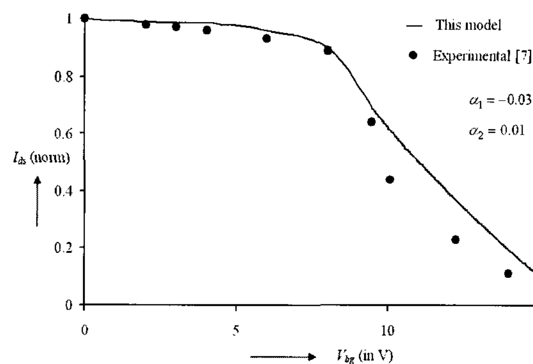


Fig. 4. The dependence of the normalized saturation drain current (normalized by dividing current under zero backgate bias) of the GaAs MESFET on the backgate voltage. The computed result of the normalized Ids is compared with the experimental result of [7]. Various parameters used in this comparison are: $a = 0.12\mu\text{m}$, $N_d = 2\times10^{23}\text{m}^{-3}$, $V_{ds} = 2.5V$, $V_{gs} = 0V$, $N_{sub} = 5\times10^{21}\text{m}^{-3}$, $V_{bi} = 0.7V$ and $V_{thbg} = 8V$.

voltage of the MESFET is severely degraded which closely tracks the experimental observations of [3]. The normalized threshold voltage shift of the MESFET from $V_{th,con}$ $\left(\Delta V_{th,norm} = \left(V_{th,con} - V_{th}\right)/V_{th,con}\right)$ with the degree of the substrate compensation $\left(N_{sub}\right)$ for different backgate voltages is depicted in the inset of fig.3. Even without the presence of the backgate voltage, $\Delta V_{th,norm}$ increases substantially i.e. the threshold voltage of the MESFET degrades due to the presence of the deep level traps in the substrate. For low N_{sub} , the shifting in the threshold voltage is observed to be very small (typically less than 10% for MESFET with N_{sub} in the order of 10^{20}-10^{21} m^{-3} which corresponds to N_{EL2} in the range of 1 x10^{22}-2x10^{22} m^{-3}). Since the EL2 concentration in a GaAs substrate grown by the LEC fluctuates across wafer possibly due to the thermal stress during crystal growth, the threshold voltage of the MESFET fabricated on such a wafer also fluctuates as shown by Anholt *et al.* [10]. As the EL2 concentration increases, more carriers in the channel get trapped by the EL2 levels leading to more negative concentration in the substrate side which decreases the effective channel opening requiring lesser gate voltages to pinch off the channel. Hence, the increase in N_{sub} merely reflects the case of the increase in the EL2 concentration in the substrate. The decrease in the threshold voltage is more pronouncing when the backgate voltage$\left(V_{bg}\right)$ is greater than V_{thbg} . Hence, a closely compensated substrate (in which EL2 concentration closely compensates the shallow acceptor and shallow donor concentration leading to smaller N_{sub}) produces minimum backgating effect on the threshold voltage of a MESFET. Fig. 4 demonstrates the suppression of the normalized drain current in the saturation region by the application of a backgate voltage. The normalized drain current of our model is compared with the reported experimental results [7]. Both of the results clearly demonstrates the conventional backgating effect in terms of a sudden drop in the normalized drain current for the backgate voltage exceeding a certain threshold value.

It may be mentioned here that the fitting parameters of an empirical model are often determined by comparing the model with either a known experimental or simulation result of the device. Once the parameters of the empirical model are so obtained for a particular device, the model becomes ready to use for designing circuits and systems with the device for various applications. Since, the similar devices but with different device parameters result in different device characteristics, two different sets of values for α_1 and α_2 are obtained for the two different MESFET's of Refs. [5] and [7]. The values of α_1 and α_2 have been extracted in Fig.2 and Fig.4 by using the curve fitting technique to obtain the best matching between the

model and experimental results for the MESFET's of Refs. [5] and [7] respectively. However, the values of α_1 and α_2 in Fig. 3 are assumed to be same as in Fig.2.

IV. CONCLUSIONS

In this paper, we have made an attempt to quantify backgating effect in GaAs MESFET through the depletion width modulations at the Schottky-junction and channel-substrate interface. An empirical relation has been developed to model the fraction of the backgate voltage which is propagated through the semi-insulating substrate and superimposed on the gate voltage of a GaAs MESFET. The depletion width modulation in the channel-substrate interface has been modeled by using an analytical method. The developed models for the depletion width-modulations in the two depletion regions have been used in the conventional analytical model to characterize the backgating effect of the device. Further, to emphasize the importance of such modeling, the threshold voltage variation and the drain current suppression due to the backgating are obtained by using the effective channel opening in the active region of the device. Some of the results have been compared with the reported experimental results to show the validity of our proposed model in terms of a reasonable matching between the two. We strongly believe that this model may serve as a staring step for the rigorous characterization of the backgating effect in the GaAs MESFET MMICs fabricated on a semi-insulating substrate.

APPENDIX

The drain-source current of a GaAs MESFET in the linear region, including the deep level traps and backgating can be obtained by replacing the channel opening by an effective channel opening a_{eff} in the model of ref.[8] which can be written as

$$I_{ds}=\frac{Z\mu_n q^2 N_d^2 a^3}{6\varepsilon_s L}\left[3\left(\frac{V_{ds}}{V_{po}}\right)-2\left(\left(\frac{V_{ds}-V_{gs}+f(V_{bg})+V_{bi}}{V_{po}}\right)^{\frac{3}{2}}-\left(\frac{V_{bi}-V_{gs}+f(V_{bg})}{V_{po}}\right)^{\frac{3}{2}}\right)\right.$$
$$\left.-2\left(\frac{N_{sub}}{N_d+N_{sub}}\right)\left(\left(\frac{V_{ds}+V_{cs}}{V_{po}}\right)^{\frac{3}{2}}-\left(\frac{V_{cs}}{V_{po}}\right)^{\frac{3}{2}}\right)\right] \qquad \text{(A1)}$$

where μ_n , a and L are mobility of electrons, channel height and gate length respectively. The last term in the above equation represents reduction in drain current due to the deep level traps in the substrate. The application of a backgate voltage further increases the widths of both of the depletion regions at the Schottky-juction and channel-substrate junction, which in turn directly reduces the drain current. Equation 8 is strictly valid up to the onset of the velocity saturation $(V_{ds}=V_{sat})$ at which electric field in the channel below gate reaches the saturation electric field (E_s) . The drain voltage at the onset of the velocity saturation is given by [9]

$$V_{sat}\approx\frac{(V_{gs}-V_{bi}+V_{po})E_s L}{E_s L+V_{gs}-V_{bi}+V_{po}} \qquad \text{(A2)}$$

When a MESFET is operated in the saturation region (i.e. beyond V_{sat}), both the depletion regions laterally extend towards drain and source which in turn modulates the channel length. As a result, the drain current will increase with a finite slope in I-V characteristics. In a physical model channel length modulation is the phenomenon producing finite output conductance in the saturation region. The effective channel length in the saturation region is

$$L_{eff}=L-L_s \qquad \text{(A3)}$$

where L_s is length of the velocity saturation region below the Schottky gate [9] and is given by

$$L_s=2.06\,K_d\left(\frac{\varepsilon_s(V_{ds}-V_{sat})}{q\sqrt{n_{cr}}N_d}\right)^{1/2} \qquad \text{(A4)}$$

here K_d is a domain parameter and n_{cr} is the characteristic doping density of GaAs [9].

Finally, the drain current in the saturation region with all the major effects included is given by

$$I_{sat}=\left(\frac{L}{L_{eff}}\right)\left(I_{ds}\big|_{V_{ds}=V_{sat}}\right) \qquad \text{(A5)}$$

REFERENCES

[1] Y. Ohno and N. Goto, "Mechanism of electrostatic potential conduction in semi insulating substrates," *J. Appl. Phys*, vol. 66, pp. 1217-1221, 1990.

[2] C. Kocot and C. A. Stolte, "Backgating in GaAs MESFET's," *IEEE Trans. Microwave Theory Tech*, vol. 30, pp. 963-968, 1982.

[3] K. Shenai and R. W. Dutton, "Channel-buffer (substrate) interface phenomenon in GaAs MESFET's fabricated by molecular-beam epitaxy," *IEEE Trans. Electron Devices*, vol. 35, pp. 590-603, 1988.

[4] A. E. Bond, C. K. Lin, M. H. McDougal, P. D. Dapkus, K. Kaviani, O. Adamczyk, and R. Nottenburg, "Backgating reduction in MESFETs using an AlAs native oxide buffer layer," *Electron Lett.*, vol. 32, pp. 2271-2273, 1996.

[5] J. Wu, Z. G. Wang, T. W. Fan, and L. Y. Lin, "Sidegating effect on Schottky contact in ion-implanted GaAs," *J. Appl. Phys.*, vol. 78, pp. 7422-7423, 1995.

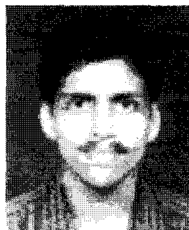
[6] E. B. Stoneham, P. A. J O'Sullivan, S. W. Mitchell, and A. F. Podell, "Working with nine different foundries," *12th annual GaAs IC Symp.,* 1990 Tech Digest, pp. 11-14, 1990.

[7] Y. H. Chen, Z. G. Wang, J. J. Qian, and M. F. Sun, "Threshold behavior in backgating in metal-semiconductor field effect transistor: Induced by limitation of channel-substrate junction to leakage current," *J. Appl. Phys.*, vol. 81, pp. 511-515, 1997.

[8] S. M. Sze, *Physics of Semiconductor Devices* 2nd ed., New Delhi: Wiley, 1999.

[9] Michael Shur, *GaAs Devices and Circuits*, New York: Plenum press, 1986.

[10] R. Anholt and T. W. Sigmon, "Mechanism of EL2 effects on GaAs field-effect transistor threshold voltages", *J. Appl. Phys.*, vol. 62, pp. 3995-3997, 1987.



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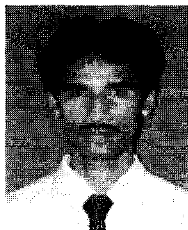

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