A Nonvolatile Refresh Scheme Adopted 1T-FeRAM for Alternative 1T-DRAM

Hee-Bok Kang*,, Bok-Gil Choi***, and Man Young Sung***

***Abstract*—1T1C DRAM has been facing technological and physical constraints that make more difficult their further scaling. Thus there are much industrial interests for alternative technologies that exploit new devices and concepts to go beyond the 1T1C DRAM technology, to allow better scaling, and to enlarge the memory performance. The technologies of DRAM cell are changing from 1T1C cell type to capacitor-less 1T-gain cell type for more scalable cell size. But floating body cell (FBC) of 1T-gain DRAM has weak retention properties than 1T1C DRAM. FET-type 1T-FeRAM is not adequate for long term nonvolatile applications, but could be a good alternative for the short term retention applications of DRAM. The proposed nonvolatile refresh scheme is based on utilizing the short nonvolatile retention properties of 1T-FeRAM in both after power-off and power-on operation condition.**

***Index Terms*—1T1C DRAM, floating body cell (FBC) 1T DRAM, 1T-gain DRAM, FET-type 1T-FeRAM, nonvolatile refresh scheme**

I. INTRODUCTION

Ferroelectric RAM (FeRAM or FRAM) is a type of non-volatile memory based on electric field orientation and with near-unlimited number (exceeding 1E14) of write and read cycles. FeRAM combines the advantages of SRAM or DRAM in which writing is roughly as fast as reading (less 100 ns), and EEPROM or Flash non-volatility. FeRAM does not yet offer the high density of DRAM or Flash. Non-volatile FeRAM offers an optimized, most cost-effective solution for a variety of advanced electronic metering systems, whether metering electricity, water, gas, or heat. FeRAM process technology is compatible with industry standard CMOS manufacturing processes. A ferroelectric thin film is placed over CMOS base layers and sandwiched between two electrodes. High permittivity FeRAM memory cell capacitor is also very useful in analog circuits as high capacitance capacitor and removing the conventional PIP (poly insulator poly) and MIM (metal insulator metal) capacitor process. It is possible to make a ferroelectric memory chip only using two additional masking steps during normal semiconductor manufacture, leading to the possibility of full integration of FeRAM into the microcontrollers and other chips. Flash typically requires nine masks. This makes FeRAM particularly attractive as an embedded non-volatile memory on microcontrollers, where the simpler process can reduce costs. Flash solid state disks (SSDs) have undoubtedly gained a strong foothold in the military and enterprise markets. Current technology trends show a great deal of opportunity for FeRAM as a buffer memory (>32Mb) in flash SSDs. The speed performance of FeRAM implemented SSDs shows 6 times higher and cost is down to one third due to replacing other buffer memory of NOR and other RAM.

Fig. 1 shows the trend of memory requirements in system on a chip (SOC). Embedded memory is increasingly dominating SOC chip area and cost, and is used in all application segments.

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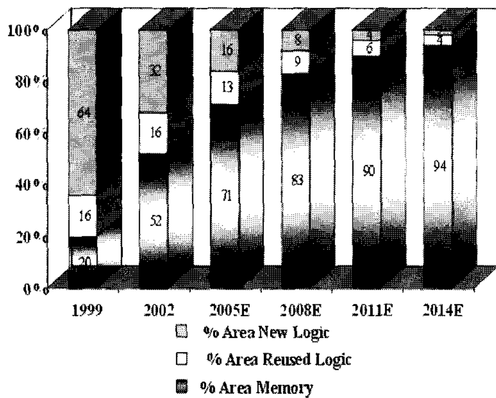

Fig. 1. Embedded memory in SOC.

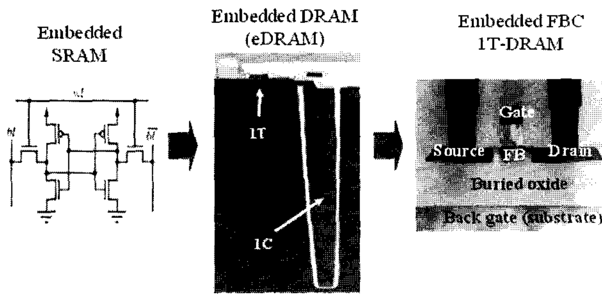

Fig. 2. Embedded memory cell technology trend.

Fig. 2 shows embedded memory cell technology trend. The first generation memory cell type is embedded SRAM (eSRAM) cell, in which 6-tansistor consumes huge area and power, prompting severe soft error rate (SER) problems at 50nm and below, and being useful for small (<64KB) memories only. The second generation memory cell type is 1-transistor and 1-capacitor (1T1C) embedded DRAM (eDRAM) cell, which is 2 – 3 times denser than eSRAM, requires 6-9 extra processing steps, and have the huge manufacturability challenge and barrier to scaling beyond 90nm.

The next generation memory cell candidate is silicon-on-insulator (SOI) wafer based floating body cell (FBC) 1-transistor (1T) embedded DRAM cell, which is 5 times denser than eSRAM, highest density embedded memory, faster than 1T1C eDRAM, soft error rate 10 times better than eSRAM, and uses standard SOI processes with no changes.

Fig. 3 shows the comparison cell structures of FBC 1T-DRAM and 1T-FeRAM.

FBC 1T-DRAM is based on SOI wafer process MOS field effect transistor (FET) type cell, and compared 1T-FeRAM with metal ferroelectric insulator semiconductor

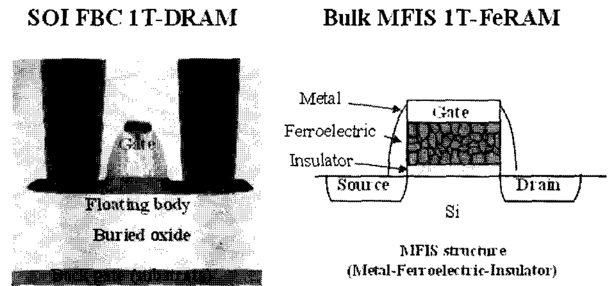

Fig. 3. Cell structures of FBC 1T-DRAM and 1T-FeRAM.

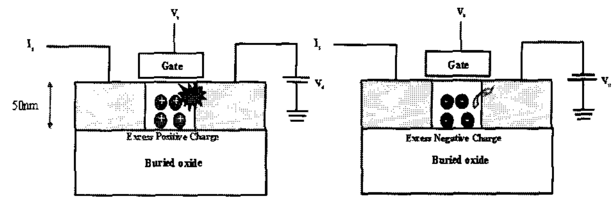

Fig. 4. Write operation of FBC 1T-DRAM.

(MFIS) FET-type cell in bulk silicon or SOI wafer. FBC 1T-DRAM on SOI has been proposed to overcome scaling challenges of 1T1C DRAM for high density memory applications [1]. The most attractive features include a small cell size and the absence of the storage capacitor. FBC 1T-DRAM never necessitates an extra capacitor, which the conventional 1T1C DRAM necessitates. The cell structure is so simple that its cell size is shrinkable. In addition to device geometry, operation voltages should be carefully reduced in the scaling. The floating body stores an information bit in the form of an electric charge as shown in Fig. 4.

The floating body is charged and discharged during data write operations. By setting the word line (WL), bit line (BL) and source line (SL) to specific voltage states, the channel body stores a logic “1” potential as a result of impact ionization and a logic “0” value as a result of forward bias of body to BL. By applying 0V to the BL and by applying a negative voltage to the WL, the floating body potential level is held for a refresh time. The data states can be identified using FBC current modulated by the floating body potential level. The logic “1” stored FBC shows a high level of current and the logic “0” stored FBC shows a low level of current as shown in Fig. 5.

The conventional 1T1C DRAMs show several hundred milli-seconds of retention time in standalone applications as shown in Fig. 6 But the FBC 1T-DRAM is far less to level of retention time of the conventional

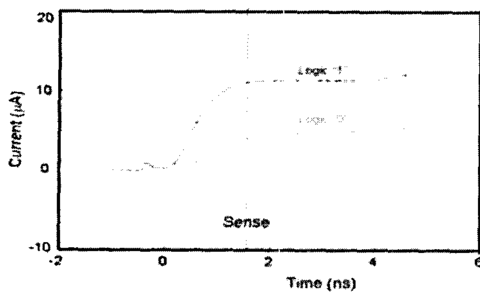

Fig. 5. Cell sensing current of FBC 1T-DRAM.

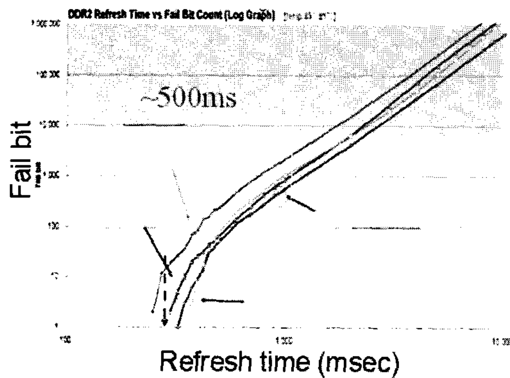

Fig. 6. Refresh property of 1T1C DRAM.

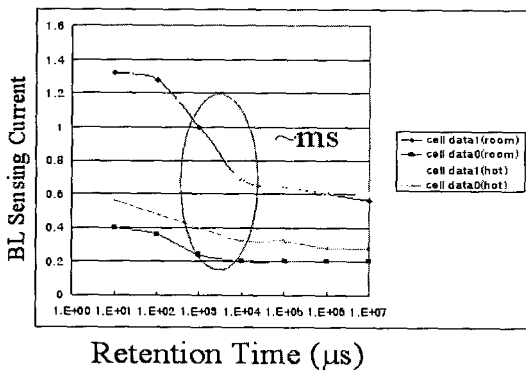

Fig. 7. Retention property of FBC 1T-DRAM.

1T1C DRAM as shown in Fig. 7 Retention time level of FBC 1T-DRAM is around several milli-seconds time. One of the most urgent issues of FBC 1T-DRAM technologies is to increase the retention time to the level of 1T1C DRAM.

II. Nonvolatile Refresh Adopted Scheme of 1T-FeRAM

Since 1T-FeRAM consists of only one ferroelectric gate field effect transistor (FET) [2], the area required for one bit memory cell is extremely small. It therefore

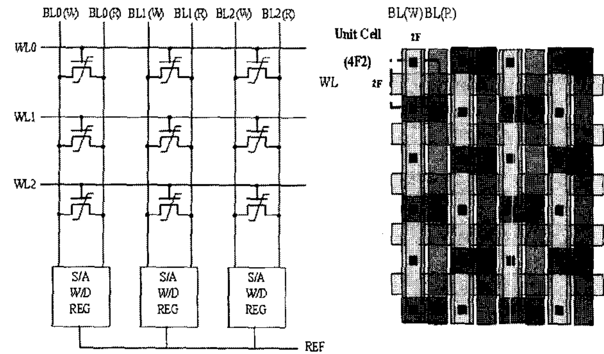

Fig. 8. Cell array and layout of 1T-FeRAM.

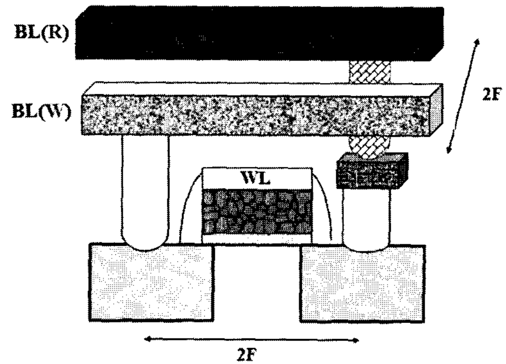

Fig. 9. Unit cell structure of 1T-FeRAM.

holds great promise of serving as an ultra giga-bit FeRAM with a cell size of 4F2 as shown in Fig. 8 Each cell is composed of a WL and two BLs (write BL BLn(W) and read BL BLn(R)). Cell data is written and refreshed by the polarization bias between the WL and BLs.

The write BL of BL(W) and read BL of BL(R) are composed of different levels of metal layers as shown in Fig. 9 The BL(W) is formed directly on the contact plug, and the BL(R) is formed on the oxide field region through the interconnection pad layer and two contact plugs. Thus, the unit cell size is theoretically 4F2 from feature sizes of 2F (row) x 2F (column).

The operational timing diagram of refresh cycle of 1T-FeRAM is composed of time period of t1 for cell data read operation and time periods of t2 and t3 for rewriting operation as shown in Fig. 10 In time period t1, WL voltage is Vread of 2/3Vc, and read BL of BL(R) is biased to sensing voltage of Vsen (Vsense) to detect cell sensing current, and write BL of BL(W) is biased to ground voltage. The sensed and amplified data in t1 is registered by the sense amplifier for rewriting or restoring operation. In time periods of t2 and t3, the rewriting data '0' and '1' are written, respectively. In the

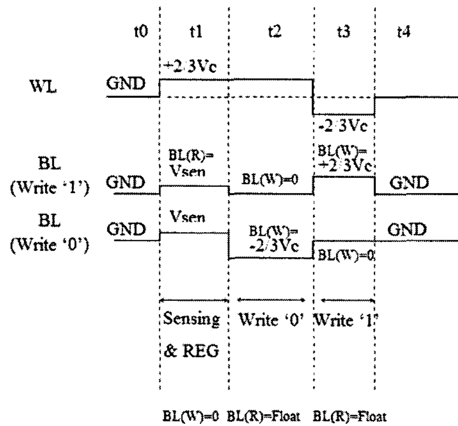

Fig. 10. Operational timing diagram of refresh cycle.

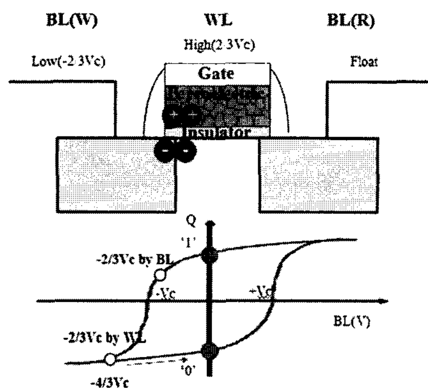

Fig. 11. Negative polarization voltage condition of write '0'.

rewriting periods, the rewriting data is provided to the write BL of BL(W), and the read BL of BL(R) is on float state. For write '0' and '1' in t2 and t3, the absolute write voltage between WL and BL(W) should be higher than the coercive voltage Vc of ferroelectric film, and the needed write time for polarization switching of ferroelectric film is less than 1.0 ns. For writing data '0', BL(W) to WL write voltage condition is -4/3Vc, and for writing data '1', BL(W) to WL write voltage condition is +4/3Vc. By the way, in normal read mode, the read cycle is only composed of the time period of t1 due to non-destructive readout operation without restoring period. In normal write mode, the write cycle is composed of the time periods of t2 and t3.

Negative polarization voltage condition of write '0' in t2 is shown in Fig. 11 BL(W) voltage is -2/3Vc and WL voltage is 2/3Vc, thus the ferroelectric film polarization bias of selected cell is -4/3Vc.

Positive polarization voltage condition of write '1' in t3 is shown in Fig. 12 BL(W) voltage is 2/3Vc and WL voltage is -2/3Vc, thus the ferroelectric film polarization

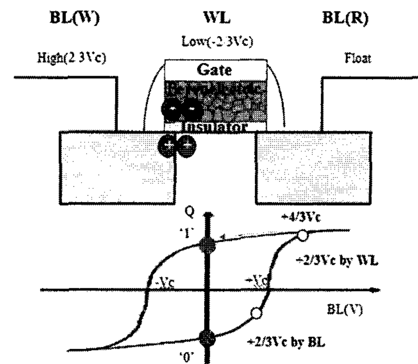

Fig. 12. Positive polarization voltage condition of write '1'.

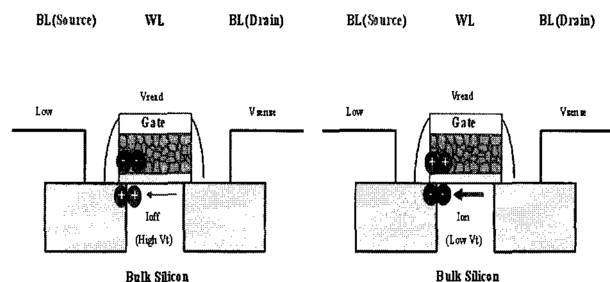

Fig. 13. Cell read operation of 1T-FeRAM.

bias of selected cell is 4/3Vc. The unselected cells are biased only 2/3Vc, thus no write disturbance is occurred to the unselected cells.

When the ferroelectric thin film on insulator at the gate portion causes polarization, electric charges are induced in the channel region of the MFISFET as shown in Fig. 13 When positive polarization is present at the channel region side, electrons are induced in the channel region. The induced electrons form a channel or at least lower the threshold voltage of the MFISFET. Moreover, when negative polarization is present at the channel side, it raises the threshold voltage of the MFISFET. The read current flowing through the saturated region is actually decided by a region in which a channel is formed by inducing electric charges at the source side and it is known that the read current is hardly influenced by the state of the depletion layer side at the drain side. Therefore, the polarization state of the ferroelectric thin film at the source side influences the threshold voltage to control the magnitude of the flowing current value in read mode.

Sensing block circuit is composed of sense amplifier (S/A), write driver (W/D) and temporary data storage cache of register. The register is used for refreshing operation and writing operation. For the refresh operation,

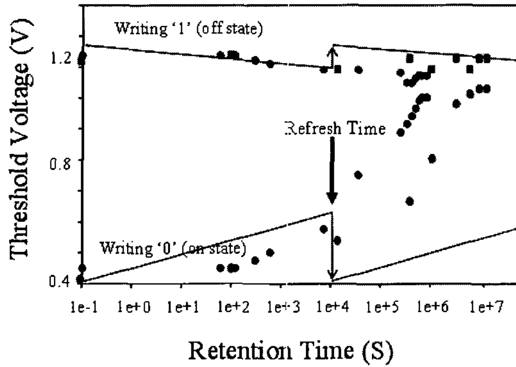

Fig. 14. Nonvolatile refresh concept of 1T-FeRAM.

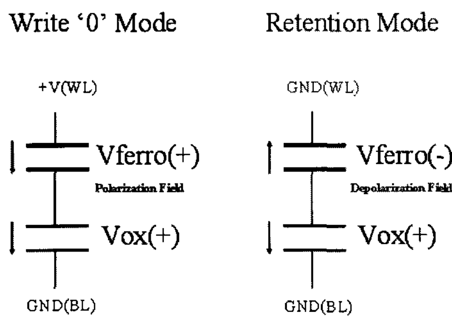

Fig. 15. Depolarization field degradation of MFIS 1T-FeRAM.

in first time step, the cell data are sensed and registered to the register. In second time step, logic "0" data are restored and in third time step, logic "1" data are restored.

However, the problem of 1T-FeRAM as a nonvolatile memory of 10-years retention expectation is that the data retention time is short of several days. But compared to 1T1C DRAM or 1T-DRAM, the current retention time of 1T-FeRAM is already much sufficient for refresh scheme adopted memory application such as DRAM. It adopts a nonvolatile refresh concept for DRAM-like memory application as shown in Fig. 14.

The metal ferroelectric metal insulator semiconductor (MFMIS) FET or metal ferroelectric insulator semiconductor (MFIS) FET type cell have inherent problems of short retention time from the reverse depolarization bias effect as shown in Fig. 15, which is from the cell structure itself of insulator buffer layer and would be very difficult to overcome the fundamental issue in near future, thus should find another alternative solution and application.

In this paper, we propose a new refresh adopted architecture for 1T-FeRAM, which adopts the refresh scheme similar to DRAM as shown in Fig. 16.

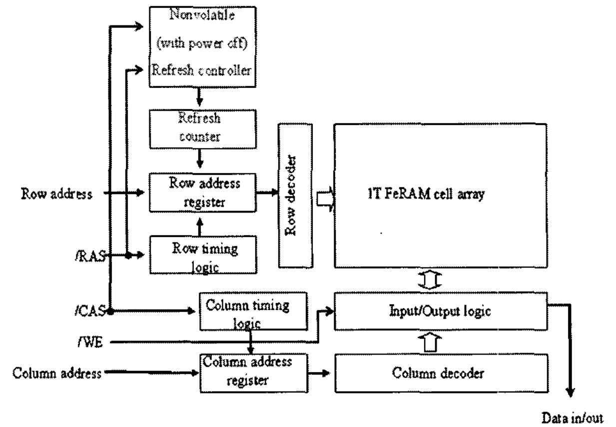

Fig. 16. Chip block architecture of MFIS 1T-FeRAM.

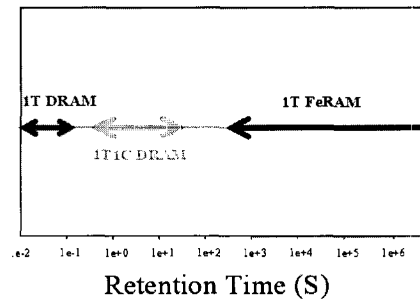

Fig. 17. Retention time comparison.

In the conventional DRAM, the data and refresh operation is only valid in the power-on state, but in the 1T-FeRAM, the data retention and refresh operation are valid in both the power-on state and also after the power-off and on, if the retention time of 1T-FeRAM cell is longer than the interval of power-off and on. By this way, the conventional refresh operation concept would be shifted from power-on period refresh to power-off period refresh. The standby current of the 1T-FeRAM can be almost same to the level of nonvolatile 1T1C FeRAM, but cell size can be compete to 1T-DRAM cell. The comparing retention properties among 1T1C DRAM, 1T-DRAM, and 1T-FeRAM are shown in Fig. 17.

The comparison table of key operations between floating body 1T-DRAM and 1T-FeRAM is shown in Table 1.

When reading operation, the data of FBC 1T-DRAM is degraded partially by the WL and BL disturbance from leakage current source, thus the reading operation of FBC 1T-DRAM is partially destructive read out (DRO) mode. But reading operation of 1T-FeRAM is stable under the coercive voltage bias condition so that the non-destructive read out (NDRO) operation is

Table 1. Comparison table.

Floating body 1T-DRAM	1T-FeRAM
Partially DRO	NDRO
Short refresh cycle=~100ms	Long refresh cycle=~Days
Refresh during power-on	Refresh during power-on or after power-off
Obeying the scaling rule	Obeying the scaling rule
High Density	High Density
High speed current sensing	High speed current sensing
Sensitive to CMOS process	No-Sensitive to CMOS process

guaranteed. The refresh time of FBC 1T-DRAM is the range of several milli-seconds compared to several days of 1T-FeRAM. Refresh scheme is only valid in power-on state in FBC 1T-DRAM, but in 1T-FeRAM, during standby mode the memory power can be completely shut off or deep power down (DPD) mode without the stored data failure. Because the cell structure is based on 1T-FET in both FBC 1T-DRAM and 1T-FeRAM, the shrinking down of cell size gets advantage until next generation technologies. Thus high density memories over giga-bit or tera-bit are possible. The both cell is operated by the current base, the high speed current sensing scheme is possible. The FBC 1T-DRAM is sensitive to leakage source from CMOS device and operation. 1T-FeRAM is sensitive to the ferroelectric properties but not CMOS leakage source properties.

III. CONCLUSIONS

The proposed nonvolatile refresh scheme adopted 1T-FeRAM circumvents the inherent retention degradation problems of 1T-FET type cells. The present retention property of 1T-FeRAM is already superior to that of FBC 1T-DRAM or 1T1C DRAM. 1T-FeRAM cell properties evaluation is needed in a small cell size of less 50nm feature size. The proposed refresh scheme adopted architecture of 1T-FeRAM is the most promising future technology for the alternative giga-bit DRAM applications.

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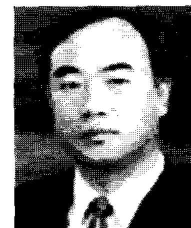
His current interests are to develop DRAM related researches such as 1T-FeRAM for the alternative next generation capacitor-less 1T-DRAM, FeRAM embedded system on a chip (SOC) and RFID tag, and next generation nonvolatile memories.



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