A Novel Boost PFC Converter Employing ZVS Based Compound Active Clamping Technique with EMI Filter

P. Ram Mohan*, M. Vijaya Kumar, and O.V. Raghava Reddy*****

Abstract—**A Boost Power Factor Correction (PFC) Converter employing Zero Voltage Switching (ZVS) based Compound Active Clamping (CAC) technique is presented in this paper. An Electro Magnetic Interference (EMI) Filer is connected at the line side of the proposed converter to suppress Electro Magnetic Interference. The proposed converter can effectively reduce the losses caused by diode reverse recovery. Both the main switch and the auxiliary switch can achieve soft switching i.e. ZVS under certain condition. The parasitic oscillation caused by the parasitic capacitance of the boost diode is eliminated. The voltage on the main switch, the auxiliary switch and the boost diode are clamped.**

The principle of operation, design and simulation results are presented here. A prototype of the proposed converter is built and tested for low input voltage i.e. 15V AC supply and the experimental results are obtained. The power factor at the line side of the converter and the converter efficiency are improved using the proposed technique.

Index Terms—**Boost converter, power factor correction, zero voltage switching, compound active clamping, electro magnetic interference**

I. INTRODUCTION

In the boost PFC converters, hard switching of the switching device results in reverse recovery losses and Electro Magnetic Interference problems. In recent years, many soft switching techniques have come forth to reduce the adverse effects of reverse recovery characteristics of boost PFC converters [1-4].

Active Clamping technique has been an attractive choice due to achieving ZVS for both the main switch and the auxiliary switch [5-7]. However, when the main switch is on, there exists a parasitic resonance between the resonant inductor and the junction capacitance of the boost diode, leading to a high voltage stress on the boost diode. To eliminate the parasitic ringing, a diode is introduced to clamp the voltage on the boost diode at the value of the output voltage [8].

Electro Magnetic Interference problem arises due to the sudden changes in voltage (dv/dt) or current (di/dt) levels in a waveform. In diode rectifier, the line current can be pulse of short duration and the diode recovery current pulse can generate transient voltage spikes in the line inductance. A conductor carrying dv/dt wave acts like an antenna and sensitive signal circuit and appear as noise. The EMI problems create communication line interference with sensitive signal electronic circuits. [9, 10]

In this paper, a novel Boost PFC Converter is proposed employing ZVS based CAC technique with EMI Filter.

II. TOPOLOGY OF PROPOSED CONVERTER

In the converter circuit, the active clamping branch composed of a clamping capacitor and an active switch is placed in parallel with resonant inductor. Also, the main switch, the auxiliary switch, the clamping capacitor, the boost diode and the output capacitor form a voltage loop.

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* Assistant Professor, G. Pulla Reddy Engg. College, Kurnool, Andhra Pradesh, India
** Professor, JNTU College of Engg., Anantapur, Andhra Pradesh, India
*** Scientist, ISRO Satellite Center, Bangalore, India
E-mail : rammohan_cdp@yahoo.co.in

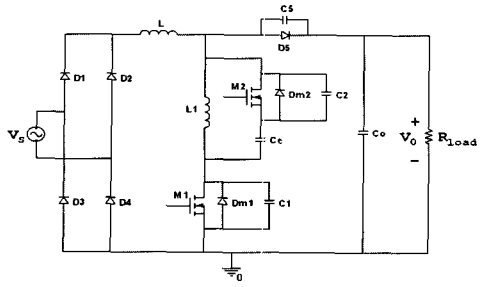

Fig. 1. Boost PFC Converter with ZVS based CAC technique

The concept is that except the switching periods, at any time during operation there are two switching devices conducting among the main switch, the auxiliary switch and the diode, so that the voltage across the switching device that is off is clamped. The auxiliary switch is always turned on under zero voltage condition while the main switch can achieve zero voltage switching under certain condition. The topology of the proposed converter is shown in Fig.1.

The converter circuit with proposed technique comprises of two sections. The diode bride rectifier (D_1, D_2, D_3 and D_4), input filter inductor L, main switch M_1, boost diode D_5, output filter capacitor C_0 and the load forms the boost converter section.

The resonant inductor L_1, auxiliary switch M_2, clamping capacitor C_C forms the auxiliary circuit section. The parasitic capacitances of the two switches are C_1 and C_2. The parasitic capacitance of boost diode is C_5. The body diodes of the two switches are D_{m1} and D_{m2}.

To analyze the principle of operation of the proposed converter, the following assumptions are to be made.

1. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is considered as an ideal switch with its body diode.
2. The capacitances C_1 and C_2 paralleled with switches M_1 and M_2 respectively include parasitic capacitance and external capacitance. The capacitance C_5 paralleled with the boost diode D_5 also includes parasitic capacitance and external capacitance.
3. The input filter inductor L is very large that the current hardly change and can be considered as a constant current source in one switching cycle.
4. The output filter capacitor C_0 is represented by a constant voltage source.
5. The value of clamping capacitor C_C is large enough so that the voltage ripple across it is small, thus can be seen as a voltage source.
6. The resonant frequency of the capacitance C_C and resonant inductance L_1 is much lower than the operation frequency of the converter. Here only one switching cycle in the positive part of power line input is explained.

III. Modes of Operation

1. Mode 1 (t0-t1)

Before t_0, the boost diode D_5 is conducting and auxiliary switch M_2 is in off state. After that the current in L_1 charges the parasitic capacitance C_2 paralleled with M_2 and discharges the parasitic capacitance C_1 paralleled with M_1.

At t_0, the voltage across M1 decreases to zero and body diode of M_1 i.e. D_{m1} starts to Conduct. Then, M_1 is turned on under zero voltage condition. The voltage across M_2 is clamped to (V_0+V_{Cc}). During this mode, current in D_5 is decreasing, while current in M_1 is increasing at same rate with D_5.

This operation is shown in fig.2. The current changing rate is determined by L_1. The current in L_1 increases at the rate of

$$\frac{di_{L_1}}{dt} = \frac{V_0}{L_1} \tag{1}$$

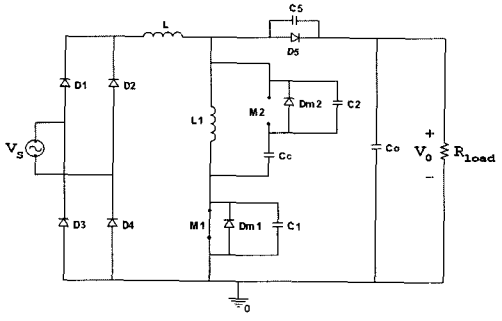

Fig. 2. Mode 1

2. Mode 2 (t1-t2)

At t_1, the current in D_5 decreases to zero, resonance between the inductance L_1, the capacitance C_5 paralleled with D_5 and the capacitance C_2 paralleled with M_2 begins. At end of this mode, voltage across D_5 reaches the value V_0+V_{Cc} and voltage across M_2 is zero. Thus, M_2 can be turned on under zero voltage condition. At t_2, all the

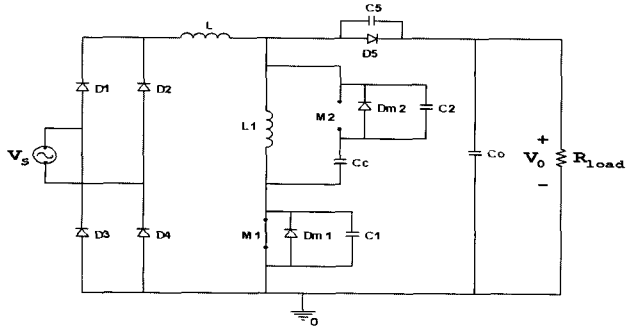

Fig. 3. Mode 2

current in the inductor L flows through M_1. This operation is shown in fig.3.

3. Mode 3 (t2-t3)

The body diode of M_2 i.e. D_{m2} begins to conduct at t_2 and the resonance of L_1, C_5 and C_2 terminates. M_2 is turned on with zero voltage condition. This operation is shown in fig.4. In this mode, the slope of the current in L_1 is

$$\frac{di_{L_1}}{dt} = -\frac{V_{C_C}}{L_1} \tag{2}$$

In this mode, the current in L increases at the rate of

$$\frac{di_L}{dt} = \frac{V_S + V_{C_C}}{L} \tag{3}$$

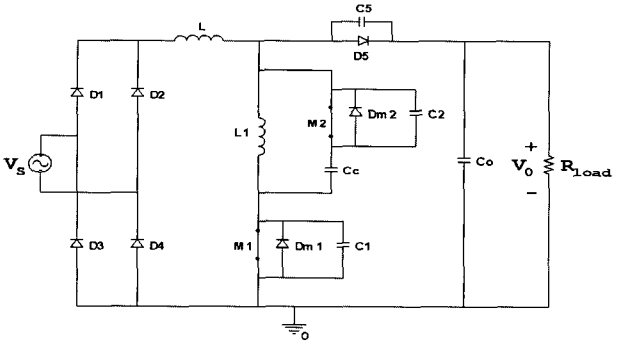

Fig. 4. Mode 3

4. Mode 4 (t3-t4)

At t_3, M_1 is turned off with ZVS because of the existence of C_1. In this mode, the capacitance C_5 is discharged by the current in L until the voltage across D_5 reaches to zero at t_4. This operation is shown in fig.5.

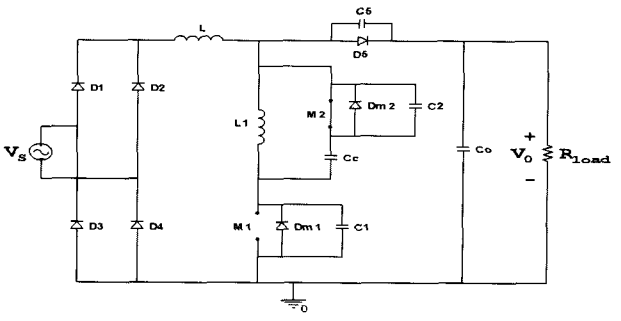

Fig. 5. Mode 4

5. Mode 5 (t4-t5)

At t_4, D_5 starts to conduct. The energy stored in the inductor L is transferred to the load of the converter. In this mode, the voltage across M_1 is clamped to (V_0 + V_{Cc}). This operation is shown in fig.6.

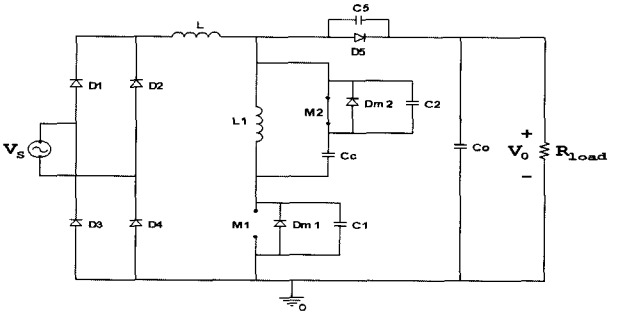

Fig. 6. Mode 5

6. Mode 6 (t5-t6)

At t_5, the boost diode D_5 is conducting, the switch M_2 is turned off. At this time, current through resonant inductor L_1 is negative and it will discharge the parasitic capacitance C_1. At t_6, the voltage of M_1 can decrease to zero and the body diode of M_1 i.e. D_{m1} will start to conduct. Then, M_1 can be turned on under ZVS. This operation is shown in fig.7. After t_6, next switching cycle starts again.

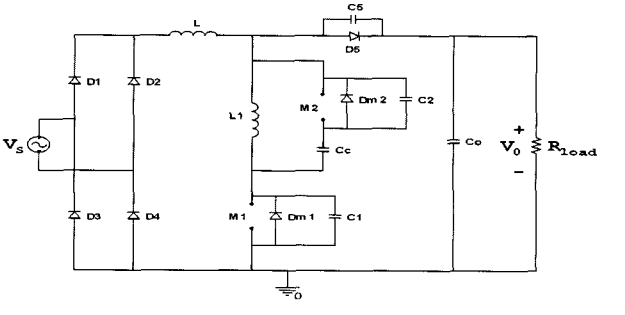

Fig. 7. Mode 6

IV. DESIGN

The design specifications of the proposed converter with EMI Filter are

AC input Voltage = V_S = 230 V

DC output Voltage = V_0 = 400 V

Output Power = P_{out} = 500 W

Switching Frequency = F_s = 100 KHz

Efficiency = η = 95%

The maximum input current is

$$I_{peak} = \frac{2*P_{in}}{\sqrt{2}*V_S} = \frac{2*(500/0.95)}{\sqrt{2}*230} = 3.24A \quad (4)$$

Both the main switch and auxiliary switch are IRFP460 which has $V_{DS(max)}$ = 500V and I_D = 20A.

The selection of resonant inductor L_1 is determined by the need to suppress the diode reverse recovery current. Usually the current change should be lower than 100A/μs. According to equation (1), the resonant inductor L_1 is calculated and it is 8μH.

The selection of the capacitor C_5 which is parallel with diode D_5 should consider ensuring a wide ZVS operation range. The capacitances C_1 and C_2 are chosen as 1nF, and then the value of C_5 should be a little larger than C_1. Hence, 4nF is selected.

The selection of the clamping capacitor C_C should ensure that the resonant frequency of C_C and L_1 is much lower than the operating frequency of the main switch. i.e.

$$\frac{1}{2\pi\sqrt{L_1 * C_C}} <<< 100 \text{ KHz} \quad (5)$$

So, a capacitor of 4.7μF is selected.

The components used are L=1mH; C_0=880μF; L_1=8μH; C_1=1nF; C_2=1nF; C_5=4nF; C_C=4.7μF.

V. ELECTRO MAGNETIC INTERFERENCE (EMI) FILTER

The Electro Magnetic Interference can be transmitted in two forms: radiation and conduction. The switching converters supplied by the power lines generate conducted noise into the power lines that is usually several orders of magnitude higher than the radiated noise into free space. Metal cabinets used for housing power converters reduce the radiated component of the electromagnetic interference. Conducted noise consists of two categories commonly known as the differential mode and the common mode.

The differential mode noise is a current or a voltage measured between the lines of the source that is line-to-line voltage. The common mode noise is a voltage or a current measured between the power lines and ground that is line-to-ground voltage. An EMI filter is needed to reduce the differential mode and common mode noises. The EMI Filter for Boost PFC converter is shown in fig.8.

For CM Noise,

$$f_{R,CM} = 1/(2\pi\sqrt{(2Cy*L_{CM})}) \quad (6)$$

$$L_{leakage} = 0.5\% \text{ to } 2\% \text{ of } L_{CM} \quad (7)$$

For DM Noise,

$$f_{R,DM} = 1/(2\pi\sqrt{(2L_DC_X)}) \quad (8)$$

$$L_{DM} = (L_D - L_{leakage}) / 2 \quad (9)$$

The PFC converter has the predicted noise level and EMI which includes total noise, common mode and differential mode noises. In general, the corner frequencies of EMI noises in the PFC circuits are 28 KHz for CM noise and20.5 KHz for DM noise. The designed values are L_{CM} is 4.9mH and L_{DM} is 40μH.

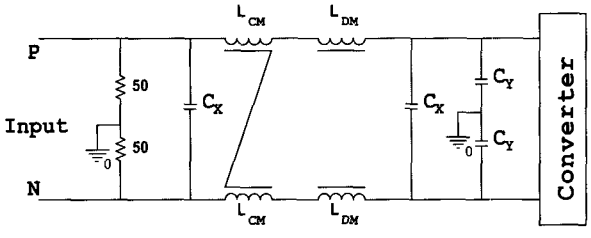

Fig. 8. EMI Filter for proposed converter

VI. RESULTS

1. Simulation Results

The proposed converter along with EMI Filter is simulated using the software ORCAD – PSPICE 9.2.

Fig.9 shows the gate pulses of the main switch M_1 and the auxiliary switch M_2. Fig.10 shows the drain current and drain to source voltage waveforms of M_1 and fig.11 shows the drain current and drain to source voltage

waveforms of M_2. From these two figures, it is clear that both the main switch M_1 and the auxiliary switch M_2 are turned on with Zero Voltage Switching.

The current and voltage waveforms of boost diode D_5 are given in fig.12. From this figure, it is clear that there are no voltage oscillations on the boost diode D_5. The current waveform through the resonant inductor is given fig.13. The output voltage waveform across the load is given in fig.14. The input current and input voltage waveforms are given in fig.15.

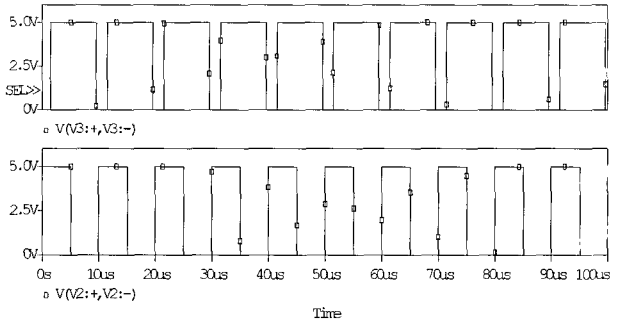

Fig. 9. Gate pulses for switches M_1 and M_2

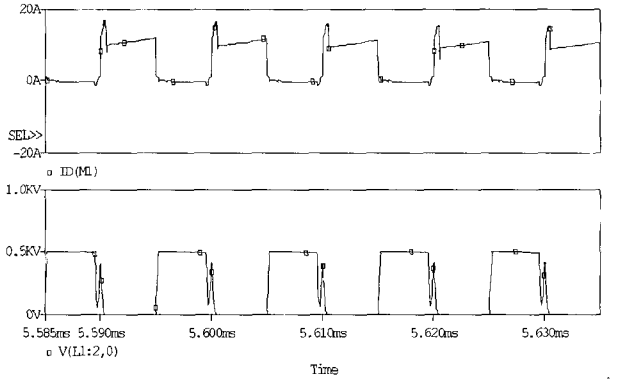

Fig. 10. Drain current and drain to source voltage waveforms of switch M_1

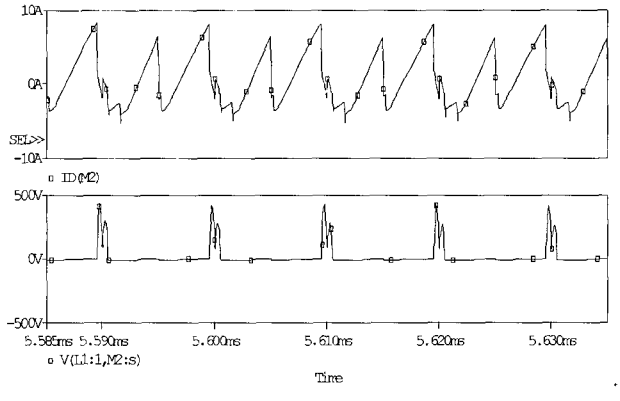

Fig. 11. Drain current and drain to source voltage waveforms of switch M_2

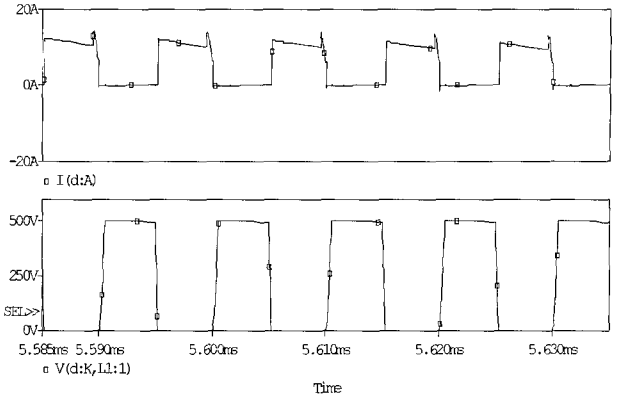

Fig. 12. Current and voltage waveforms of boost diode D_5

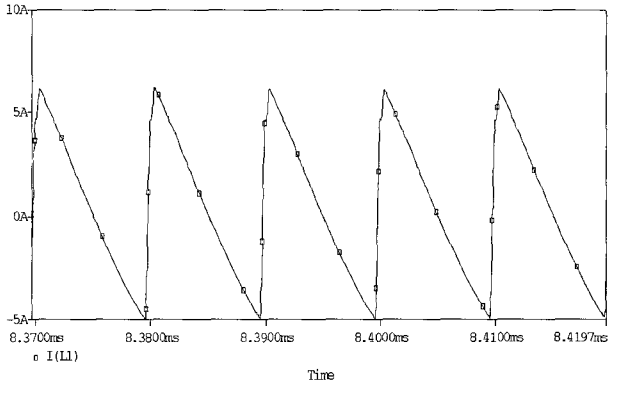

Fig. 13. Current waveform through inductor L_1

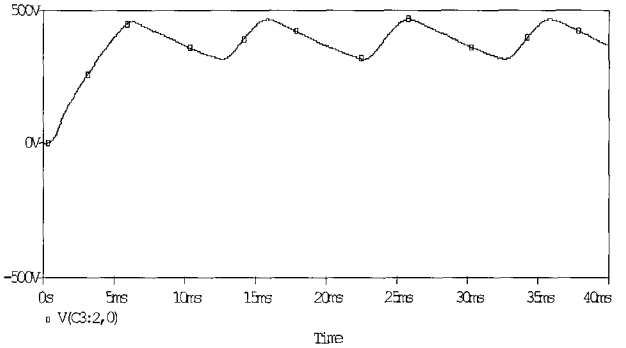

Fig. 14. Output voltage waveform across the load

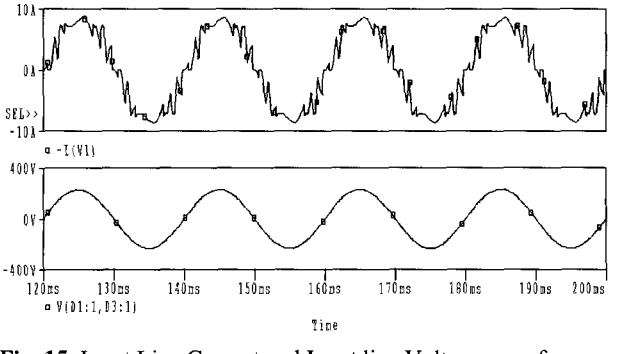

Fig. 15. Input Line Current and Input line Voltage waveforms

2. Experimental Results

A prototype of proposed converter is built for low AC input i.e. 15V supply. The designed components with low ratings are connected in the circuit.

The hardware circuit of proposed converter is shown in fig.16. The control pulses are generated using the micro controller 89C2051. These pulses are amplified to using the driver IC IR2110. The outputs of this chip are applied to the gate terminals of the MOSFETs.

The gate pulses for switch M_1 is shown in fig.17. The gate pulses for switch M_2 is shown in fig.18. The output voltage waveform is shown in fig.19. The input line voltage and line current waveforms are shown in fig.20.

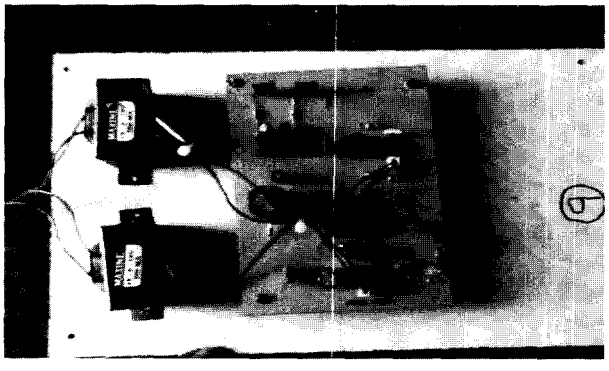

Fig. 16. Hardware circuit of proposed converter

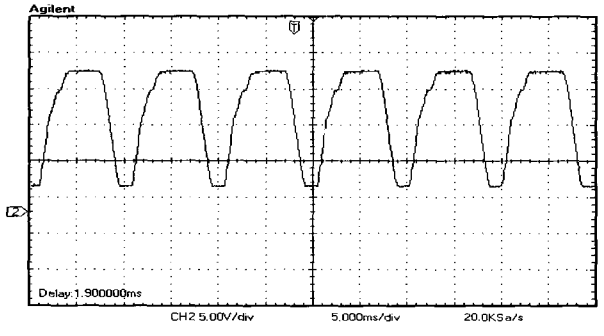

Fig. 17. Gate pulses for switch M_1

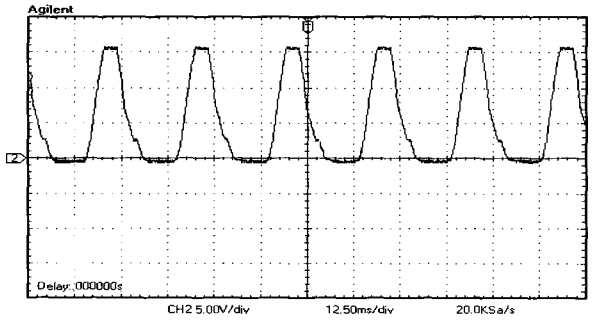

Fig. 18. Gate pulses for switch M_2

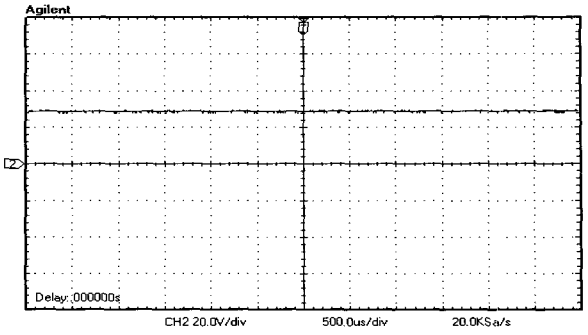

Fig. 19. Output voltage waveform

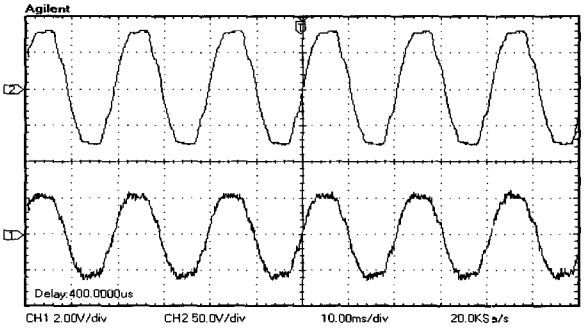

Fig. 20. Input line voltage and current waveforms

The Simulation and Experimental results show that the power factor of the AC supply using the proposed converter is improved to around 0.95 and the efficiency of the converter is around 95%.

VII. Conclusions

The Boost PFC converter employing ZVS based Compound Active Clamping technique with EMI Filter is presented in this paper. This topology solves the problem of diode reverse recovery; meanwhile create soft switching condition for both main switch and the auxiliary switch. The parasitic oscillation on the boost diode caused by the resonant inductor and the parasitic capacitance of the diode is eliminated. The simulation and experimental results show that the power factor at the line side of the converter and the converter efficiency are improved using the proposed technique.

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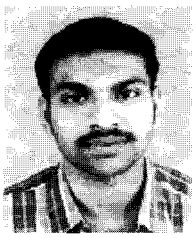
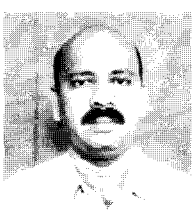
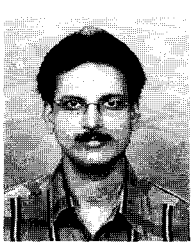


P. Ram Mohan received the B.E. degree in Electrical Engineering from Bangalore University, India in 1999 and M.Tech. degree in Power Electronics from Visvesvaraiah Technological University, India in 2002. Currently he is pursuing his Ph.D. degree under Jawaharlal Nehru Technological University, Andhra Pradesh, INDIA. Since 2002, he has been an Assistant Professor at G. Pulla Reddy Engineering College, Kurnool, Andhra Pradesh, INDIA. His research interests are Switching Mode Power Supplies, Power Converters, High Power Factor Rectifier and Electro Magnetic Interference in converters.



M. Vijaya Kumar graduated from NBKR Institute of Science and Technology, Vidyanagar, A.P, India in 1988. He obtained M.Tech degree from Regional Engineering College, Warangal, India in 1990. He received Doctoral degree from JNT University, Hyderabad, India in 2000.

Currently he is working as Professor and head of Electrical and Electronics Engineering Department, JNT University, Anantapur, A.P, India. He is a member of Board of studies of S.V. University, Tirupathi and JNT University, Hyderabad, India. He has published over 40 research papers. He received two research awards from the Institution of Engineers (India). His areas of interests include Power Electronics, Electrical Drives, Microprocessors and Instrumentation.



O.V. Raghava Reddy received the B.Tech., M.Tech.. degrees in Electrical Engineering from National Institute of Technology, Warangal, Andhra Pradesh, India. Since 1990, he has been a Scientist at ISRO Satellite Center, Bangalore, India. His Research interests are Power Electronics, Drives, EMI and High Power Factor Rectifiers.