Two-Bit/Cell NFGM Devices for High-Density NOR Flash Memory

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Abstract—**The structure of 2-bit/cell flash memory device was characterized for sub-50 nm non-volatile memory (NVM) technology. The memory cell has spacer-type storage nodes on both sidewalls in a recessed channel region, and is erased (or programmed) by using band-to-band tunneling hot-hole injection (or channel hot-electron injection). It was shown that counter channel doping near the bottom of the recessed channel is very important and can improve the V_{th} margin for 2-bit/cell operation by ~2.5 times. By controlling doping profiles of the channel doping and the counter channel doping in the recessed channel region, we could obtain the V_{th} margin more than ~1.5 V. For a bit-programmed cell, reasonable bit-erasing characteristics were shown with the bias and stress pulse time condition for 2-bit/cell operation. The length effect of the spacer-type storage node is also characterized. Device which has the charge storage length of 40 nm shown better ΔV_{th} and V_{th} margin for 2-bit/cell than those of the device with the length of 84 nm at a fixed recess depth of 100 nm. It was shown that peak of trapped charge density was observed near ~10 nm below the source/drain junction.**

Index Terms—**2-bit/cell, Recessed channel, nano-dot, channel hot electron, V_{th} margin**

I. INTRODUCTION

Flash memory has become a cost-effective solid-state storage technology widely used in mobile electronics devices and other consumer applications. The NOR flash memory has typically been used for code storage and direct execution in portable electronics devices, such as cellular phones and PDAs. Since there is no roadmap for nano-flaoting gate memory (NFGM) NOR application, we follow the roadmap for SONOS. According to the projection of the latest updated version 2006 ITRS, the SONOS NVM device for 2-bit/cell cannot be scaled down to the physical gate length below 140 nm due to the charge separation issue in the nitride layer [1]. Especially, the 2-bit/cell SONOS type NVM memories are faced serious problems for ultra high density and reliability application when the gate length (L_g) comes into the sub-90 nm regime [2]-[4]. To shrink the L_g down to sub-100 nm and remove charge redistribution in the storage layer, localized charge trapping method by using spacers formed [2]-[6] on both sides of the control gate was adopted in planar channel flash memory devices to achieve 2-bit/cell operation [4]-[9]. However, those structures have large drain-induced-barrier-lowering (DIBL (poor scalability)) and probably have a big non-uniformity in controlling the dimension of the control gate and the spacers for the localized charge storage in sub-50 nm regime. Thus Two-bit/cell operation has been attractive to increase storage capacity of a flash memory. However, it is very difficult to achieve large threshold voltage (V_{th}) margin for 2-bit/cell in conventional devices.

As the L_g scales down to 50 nm or less, low frequency noise (LFN) in NOR cell devices is becoming serious problem, since the 1/f noise power density of the drain is proportional to $1/L^3$ [10], and the current fluctuation of the drain is inversely proportional to L^2 [11]. Especially, random telegraph noise (RTN) makes the drain current

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fluctuate and finally gives some errors in reading the drain current [12]. The best way to suppress the LFN is to increase L_g, which degrades memory density. Increasing L_g also gives less V_{th} fluctuation due to dot size and density non-uniformity [13].

Compared to atomic-size nitride traps, electron or hole energy states are energetically deeper in the nanocrystal wells. For instance, the energy level of traps is typically 1-2 eV below the Si_3N_4 conduction band, while the electron ground state in nanocrystals could exceed 3 eV below the SiO_2 conduction band [14]. Hence, if the nanocrystals are well separated in the 2-D layer, then conduction between the nodes is totally prevented in NFGM cells.

In this review paper, we briefly introduce a new NFGM cell transistor for high-density NOR flash memory. Since the device has basically recessed channel structure, effective channel length is very long without increasing 2-D cell area. Therefore we can solve the problem regarding the LFN and suppress V_{th} non-uniformity due to non-uniformity of nano-dots size and density. We can also achieve 2-bit/cell SONOS flash memory by adopting spacer-type charge storage layer inside recessed channel region. We investigate the programming and erasing characteristics of the proposed cell with an L_g of 40 nm by changing counter channel doping and channel doping profiles using device simulator [15]. The bottom corner of the recessed region affects negatively V_{th} margin for 2-bit/cell operation. Thus it is required to check the length effect of the spacer-type storage sidewall formed vertically on the side surface of the recessed region on the V_{th} margin for 2-bit/cell. We investigate mainly programming characteristics with the length by using CHEI (Channel Hot Electron Injection) and injected charges density along vertical storage layer.

II. DEVICE STRUCTURE

Fig. 1 shows that the schematic cross-sectional views of the cell structures cut along channel length direction. The width (x_{rw}) and depth (x_{rd}) of the recessed region are 50 and 100 nm, respectively. The x_j stands for the junction depth from the top of the body and is fixed at 30 nm. We call the recess width as the gate length (L_g), although actual effective channel length (L_{eff}) depends

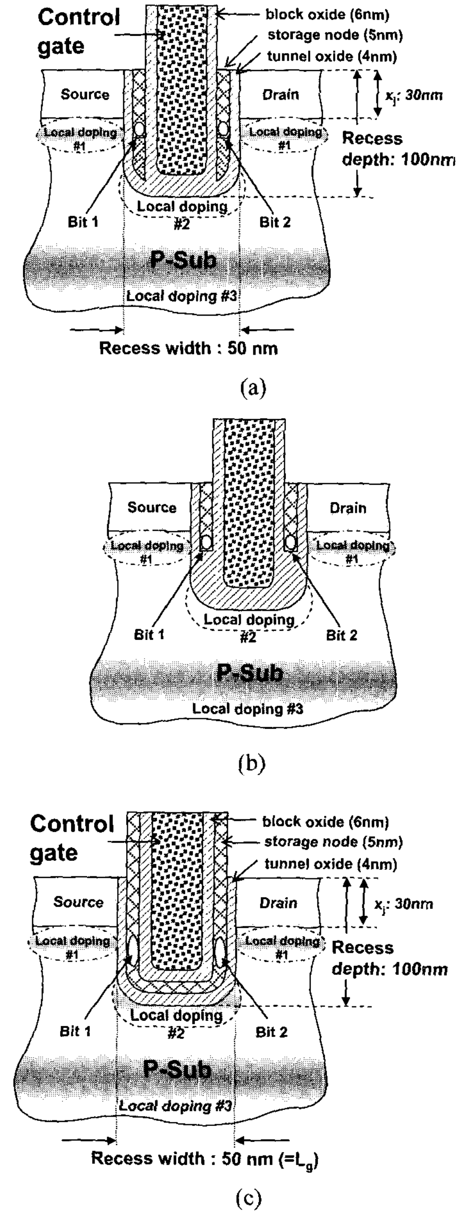


Fig. 1. Schematic cross-sectional views of flash memory cell transistors with different storage node structures. Figures (a) and (b) have spacer-type storage nodes and their vertical lengths are 84 nm and (b) 40 nm, respectively. Figure (c) has continuous-type storage node. Localized #1 channel doping determines hot carrier generation and device V_{th}. The channel length (L_g) represents the open width of the recess region and 50 nm in this work. The #2 local doping is counter-doping to alleviate the bottom corner effect.

on the recess depth and is longer than the recess width. For the given recess width and depth, the L_{eff} is given by approximately $\pi r+2(x_{rd}-x_j-r)$ and is about 170 nm in this work. The physical control gate width is 20 nm for an L_g of 50 nm. The uniform body doping is 1×10^{17} cm^{-3} and

n^+ poly-Si gate is applied. The thicknesses of tunnel and blocking oxides are 4 nm and 6 nm, respectively. The storage layer thickness is 5 nm which accommodates 5 nm diameter nano-dots. We considered mainly three types of localized channel doping for reasonable 2-bit operation. The #1 p-type channel doping [p-type, peak = 2×10^{18} cm^{-3}, and standard deviation (ΔR_p) of 20 nm] is localized nearby metallurgical source/drain (S/D) junction for V_{th} control and hot carrier generation by impact ionization. The #2 n-type channel (counter) doping [n-type, peak = 1.5×10^{18} cm^{-3}, and ΔR_p of 15 nm] is localized near the bottom of the recessed region. The #2 channel doping plays an important role for 2-bit operation. Under the programming or erasing bias condition, most of the hot carriers are trapped into the storage layer near the x_j. Since there is an electric field at the PN junction between the #2 n-type doping region and the p-substrate doping region near the bottom region, small number of carriers can be trapped into the storage node near the bottom of the recess region. Consequently, threshold voltage (V_{th}) can be increased by the trapped charge near the bottom channel region, but the #2 counter channel doping covers the bottom region so that the V_{th} increase near the bottom region of the recessed region can be minimized, which leads to high V_{th} margin for 2-bit operation. The device has #3 localized Gaussian doping profile [p-type, peak = 2×10^{18} cm^{-3}, and ΔR_p of 82 nm] at 350 nm underneath from the top of the body to control body (or well) doping and field isolation V_{th}. Several electrodes with 2 nm length and 1 nm thickness are inserted to the storage node at regular intervals of 1 nm to mimic roughly the nano-dots in the storage layers.

Fig. 1 (a) and (b) show the schematic cross-sectional views of the cell structure with spacer type storage node. The lengths of the storage node formed on the sidewall of the recessed region are 84 and 40 nm, respectively, as shown in figures (a) and (b). The fabrication process of the storage layer is briefly given in the following as an example. In Fig. 1 (a), the storage layer is formed on the tunnel oxide grown in the recessed region, and then spacer type storage nodes are formed by anisotropic dry etching. To form the storage layer in Fig. 1 (b), part of the recess region is formed first to a vertical depth from the top of the body, and then tunnel oxide is followed by the deposition of the storage layer. Short spacer type storage layers are formed on the side surface by anisotropic etching, and further Si etch is performed to a target depth of the recess region. Fig. 1 (c) shows the schematic cross-sectional view of the cell structure with continuous-type storage node.

III. SIMULATION RESULTS AND DISCUSSIONS

In order to achieve localized charge injection, channel hot electron (CHE) injection method is used for programming. Fig. 2 (a) shows log I_D-V_G characteristics before and after programming for the device with the #1 and #3 channel doping profiles. The programming time (t_{PGM}) was fixed at 1 μs for given biases of V_G=4.5 V and V_D=3.5 V. The #1 channel doping is characterized by a Gaussian profile with a peak doping of 3×10^{18} cm^{-3} and an ΔR_p of 20 nm. The V_{th} shift (ΔV_{th}) after programming is about 2.6 V at a V_D of 0.1 V. The V_{th} was defined as the control gate bias when the drain current is 1×10^{-7} A/cell. If we increase the V_D to 1.5 V, the ΔV_{th}

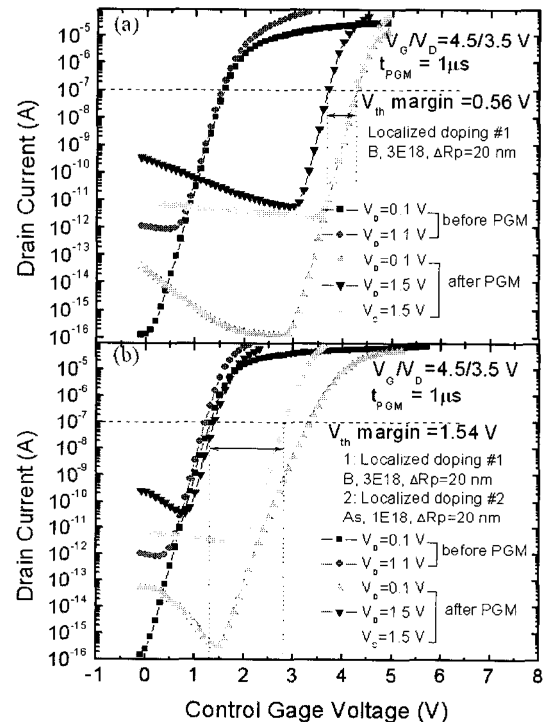


Fig. 2. log I_D-V_G characteristics before and after CHE programming. Figure (a) shows the data with the localized doping profiles of #1 (nearby x_j) and #3. The data for all three local doping profiles are shown in (b). Programming has been done for 1 μs at V_G=4.5 V and V_D=3.5 V. Dotted lines stand for the V_{th} margin for 2-bit/cell operation.

decreases to about 2 V since the inversion electrons move to the source side slightly by which there are few electrons under the programmed region. For a V_D of 1.5 V, it is desirable that the ΔV_{th} becomes nearly 0 V. However, unwanted charge trapping near the bottom region increases the ΔV_{th} at a V_D of 1.5 V. By applying 1.5 V to the source, the ΔV_{th} is again about 2.6 V. The V_{th} margin for 2-bit/cell operation at a given read bias of 1.5 V is about 0.56 V as represented by dotted lines in Fig. 2 (a). Fig. 2 (b) shows log I_D-V_G characteristics under the same situation as Fig. 2 (a). The difference in (b) is a counter-doping near the bottom corner region using n-type impurity that its profile is characterized by a Gaussian profile with a peak doping of 1×10^{18} cm^{-3} and an ΔR_p of 20 nm. Due to the counter-doping, the ΔV_{th} after programming is reduced to about 2 V at a V_{DS} of 0.1 V. Under the programming bias condition, most of the hot electrons are trapped into the storage layer near the x_j and small number of electrons can be trapped into the storage near the bottom of the recess region. The n-type counter-doping alleviates significantly the V_{th} shift with the unwanted charge trapping near the bottom of the recess region. As the result, we can achieve larger V_{th} margin of 1.54 V than that without the counter-doping although the ΔV_{th} is reduced. The I_D-V_G curves in (b) show not only excellent 2-bit/cell operation but also good DIBL characteristics.

Fig. 3 shows V_{th}, ΔV_{th}, and V_{th} margin characteristics versus the ΔR_p of the #1 p-type doping profile when the device has the same n-type counter-doping as that shown in Fig. 2 (b). The V_{th} margin represents the difference between reverse read V_{th} and forward read V_{th}. As a reference, V_{th} margin without #2 doping is represented by open star symbols for comparison. As the ΔR_p of the #1 p-type doping increases, the ΔV_{th} is slightly increased because the program V_{th} is increased with slightly steeper slope than the initial V_{th}. With the ΔR_p increase, the initial V_{th} increases since the p-type doping increases near the bottom corner. The V_{th} margin represented by solid star symbols increases due to the electric filed increase near drain junction when the ΔR_p of #1 doping is increased from 15 nm to 20 nm. Then the V_{th} margin decreases significantly for further increase of ΔR_p because the unwanted charge trap near the bottom corner of the recess region affects channel V_{th} and degrades the

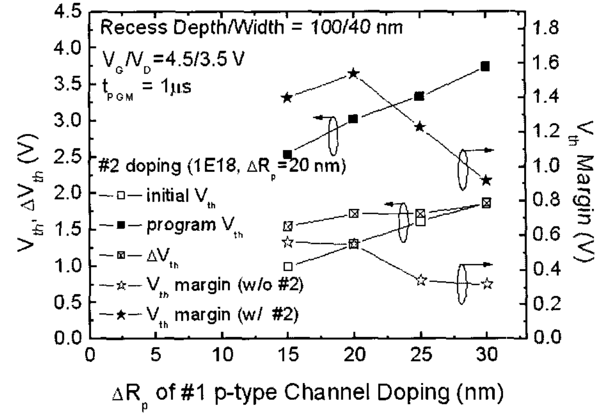


Fig. 3. V_{th}, ΔV_{th}, and V_{th} margin versus the ΔR_p of the #1 p-type channel doping profile. The ΔV_{th} is a V_{th} shift after programming, and the V_{th} margin is a difference between reverse read V_{th} and forward read V_{th}. The star symbols stand for the V_{th} margin. The solid star symbols represent the V_{th} margin with the #2 local doping profile. The V_{th} margin without #2 localized doping profile is represented by open star symbols. The #2 n-type counter doping is located near the bottom of the recess region.

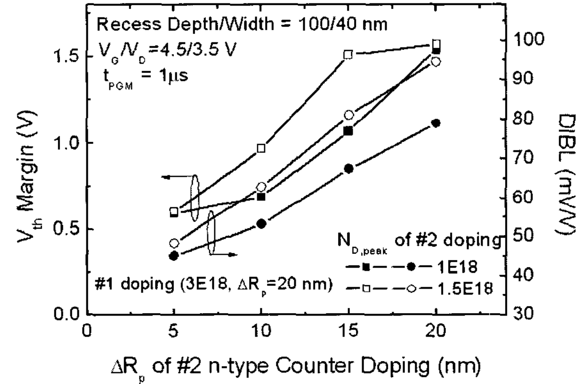


Fig. 4. V_{th} margin and DIBL characteristics versus ΔR_p of the #2 n-type counter-doping profile as a function of a peak concentration (1×10^{18} cm^{-3} and 1.5×10^{18} cm^{-3}). Here the #1 p-type channel doping has a peak value of 3×10^{18} cm^{-3} and an ΔR_p of 20 nm.

V_{th} margin as explained in Fig. 2 (a). The V_{th} margin without the #2 doping (open star symbols) can be explained as the same manner. The V_{th} margin with the n-type counter-doping is about 2.5 times larger than that without the counter doping at an ΔR_p of 20 nm. It is required to keep the ΔR_p of the #1 p-type channel doping small as possible to increase the V_{th} margin.

Fig. 4 shows V_{th} margin and DIBL characteristics versus the ΔR_p of the #2 n-type counter-doping profile

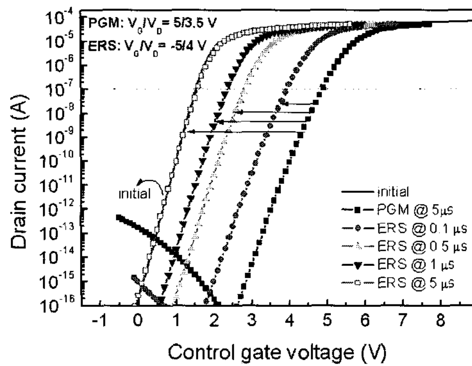
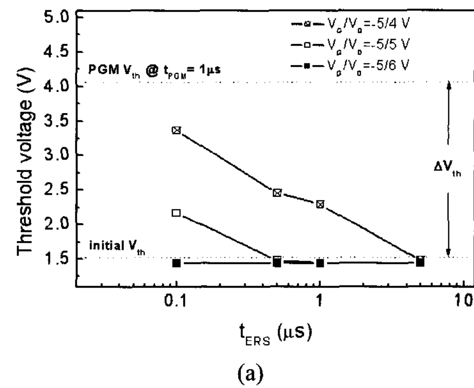


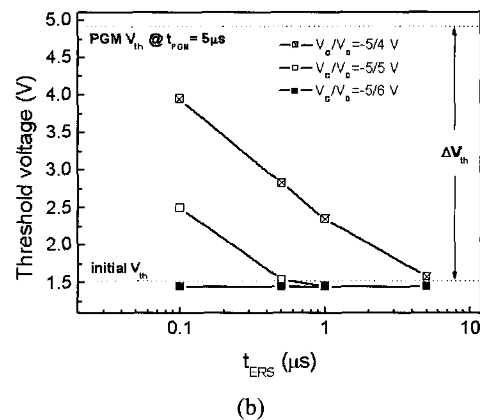
Fig. 5. log I_D-V_G characteristics of initial state, a bit-programming, and a bit-erasing for single bit of the proposed cell with the local channel doping profiles when drain bias is 0.1 V. The programming time (t_{PGM}) was fixed at 5 μs for given biases of V_G=5 V and V_D=3.5 V.

when the device has the same #1 p-type channel doping as that shown in Fig. 2 near the x_j. With increasing ΔR_p of the n-type doping, the V_{th} margin improves significantly since the V_{th} increase due to the unwanted charge trapping near the bottom of the recess region is suppressed. In this case, the charges trapped in the storage layer near the x_j contribute dominantly V_{th} increase and the program V_{th} can be easily changed to the initial value by forward read (V_D=1.5 V), which leads to large V_{th} margin. By increasing ΔR_p of the n-type counter-doping, the n-type doping covers the bottom corner by which the corner effect of bottom region is suppressed. Higher peak concentration (1.5×10^{18} cm^{-3}) of the #2 doping gives larger V_{th} margin. However, the margin saturates for an ΔR_p larger than ~15 nm, which means that the bottom corner gives no further effect on the V_{th} margin. The DIBL increases with increasing ΔR_p of the #2 doping, but the DIBL is less than 100 mV/V.

Now we address erasing characteristics with band-to-band (BTB) hot-hole injection (HHI) in the storage node [16]-[18] for complete 2-bit/cell operation using device simulator [15]. For a bit-programming and a bit-erasing, we used channel hot-electron injection (CHEI) and band-to-band (BTB) hot-hole injection (HHI). Fig. 5 shows log I_D-V_{GS} characteristics of initial state, a bit-programming, and a bit-erasing for single bit of the proposed cell with the local channel doping profiles when drain bias is 0.1 V. The t_{PGM} was fixed at 5 μs for given biases of V_G=5 V and V_D=3.5 V. The ΔV_{th} after programming is about 3.3 V at a V_D of 0.1 V. The



(a)



(b)

Fig. 6. V_{th} characteristics versus t_{ERS} as a parameter of erasing bias (V_D) at a fixed V_G of -5 V. The t_{PGM} were fixed at 1 μs (a) and 5 μs (b) for biases of V_G=5 V and V_D=3.5 V. The t_{ERS} is changed from 0.1 μs to 5 μs.

V_{th} was defined as the control gate bias when the drain current is 1×10^{-7} A/cell as mentioned above. The erasing time (t_{ERS}) were changed from 0.1 μs to 5 μs for given biases of V_G=-5 V and V_D=5 V. For a short t_{ERS}, some electrons still remain in the storage layer. Higher V_{th} than initial V_{th} was maintained by the electrons trapped in the storage region near the drain x_j. When we increase the t_{ERS} to 5 μs, the erased V_{th} was shifted to initial V_{th}, because of increasing trapped hot-hole density.

Fig. 6 (a) and (b) show V_{th} characteristics versus t_{ERS} as a parameter of erasing bias of V_D at a fixed V_G of -5 V. Before the erasing, the charge trap layer near the drain was programmed at V_G/V_D of 5/3.5 V for t_{PGM}s of 1 μs and 5 μs, respectively, by using CHEI method. In Fig. 6 (a) and (b), ΔV_{th}s between initial V_{th} state and bit-programming state for t_{PGM}s of 1 μs and 5 μs are 2.56 V and 3.3 V, respectively. Then we performed erasing by changing t_{ERS} from 0.1 μs to 5 μs using BTB HHI method. When we use V_G=-5 V and V_D=4 V to erase the

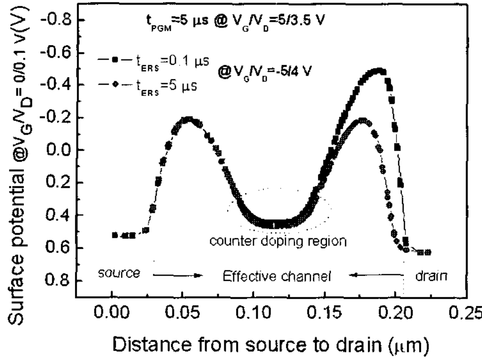
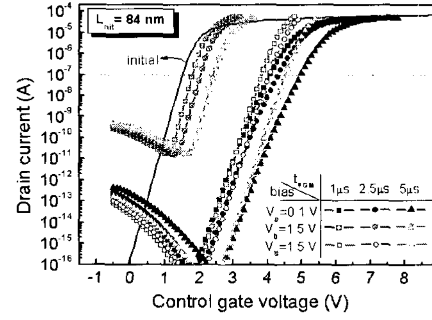


Fig. 7. Surface potential along the channel surface from the source to the drain as a parameter of t_{ERS}. Erasing times are 0.1 μs and 5 μs. V_G and V_D for the erasing are -5 V and 4 V, respectively.

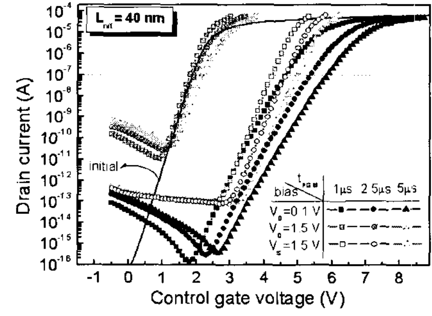
programmed cell for 0.1 μs, the V_{th} was decreased by 28 % for a given t_{ERS} of 0.1 μs. However, we could obtain much faster erasing speed (0.1 μs) by increasing V_D to 6 V at a fixed V_G of -5 V. We could also achieve fully bit-erased cell by increasing t_{ERS} to about 5 μs at a given V_D of 4 V.

To show internal physics regarding the bit-erasing, surface potentials along the channel surface from the source to the drain as a parameter of t_{ERS} (0.1 and 5 μs) are shown in Fig. 7. The surface potential was prepared at V_G of 0 V and V_D of 0.1 V to exclude the effect from control gate bias. Due to high #1 doping near source/drain x_js and #2 counter doping in the bottom of the recessed region, peak surface potential is observed near source-side x_j and drain-side x_j, which means the V_{th} of the cell is mainly determined by the #1 doping. The t_{PGM} was fixed at 5 μs at a given bias of V_G=5 V and V_D=3.5 V. It can be observed from the peak potential near the drain at a t_{ERS} of 0.1 μs that the electrons are injected into only the storage layer near the drain by the CHEI. When t_{ERS} is 0.1 μs, there are still many electrons in the trap layer so that the barrier height near the drain is higher than the height near the source. For longer t_{ERS} than 5 μs, the cell V_{th} is not lowered because the potential barrier near the source cannot change although the barrier near the drain can be lowered.

Now we compare programming characteristics in both structures in Figs. 8 and 9. The programming was achieved by channel hot electron (CHE) injection into the space type storage layer. Fig. 8 (a) and (b) show log I_D-V_G characteristics of devices before and after



(a)



(b)

Fig. 8. log I_D-V_G characteristics of flash devices before and after CHE programming for t_{PGM}s of 1, 2 and 5 μs at V_G=5 V and V_D=3.5 V. Figures (a) and (b) show the characteristics, respectively, for the charge storage lengths of 84 nm and 40 nm. Solid and cross symbols stand for read currents when drain bias of 0.1 and 1.5 V, and open symbols represent read current at source bias of 1.5 V, after programming. The V_{th} is defined as the control gate bias when the drain current is 1×10^{-7} A/μm as represented by dotted line.

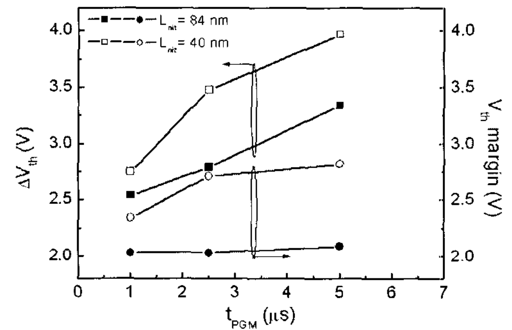


Fig. 9. ΔV_{th} and V_{th} margin versus the t_{PGM} as a parameter of storage layer length at V_G=5 and V_D=3.5 V. The ΔV_{th} is a V_{th} shift after programming, and the V_{th} margin is a difference between reverse read V_{th} and forward read V_{th}.

programming as a parameter of t_{PGM}. The t_{PGM} was changed from 1 to 5 μs at given biases of V_G=5 V and V_D=3.5 V. As t_{PGM} increases, ΔV_{th} increases at a low forward read (V_D=0.1 V). The device with short storage

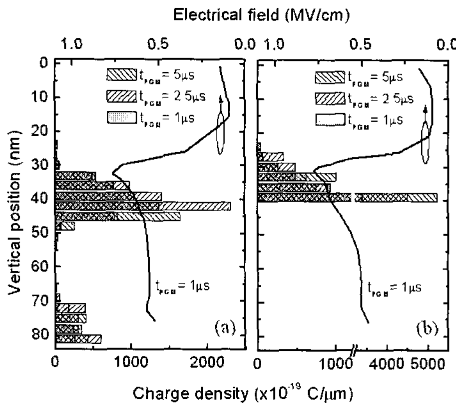


Fig. 10. Trapped charge distribution and electric field profile in the vertical storage layer as a parameter of t_{PGM} from 1 to 5 μs. Figures (a) and (b) represent the distributions and field profiles for the storage layer lengths of 84 and 40 nm, respectively.

layer shows higher SS (subthreshold swing) than that of long storage layer, which seems to be due to high-density stored charge in the localized region as shown in Fig. 10. With a high reverse read (V_S=1.5 V), the ΔV_{th} decreases a litter. Device with short storage layer shows larger ΔV_{th} decrease and change with the reverse read. In case of a high forward read (V_D=1.5 V), the ΔV_{th} of both devices decreases significantly since the channel region near the charge trapped region is depleted. The device with long storage layer shows some deviation from the initial curve mainly due to unwanted charge storing near the bottom corner although the #2 counter doping covers the bottom region. Thus the device with short storage layer has better V_{th} margin for 2-bit/cell since it has no storage layer near the bottom and higher charge density near x_j than that in long storage case. However, the sub-threshold slope of programmed devices with the short storage layer as shown in Fig. 1 (b) are larger than that of programmed devices with the long storage layer as shown in Fig. 1 (a) since higher charge density trapped in the short storage layer gives higher channel resistance [19].

The characteristics shown in Fig. 8 are summarized in Fig. 9 in a point view of ΔV_{th} and V_{th} margin for 2-bit/cell. The ΔV_{th} and V_{th} margin increase with increasing t_{PGM}. For t_{PGM} of 2.5 μs, the device with a storage layer length of 40 nm shows 28% higher ΔV_{th} and 35% higher V_{th} margin than those of the device with a storage layer length of 84 nm. Thus we can achieve fast programming speed with a short storage layer at given bias condition.

To see internal physics for the different characteristics with the length of storage layer, we investigated charge density distributions in the storage layer formed on the side-wall of the recess region for both long and short lengths of the storage layer as shown in Fig. 10 (a) and (b), respectively. Here vertical position of 0 nm means the top surface of the non-recessed thin body. The x_j is located at 30 nm. As the t_{PGM} increases, the trapped charge density increases generally. The maximum charge density is observed around 40 nm which is 10 nm below the x_j. However, the peak electric field is observed at the x_j. At the maximum charge density position of ~40 nm, the charge density for the short storage layer is about 2 times higher than that for the long storage layer, which increases ΔV_{th}. The stored charge distribution around x_j is wider in the long storage layer than in short storage layer. We have checked that the wide distribution of the charge around x_j in the long storage layer has no effect in the V_{th} margin for 2-bit/cell during high drain read (V_D=1.5 V). Unwanted charge trapping into the storage layer near the bottom corner mainly degrades V_{th} margin although #2 counter channel doping covers the bottom corner.

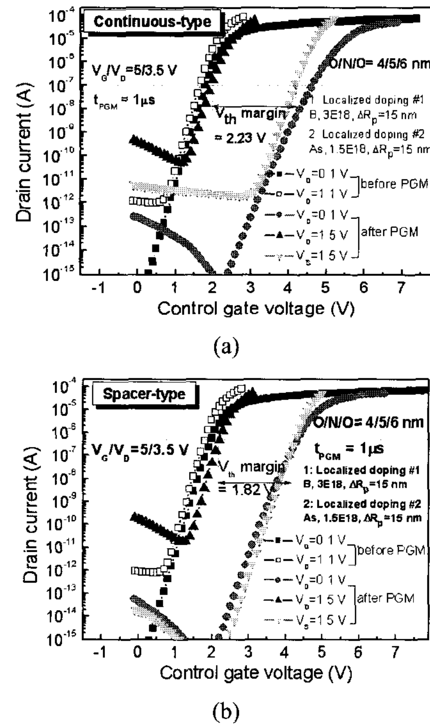


Fig. 11. *log* I_D-V_G characteristics of continuous-type (a) and spacer-type (b) devices with #1, #2 and #3 local doping profiles, before and after programming by HEI.

Now we compare device characteristics of the spacer-type and continuous-type NOR-type devices with recessed channel structure. Fig. 11 (a) and (b) show log I_D-V_{GS} characteristics and the V_{th} of the proposed spacer-type and continuous-type device with #2 doping profiles as shown in Fig. 1 (a) and (c), respectively. In Fig. 11 (a), the ΔV_{th} after programming is about 2.9 V at a V_{DS} of 0.1 V. The V_{th} margin at a given read bias of 1.5 V is increased to 2.23 V, since the n-type counter doping alleviates significantly the V_{th} shift with unwanted charge trapping near the bottom of the recess region. Fig. 11 (b) shows log I_D-V_G characteristics under the same situation as Fig. 11 (a). Under the programming bias condition, most of the hot electrons are trapped into the storage layer near the x_j and small number of electrons can be trapped into the storage near the bottom of the recess region. The n-type counter-doping alleviates significantly the V_{th} shift with the unwanted charge storage near the bottom of the recess region. As the result, we can achieve larger V_{th} margin of 1.82 V. The I_D-V_G curves in Fig. 11 (a) and (b) show not only excellent 2-bit/cell operation but also good DIBL characteristics.

We discuss how to form nano-dots in the recessed channel devices. For example, conventional LPCVD, sputtering and plasma doping methods can be a candidate for the dot formation. For the formation spacer-type storage node, anisotropic RIE could be used to etch away the dots in the bottom region.

IV. Conclusions

We have reviewed 2-bit/cell flash memory devices with spacer-type or continuous-type charge storage layer in recessed channel region for high density and high performance sub-50 nm NVM technology. By adopting counter-doping near the bottom of the recess region, we achieved successfully 2-bit/cell operation with a V_{th} margin larger than 1.5 V at a given gate length of 50 nm. Bit-programming and bit-erasing of the device were successfully achieved by using CHEI and BTB HHI, respectively, for given bias and program/erase time. We have investigated programming characteristics for 2-bit/cell with the length of the spacer-type charge trapping layers formed on the side surface of recessed channel region in high-density and high-performance 50 nm NOR-type Flash memory cell. For given source/drain junction depth of 30 nm and recess depth of 100 nm, the flash memory device with a storage layer length of 40 nm shown better ΔV_{th} and V_{th} margin than those in the length of 84 nm for the same program condition. Spacer-type and continuous-type storage layers were compared and shown reasonable characteristics. Thus the device structure can be one of the most promising device structures for high performance 50 nm NOR-type NVM technology.

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