CMOS 이미지 센서의 웨이퍼 레벨 어셈블리를 위한 스페이스 형성에 관한 연구

(A study on forming a spacer for wafer-level CIS(CMOS Image Sensor) assembly)

김 일 환*, 나 경 환*, 김 현 철*, 전 국 진*

(Ill hwan Kim, Kyounghwan Na, Hyeon Cheol Kim, and Kukjin Chun)

요 약

본 논문에서는 CMOS 이미지 센서의 웨이퍼 레벨 어셈블리를 위한 스페이스 제작 방법을 설명하였다. 스페이스 제작을 위해서 SU-8, PDMS, Si-interposer를 이용하는 세 가지 방법을 제안하였다. SU-8 스페이스에서는 균일한 두께 특성을 위해서 웨이퍼 회전 장치를 고안했으며, PDMS 스페이스에서는 glass/PDMS/glass 구조의 정렬 접합을 위해서 새로운 접합 방법을 제안하였다. Si-interposer를 이용한 스페이스 제작에서는 DRF을 이용한 접합 조건을 확립하였다. 세 가지의 실험 결과 Si-interposer를 이용한 스페이스 제작 시 glass/스페이스/glass 구조의 접합력이 가장 뛰어났으며, 접합력의 크기는 32.3MPa의 전단응력을 나타내었다.

Abstract

This paper describes the methods of spacer-fabrication for wafer-level CIS(CMOS Image Sensor) assembly. We propose three methods using SU-8, PDMS and Si-interposer for the spacer-fabrication. For SU-8 spacer, novel wafer rotating system is developed and for PDMS(poly-dimethyl siloxane) spacer, new fabrication-method is used to bond with alignment of glass/PDMS/glass structure. And for Si-interposer, DFR(Dry Film Resist) is used as adhesive layer. The spacer using Si-interposer has the strongest bonding strength and the strength is 32.3MPa with shear.

Keywords : spacer, CIS, SU-8, PDMS, DFR

I. Introduction

In case of image sensor like CIS (CMOS Image Sensor) the size of device grows according to increase of pixel's number. But consumer's demand for miniaturization needs wafer-level package and assembly. The traditional chip-scale package and assembly of CIS camera module is shown in Fig. 1. In this figure, holder and barrel increase the size of the camera module and manual assembly using this device also increase the price.

On the contrary, wafer-level packaged CIS module shown in Fig. 2 needs not any additional holder or barrel and the spacer between lens part and sensing part plays a role of defining a focal length of lens and combining two parts (lens and sensing parts). In this application, the spacer has to have hundreds of thickness with uniformity of a few micrometer and strong bonding strength for combining lens part and sensing part.

For the spacer-fabrication of this application, main stream of currently developed methods is using thick photoresist because of low price and simple

* 정회원, 서울대학교 전기컴퓨터공학부
  (School of Electrical Engineering and Computer Science, Seoul National University)
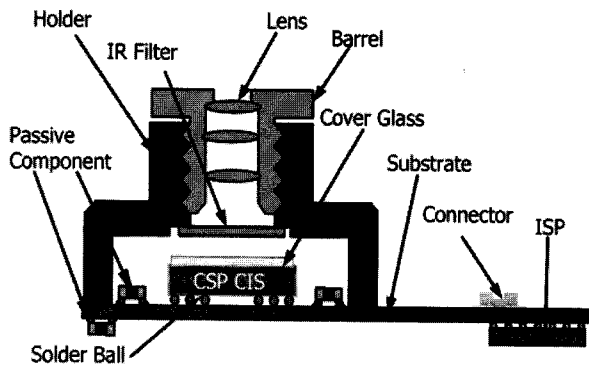
그림 1. 칩 단위로 패키징 된 CIS 카메라 모듈의 모식
도. 이러한 카메라 모듈의 어셈블리를 위해서는
칩 레벨의 패키지와 렌즈, CIS, ISP 등의 어셈
블리가 필요함

Fig. 1. Schematic of chip-scale packaged CIS camera
module. For assembly of this camera module, it
needs chip-level package and assembly of lens,
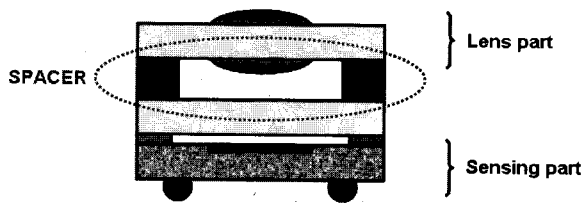CIS, ISP and etc.

그림 2. 웨이퍼 레벨로 패키징 된 CIS 모듈의 모식도.
여기에서 스페이스는 렌즈 부분의 초점을 정의
하며 렌즈와 센싱 부분을 결합하는 역할을 함

Fig. 2. Schematic viewing a cell of wafer-level
packaged CIS module. The spacer plays a role
of defining a focal length of lens part and
combining two parts (lens and sensing parts).

fabrication[1]. But this method has difficulty with good
thickness-uniformity of thick photoresist and bonding
strength.

This work presents methods to solve the problems
of thickness-uniformity and bonding strength. First,
using SU-8 as thick photoresist and wafer rotating
system for good thickness-uniformity, thick (400μm)
and uniform SU-8 layer is acquired. Additionally,
adhesive layer is used for improving of bonding
strength. Second, for more thickness-uniformity and
bonding strength, PDMS (poly-dimethyl siloxane)
spacer is developed by molding method. The last, for
the most thickness-uniformity and bonding strength,
the spacer using Si-interposer and DFR (Dry Film
Resist) is developed.

II. Design and Fabrication

1. Design and Fabrication

For the spacer-fabrication, we propose three types
as spacer-materials, SU-8, PDMS and Si-interposer.
Fig. 3 shows the schematics of each case. SU-8 and
PDMS are used as polymer-material in Fig.3 (a) and
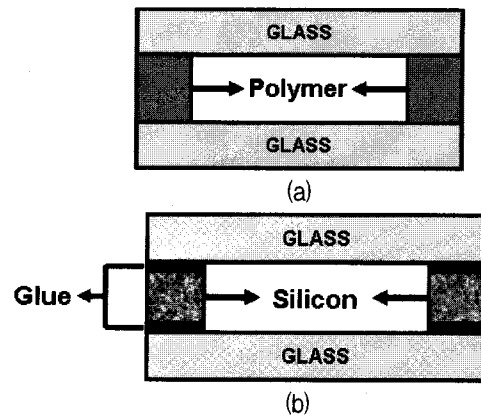Fig. 3 (b) shows the spacer using Si-interposer.

그림 3. CIS 모듈의 응용을 위한 스페이스 제작 방법.
(a) PR이나 PDMS와 같은 두꺼운 폴리머를 사
용하는 경우 (b) Si-interposer와 접착물질로써
DFR을 사용한 경우

Fig. 3. The spacer-fabrication methods for application
of CIS module. (a) using thick polymer
(photoresist or PDMS), (b) using Si-interposer
and DRF as glue layer.

A. Using SU-8

Experiments using thick SU-8 layer as the spacer
are performed. The experiments to form thick (400μm)
and uniform (<5%) SU-8 layer and to enhance the
adhesion of SU-8 to glass wafer using additional
adhesion layer are performed.

First of all, seen in Fig 4. we solve the incline of
SU-8 to achieve thick and uniform SU-8 layer.
Generally, thick photoresist lean on one side because
hot-plate's surface isn't accurately perpendicular to
the gravity. In case of thin photoresist, this
phenomenon doesn't happen because viscosity of the
photoresist is increased by evaporation of most of
solvent in photoresist during spin coating and soft
bake time of thin photoresist film is short. But the
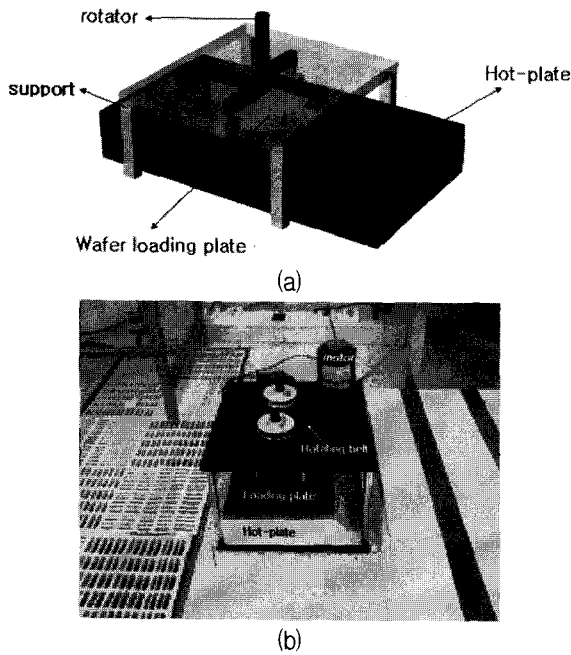viscosity of thick photoresist is not increased by

(a)

(b)

그림 4. 웨이퍼 회전 시스템. (a) 웨이퍼 회전 시스템의
모식도, (b) Hot-plate가 장착된 웨이퍼 회전 시
스템

Fig. 4. Wafer rotating system. (a) Scheme of wafer
rotating system, (b) Wafer rotating system on
Hot-plate.

much after spin coating and freestream region beyond
the boundary layer of thick film is much wider than
that of thin film. These can make far more flow in
thick photoresist film than thin photoresist film, and
moreover flow volume is increased in proportion to
the soft bake time which is increased according to
film thickness. The effect of glass surface not
perpendicular to gravity can be canceled out by
rotating the glass wafer. So wafer rotating system is
made which can rotate wafer continuously during
bake time. Wafer rotating system consists of motor,
rotating belt, rotator, rotating plate and controller as
seen in Fig. 4.

Fig. 5 shows the distribution of thickness of SU-8
with and without wafer rotating system, respectively.
The graph of Fig. 5 (a) leans on one side, but the
graph of Fig 5 (b) is relatively parallel to the surface.
These figures say the use of wafer rotating system
cancel out the incline due to wafer surface out of
perpendicular to the gravity. The measured
uniformity of 400μm thick SU-8 is 3.25%. As a result
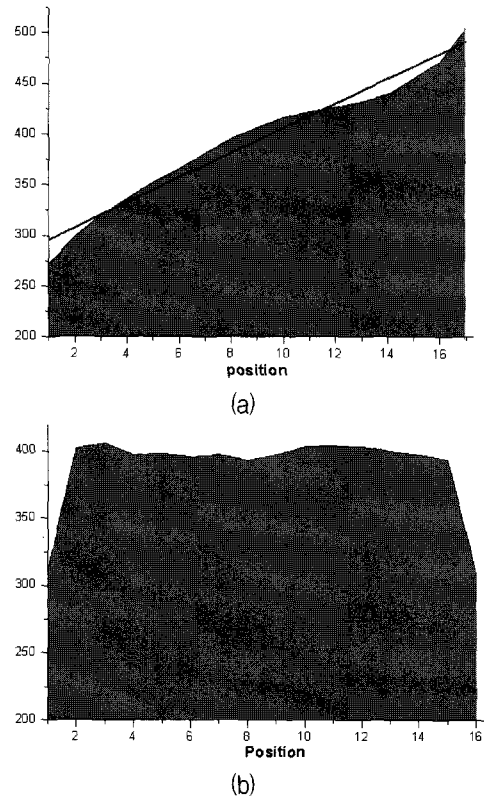of experiment varying exposure time, SU-8 film

(a)

(b)

그림 5. SU-8 필름의 두께 분포. (a) 웨이퍼 회전 시스
템을 사용하지 않은 경우, (b) 웨이퍼 회전 시스
템을 사용한 경우 (position의 숫자는 4인치 웨
이퍼의 아랫부분에서 윗부분을 1에서 16으로
나누었을 때 해당하는 위치를 가리킴)

Fig. 5. Thickness distribution of SU-8 film (a) without
wafer rotating system, (b) with wafer rotating
system. (The position-number indicates the
position of 4-inch wafer from top to bottom,
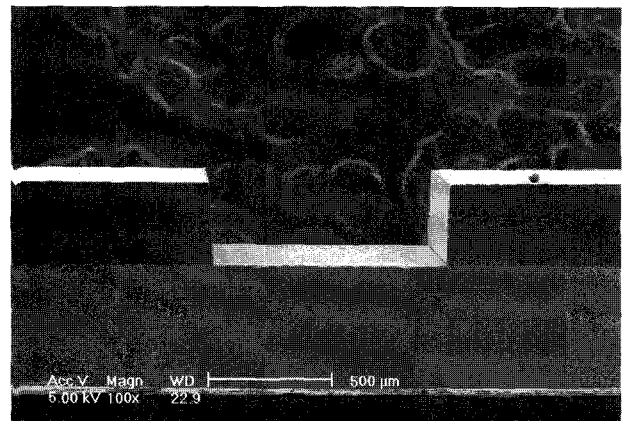top-number is 1 and bottom-number is 16)

그림 6. 400μm 두께의 SU-8 패턴의 측면 사진
Fig. 6. Profile of 400μm thick SU-8 pattern.

profile of $87°$ is able to be formed by $2600mJ/cm^2$ of
exposure energy as seen in Fig. 6.
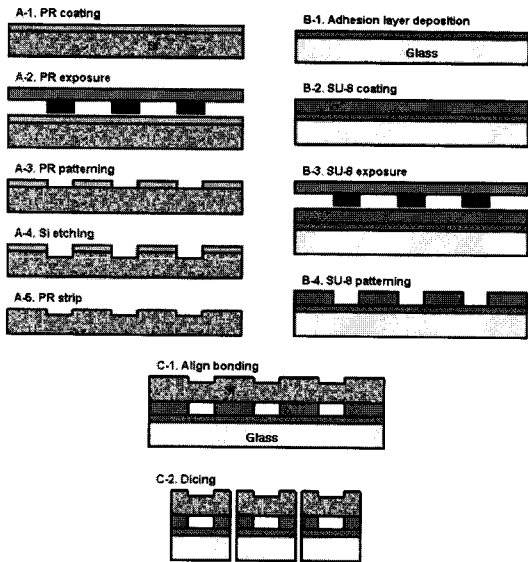
It is known that the adhesion strength of SU-8 to

그림 7. 접합층 테스트를 위한 공정 순서
Fig. 7. Process flow of adhesion layer test.

glass is poor[2]. Thus, the experiment for improvement of adhesion strength of SU-8 film to glass wafer have to be performed. Several materials are deposited onto glass wafer as interlayer between glass and SU-8 to improve adhesion strength. Gold, nickel, silicon dioxide, polycrystalline silicon, silicon nitride and chrome are chosen as adhesion material and SU-8 coated on silicon wafer is bonded to silicon wafer for reference. The process flow is described in Fig. 7.

B. Using PDMS-sheet

PDMS-spacer is also polymer-spacer as seen in Fig. 3 (a). PDMS is cheaper than SU-8 (about 1/10) and thickness-uniformity is easily achieved using molding process. The method of making PDMS-spacer of $400\mu m$ is explained as follows. First, Al layer of 3000Å is deposited on Si wafer of $400\mu m$ thickness. The Al layer plays a role of etch stop layer and preventing footing effect. Second, the Si wafer is bonded with 500μm glass wafer by anodic bonding of Al-glass. And then the $400\mu m$ Si layer is selectively etched using SiO_2 mask. Fig. 8 shows the mold fabricated with this method.

Third, PDMS mixture (curing agent : PDMS = 1 : 10) is poured onto the mold master and covered with a dummy Si wafer. Then high pressure is induced on
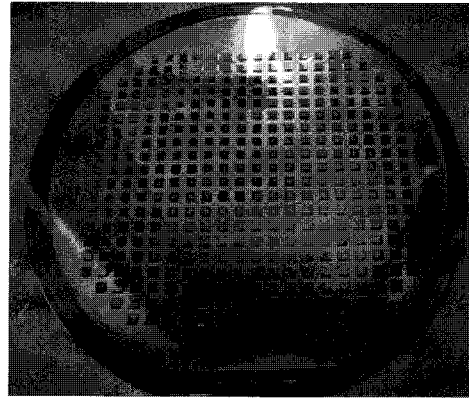

그림 8. PDMS 스페이스를 만들기 위해 제작된 Si 몰드의 사진
Fig. 8. Photograph of the fabricated Si mold for making PDMS-spacer.
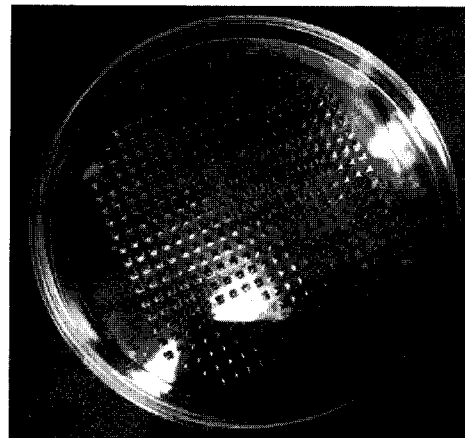

그림 9. 제작된 PDMS 스페이스의 사진 (페트리 접시에 놓여있음)
Fig. 9. Photograph of the fabricated PDMS-spacer placed in Petri dish.

each side of the wafers to form PDMS-spacer of 400 μm thickness. Finally, the PDMS-spacer is completed as Fig. 9.

In addition, Fig. 10 shows the method that the PDMS-spacer is align-bonded between two glass wafers. The fabricated PDMS-spacer is attached on a dummy glass wafer. After activating the PDMS surface of the temporary bonded PDMS-glass wafer by plasma, the wafer is align-bonded with a glass wafer using EV-620 aligner. The PDMS-glass wafer align-bonded by EV-620 aligner is baked on hot-plate of 75°C for 30 minutes. Then the irreversible covalent bond is formed between the interface of PDMS surface activated by plasma and glass. And the other PDMS surface and the dummy
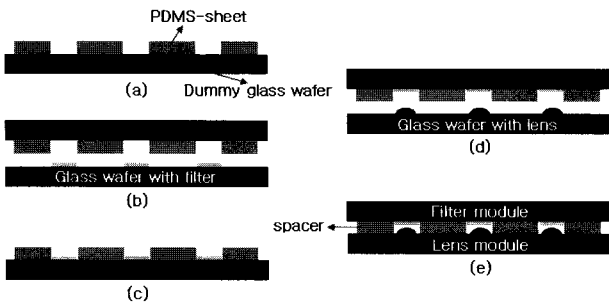
그림 10. 유리-PDMS-유리의 정렬 및 접합을 위한 제작
공정의 모식도. (a) 더미 유리 웨이퍼에 붙여진
PDMS 스페이스, (b) PDMS 스페이스와 유리 웨
이퍼의 정렬 접합, (c) 더미 유리 웨이퍼의 분
리, (d) 접합된 PDMS-유리와 또 다른 유리 웨
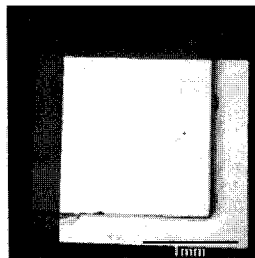이퍼의 정렬 접합, (e) 정렬 접합된 유리
-PDMS-유리 웨이퍼

Fig.   10. Schematic of the fabrication process for aligning
and bonding of glass-PDMS-glass.
(a) PDMS-spacer attached on dummy glass
wafer, (b) align-bonding of PDMS-spacer and
glass wafer, (c) separating dummy glass wafer,
(d) align-bonding of PDMS-glass and another
glass wafer, (e) align-bonded glass-PDMS-glass
wafer.
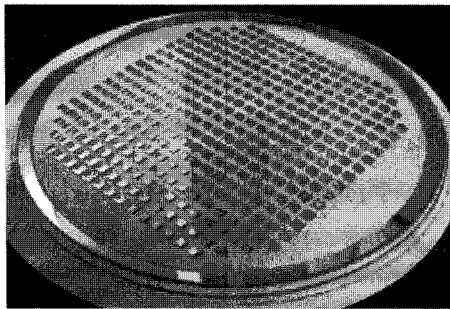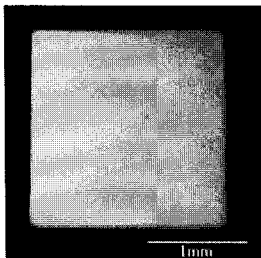
그림 11. 접합된 유리-PDMS-유리의 사진.
(a) 웨이퍼 레벨 정렬 접합된 유리-PDMS-유리,
(b) EV-620 장비를 이용해 정렬 접합한 패턴,
(c) EV-620 장비를 이용하지 않고 접합한 패턴

Fig.   11. Photograph of the bonded glass-PDMS-glass.
(a) wafer-level align-bonded glass-PDMS-glass,
(b) an align-bonded pattern using EV-620
aligner,
(c) a bonded pattern not using EV-620 aligner.

glass wafer is easily separated. The bonded
PDMS-glass wafer and another glass wafer can be
align-bonded using EV-620 aligner with same
procedure.

Fig. 11 shows the align-bonded glass-PDMS-glass
wafer.

C. Using Si-interposer

Si-interposer as spacer-material has a advantage
of good thickness-uniformity. But we cannot use
anodic bonding of Si and glass because of low
temperature limit for CIS application. In this work,
DFR is used as adhesion layer.

Dry film resist can be easily coated on patterned
interposer not by spin coating but by laminating and
can be easily patterned by using photolithography
technology because it is photosensitive polymer. The
sequence of process is as follows. First, silicon
interposer is patterned by deep Si etch process using
AZ-5214 as etch mask. Si-interposer is patterned to
$50\mu m$ deep trench. DFR with protect film is laminated
onto patterned Si-interposer. DFR is soft-baked at
$90^\circ C$ for 90 seconds and exposed with $120mJ/cm^2$ of
exposure energy through patterned mask. And then
DRF was laid on $90^\circ C$ of hot-plate for 90 seconds for
post exposure bake and developed with 1% of Na_2CO_3
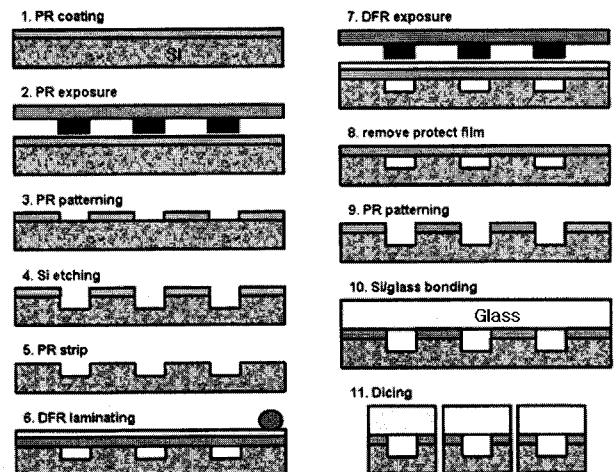solution for 80 seconds. After that, Si-interposer with

그림 12. DFR을 사용한 Si-interposer와 유리의 정렬 접합
을 위한 공정도

Fig.   12. Process flow for align-bonding of Si-interposer
and glass using DFR.

patterned DFR is bonded to dehydrated glass wafer and then bonding set is diced into samples. Whole process flow is described in Fig. 12.

III. Measurements and results

Tensile and shear strength are measured for the samples that have passed dicing test after bonding process.

As shown in Fig. 13, for tensile strength measurement, a sample is fixed to bottom chuck with glue, and then top chuck is pulled upward at a constant speed. The tensile force at the moment of the fracture occurrence is measured. Since the external tensile force is proportional to the bonding area, the tensile force divided by the area gives fracture strength in MPa unit. To prevent the glue fracture, the bonding strength of the glue should be considered. Fig. 14 shows the schematic of shear

strength measurement. A sample is fixed to a chuck with glue, and then top substrate is pulled in a shear direction. The shear force at the moment of the fracture occurrence is measured. As in the tensile strength case, the external shear force per unit area gives fracture strength. To prevent the glue fracture and glass fracture, the bonding strength of the glue and the height of top substrate should be considered.

Using SU-8 as the spacer, it looks as if the wafers are well bonded, but the interface between glass and SU-8 is detached during dicing the bonded wafer. In case of depositing various adhesion layers to increase the bonding strength, all cases show identical results.

Using PDMS as the spacer, it has maximum bonding strength of 0.5MPa with tensile strength. But in this case, many samples are detached during dicing.

Fig. 15 shows the shear strength of Si-interposer /DFR/glass bonding according to bonding temperature. The lower the bonding temperature is, the smaller the deformation of polymer is and the weaker the bonding strength is. When bonding temperature is too high, the trap of void in bonding area or the rise of internal pressure of cavity due to increase of outgassing can make the bonding strength between polymer and substrate weaker. For these reasons, the optimal temperature for bonding exists
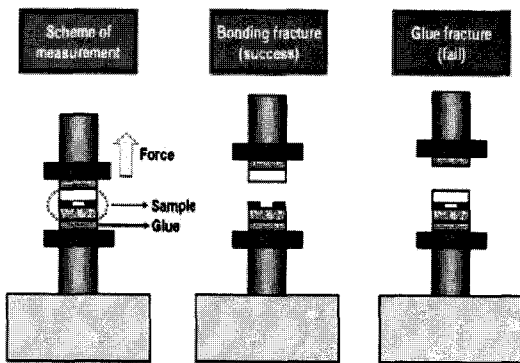

그림 13. 장력 측정의 모식도
Fig.   13. Schematic of tensile strength measurement.
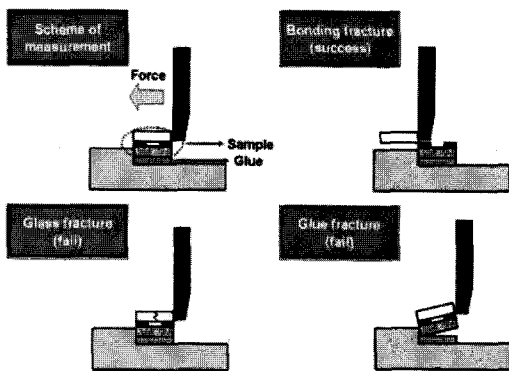

그림 14. 전단 응력 측정의 모식도
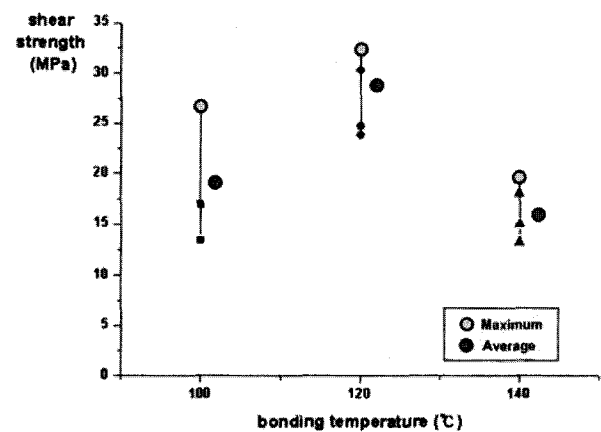Fig.   14. Schematic of shear strength measurement.

그림 15. 접합 온도에 따른 DFR의 전단 응력.
       (이 실험에서 접합력은 2000N이 적용됨)
Fig.   15. Shear strength of DFR bonding according to
       bonding temperature. (In this case, bonding
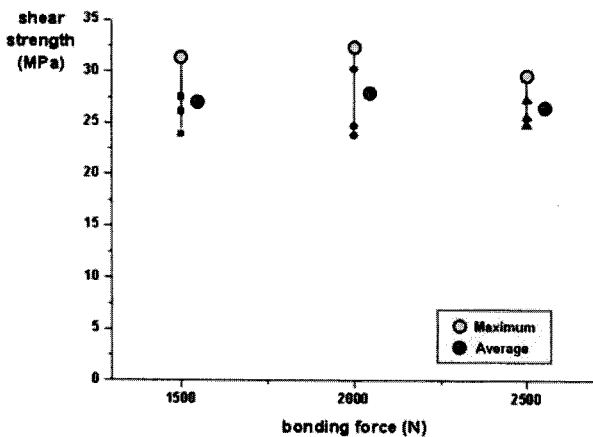   force is 2000N.)

그림 16. 접합력에 따른 DFR의 전단응력
(이 실험에서 접합 온도는 120℃가 적용됨)
Fig. 16. Shear strength of DFR bonding according to bonding force.
(In this case, bonding temperature is 120℃.)

according to polymers[3~4]. And we can know that the optimal temperature for DFR bonding is nearly 120℃ as seen in Fig. 15.

Fig. 16 shows the shear strength of DFR bonding according to bonding force. Generally, the bonding strength is proportional to bonding force below the critical point and then the bonding strength is saturated to bonding force beyond the critical point. As seen in Fig. 16, the shear strengths of bonding are nearly invariable to 1500, 2000 and 2500N of bonding forces. Thus, it can be known that critical bonding force for DFR bonding is below 1500N and sufficient bonding strength would be obtained if bonding force above 1500N is applied.

IV. Conclusions

Wafer-level package with thick, uniform, and patterned spacer using polymer bonding was researched. Three methods were devised using SU-8, PDMS, Si-interposer. Using SU-8, the spacer of 400 μm with 3.25%-uniformity can be made and using PDMS, the spacer of more thickness-uniformity and bonding strength can be made, but in this two cases, satisfactory bonding strength cannot be acquired. Si-interposer using DFR as adhesion layer had sufficient bonding strength bearable to dicing test and

the maximum bonding strength was 32.3MPa with shear strength. These results show the spacer using Si-interposer with DFR is available to CIS application and the others (SU-8 and PDMS) is cheaper than Si-interposer but many improvement in bonding strength is demanded.

References

[1] Sumitomo Bakelite Co. Ltd., "CMOS image sensor/New Low Cost Production process/Dam on Glass & Dam on Wafer", 2006.
[2] E. H. Conradie and D. F. Moore, "SU-8 thick photoresist processing as a functional material for MEMS applications", Journal of Micromechanics and Microengineering, Vol. 12, pp. 368-374, 2002.
[3] C. T. Pan and P. J. Cheng, "Intermediate wafer level bonding and interface behavior", Microelectronics Reliablility, Vol. 45, pp. 657-663, 2005.
[4] B. Bilenberg and T. Nielsen, "PMMA to SU-8 bonding for polymer based lab-on-a-chip systems with integrated optics", Journal of Micromechanics and Microengineering, Vol. 14, pp. 814-818, 2004.

────────────────── 저 자 소 개 ──────────────────
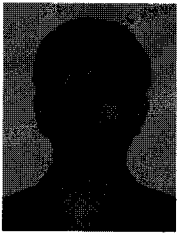
김 일 환(정회원)
2002년 KAIST 전자전산학과
      학사 졸업.
2004년 서울대학교 전기컴퓨터
      공학부 석사 졸업
2008년 현재 서울대학교 전기
      컴퓨터공학부 박사과정 중
<주관심분야 : 반도체, MEMS, Packaging>

나 경 환(정회원)
2005년 서울대학교 기계항공
      공학부 학사 졸업.
2007년 서울대학교 전기컴퓨터
      공학부 석사 졸업.
<주관심분야 : 반도체, MEMS,
Packaging>

김 현 철(정회원)
1990년 서울대학교 전자공학과
      학사 졸업.
1992년 서울대학교 전자공학과
      석사 졸업.
1998년 서울대학교 전자공학과
      박사 졸업.
2008년 현재 한국정보사회진흥원 UIT 클러스터
      추진센터 재직.
<주관심분야 : 반도체, MEMS, Packaging>

전 국 진(정회원)
1977년 서울대학교 전자공학과
      학사 졸업.
1981년 University of Michigan,
      전기공학과 석사 졸업.
1986년 University of Michigan,
      전기공학과 박사 졸업.
2008년 현재 서울대학교 전기컴퓨터공학부 교수
<주관심분야 : 반도체, MEMS, Packaging, RF>