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A Study of On-Chip Voltage Down Converter for Semiconductor Devices

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Abstract

This paper proposes a new on-chip voltage down converter(VDC), which employs a new reference voltage generator(RVG). The converter adopts a temperature-independence reference voltage generator, and a voltage-up converter. The architecture of the proposed VDC has a high-precision, and it was verified based on a 0.25㎛ 1P5M standard CMOS technology. For 2.5V to 1.0V conversion, the RVG circuit has a good characteristics such as temperature dependency of only 0.2mV/℃, and the voltage-up circuit has a good voltage deviation within ±0.12% for ±5% variation of supply voltage VDD. The output voltage is stabilized with ±1mV for load current varying from 0 to 100mA.

Key words: voltage down converter, reference voltage generator, voltage-up, VDC, RVG

I. Introduction

The designs of voltage down converters are to meet the differences in current profiles of storage arrays and peripheral circuitry. The voltage down converter for storage arrays aims at stability with high but isolated change in driving current bursts. The one for peripheral circuitry handles lower and more frequent current bursts. It would be more convenient to design voltage down converters separately for storage arrays and peripheral circuitry.

Two design concerns are reported in voltage down converter circuits: low power consumption and stability in operation. A lower voltage operation brings substantially lower power consumption since the power consumption is proportional to the square of the operating voltage. Then, the stability issue of a voltage down converter reports the minimal voltage changes due to some operational disturbances such as external supply voltage fluctuations, abrupt internal current surge and temperature changes. It helps to get normal operations under some external power supply voltage fluctuations, say 10%, without excessive additional circuitry. Without circuitry having some slight voltage increase along the ambient temperature, memories typically experience slower access. It is also to allow some tolerance on internal voltage affected by parameter variations during a silicon fabrication process[1][2]. These are the reasons, in semiconductor memory devices, to achieve both low power operation and stability in operation, of which an on-chip DC-to-DC Voltage down converter (VDC) is strongly desired.

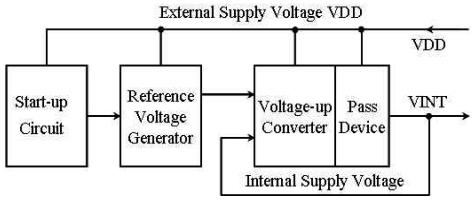

Fig. 1 The architecture of VDC

In this paper, we propose a voltage-up circuit basedVDC. Employing a bandgap reference(BGR) based on vertical parasitic bipolar in n-well, the circuit achieves good insensitivity characteristics of

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temperature and external supply voltage. Therefore, it is suitable for the low-power memory chips.

II. Analysis of Conventional VDC

A voltage down converter for converting an external power voltage into an internal power voltage and providing the internal power voltage to an internal circuitry comprising is defined by: a reference voltage generation means for receiving the external power voltage and generating a constant reference voltage where variation of the external power voltage and change of circumstance temperature are compensated; a reference voltage converting means for converting the reference voltage from the reference voltage generation means into a reference voltage for stress mode or a reference voltage for normal mode; and a driving means for receiving the references to generate the internal power voltage required to operation of the internal circuitry.

The architecture of the conventional VDC is shown in Fig.1. The basic blocks include a start-up, a reference voltage generator, a voltage-up converter, and a pass device circuit with low output impedance and large driving capability[3][4].

2.1 Reference voltage generator

A reference voltage generator(RVG) with low sensitivity to temperature and supply voltage is commonly required in analog or digital circuits. To begin with, there are three types of reference voltage generator using MOS transistors only: threshold-based generators, threshold difference based generators and thermal voltage based generators[5][6]. Unlike the bipolar type generators, these reference generation circuits are compatible to the standard CMOS process, whereas BJT type's reference generators provide with an excellent temperature coefficient. It has temperature dependency of less than 1mV/℃ and supply voltage dependency of 2mV/V, which are pretty good values. But, it has some drawbacks of an additional diffusion step in silicon fabrication making process complex and inferior device reliability and model in accuracy. To overcome the difficulties related to the parasitic transistors of MOS structure, BiCMOS type devices are being employed since it provides with a handy design parameters. It should be noted that an ideal BJT is not available in CMOS

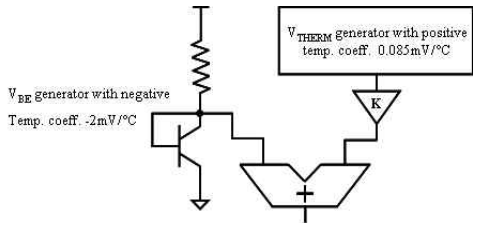


Fig. 2 Structure of a bandgap RVG

technology. A *pnp* BJT is made using the n-well normally associated with a pMOS[7] behaving the p-substrate as the collector.

Designs of band-gap reference voltage generators report the temperature dependency issue complying with the coefficient limit less than 100ppm/℃. Two circuits, each having opposite polarity in temperature coefficients, are merged so that the temperature dependencies cancel out each other. The structure of a bandgap reference voltage generator is shown in Fig.2, which consists of a V_{BE} generator and a V_{THERM} generator. The V_{BE} generator has the temperature coefficient of -2mV/℃ and the V_{THERM} generator has the coefficient of +0.85mV/℃. The output of the V_{THERM} generator is amplified to match the temperature coefficient of the V_{BE} generator, which are merged to yield the reference voltage[8].

2.1.1 Temperature dependency of V_{ref}

There are several methods to realize a temperature independent voltage. The base emitter junction used as a core component of the bandgap reference is the most popular approach. The general bandgap reference voltage is described by a linear combination of base-emitter voltage. We can compensate temperature dependent voltage by adding a positive-TC(temperature coefficient)voltage to a negative-TC voltage[9]. The temperature behavior of a pn-junction voltage is described by

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_c}{I_s} - \frac{V_T}{I_s} - \frac{E_g}{KT^2} V_T, \qquad (1)$$

where V_T is the thermal voltage. With T at room temperature and V_{BE}=750mV, $\frac{\partial V_{BE}}{\partial T} \approx -1.5 mV/^{\circ}K$.

The positive-TC voltage comes from the voltage difference between two pn-junction.

$$V_{BE1} - V_{BE2} = \triangle V_{BE} = V_T \ln \frac{I_c}{I_s} - V_T \ln \frac{I_c}{nI_s} = V_T \ln n \quad (2)$$

where n equals to the current density ratio of Q_2 to Q_1. Ideally, adding a positive-TC voltage to a negative-TC voltage can realize a zero TC 1.25V at the room temperature. Additionally, the reference voltage is required to be robust to the power supply voltage. An easy way to improve power supply rejection ratio(PSRR) is to increase the open loop gain.

2.1.2 Range of the external supply voltage

A conventional CMOS bandgap reference circuit is shown in Fig.3[10]. Here the output bandgap reference voltage is given by

$$V_{ref} = V_{EB2} + \frac{R_2}{R_1} V_T \ln \left(\frac{A_1}{A_2} \right) \quad (3)$$

where A_1 and A_2 are the emitter areas of Q_1 and Q_2. The first term to right in equation (3) is a complimentary to absolute temperature(CTAT) voltage and the second term a proportional to absolute temperature(PTAT) voltage. temperature independent voltage is obtained by adding these two voltages. The minimum supply voltage($V_{DD(MIN)}$) required for the operation of this circuit is given by

$$V_{DD(MIN)} = V_{ref} + V_{SD_{SAT3}} \quad (4)$$

for conventional BGR V_{ref}=1.25V. V_{SDsat3} can vary from 0.1 to 0.3V depending on the process, resulting in a $V_{DD(MIN)}$ of around 1.4V. Further the limitation on $V_{DD(MIN)}$ comes from the operation amplifier; we need to ensure that the operational amplifier can also work at this supply voltage. A technique to achieve sub 1V bandgap reference voltage is discussed in [11], but the operational amplifier in that design requires a $V_{DD(MIN)}$ of 1.5V. So design of low voltage bandgap reference circuits are limited by the supply voltage requirements if the operational amplifier is designed to work with a minimum supply voltage of 900mV.

2.2 Voltage-up converter

Fig. 4. shows the conventional voltage-up circuit including a differential amplifier, a pass device, and a level shifter[3]. The level shifter adopts long channel pMOS transistors including $M_A \sim M_C$ and the two transistors $M_A \sim M_B$ are entirely the same. Since these devices are in a saturation region, the current can be expressed as

$$I = \frac{\beta_1}{2} \left\{ \frac{V_{INT} - V_{FB}}{2} - |V_{TH}| \right\}^2 = \frac{\beta_2}{2} [V_{FB} - |V_{TH}|]^2 \quad (5)$$

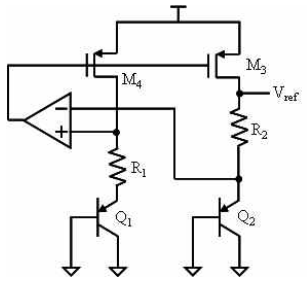


Fig. 3 CMOS bandgap reference circuit

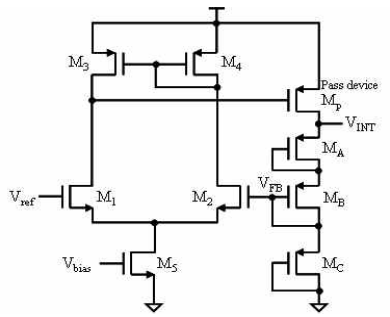


Fig. 4 Voltage-up circuit

where β_1 is the transistor gain factor of M_A and MB, β_2 is that of M_C, and V_{TP} is the threshold voltage of the transistors. β_1 and β_2 are initially identical and are changed by blowing the fuses. If the gain of the amplifier is sufficiently large, the feedback voltage V_{FB} is nearly equal to V_{ref}.

III. Design and Analysis of Proposed VDC

This paper relates to a circuit for generating a reference voltage in a semiconductor device and particularly to an internal voltage down converter which produces an internal supply voltage by down-converting an external supply voltage.

3.1 Design of proposed VDC

Two aspects are important in voltage down

converter design: lower impedance of power supply node and stabilization of the DC output level. It is difficult to an optimized design for both design concerns at the same time. Two different approaches are employed to meet these design variables: internal voltage source and reference voltage source. An internal voltage source is designed primarily aiming at lower output impedance so that it can supply constant current on loads with varying impedance. A design of a voltage reference source, on the otherhand, concentrates to overcome variations in external operational conditions such as external supply voltage fluctuations and temperature changes. A successful voltage down converter is to take advantages of these two different design approaches.

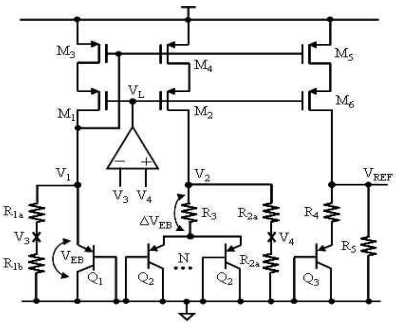
3.2 Analysis of proposed VDC

Fig. 5 is the circuit of proposed VDC, which is composed of a reference voltage generator based on bandgap reference, and a voltage-up circuit with low output impedance and high-driving capability. The function of the RVG is to produce a stable reference voltage V_{ref} that is free from fluctuations of external supply voltage V_{DD} and temperature. The proposed bandgap RVG circuit consists of a CMOS wide-swing differential-amplifier, parasitic BJTs, and resistors. The voltage-up circuit consists of a differential amplifier, a M_P pass device and a level-shifter consists of a M_A pMOS device, a R_{Drv} driving resistor and two MOSFETs M_{11} and M_{12} for voltage feedback. The wide-swing differential amplifier adjusts the internal supply voltage V_{int} level to match the V_{int} shift level with the V_{ref} level. Because of the high drivability requirement of VDC, the pass device size of M_P is relatively large.

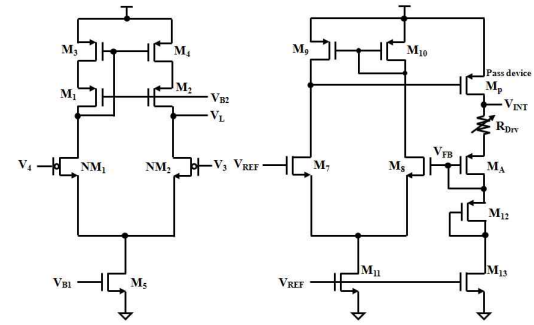
3.2.1 Proposed bandgap RVG

Major concerns of bandgap reference circuit designs are to obtain a stable voltage level even with power supply fluctuation, process parameter scattering and ambient temperature variation. Various circuit innovations are applied to keep an accurate and precise voltage level at the output of a reference voltage generator. We now review some of representative designs in terms of stability and immunity against power and junction temperature changes.

In this design some modifications are made to the circuit of conventional RVGs[3][6][8][11]. The main differences are that an amplifier with a nMOS input stage is used and the inputs of the amplifier are



(a) Proposed RVG circuit



(b) Wide-swing differential amplifier (c) Voltage-up circuit

Fig. 5 Proposed VDC circuit

connected to native nMOS stage instead of pMOS input stage. The resulted circuit is shown in Fig. 5(b). In addition, the output impedance of the current sources is improved by adding cascode devices. This is important in order to reduce the supply voltage sensitivity of the voltage V_{ref}. When the sum of the voltages across R_{1a} and R_{1b} is equal to V_{EB1}, the voltage with respect to ground at V_3 and V_4 is $(R_{1b}/(R_{1a}+R_{1b}))\cdot V_{EB1}$.

$$V_{DD_{\min}} = \max\{ V_{EB1}\times\left(\frac{R_{1b}}{R_{1a}+R_{1b}}\right) - |V_{TNM,NM1}| + |V_{DSAT,MP3}|, V_{ref} + |V_{TP,MP5}| \} \quad (6)$$

In the original design the operational-amplifier(op-amp) inputs are connected to the voltages V_1 and V_2 that are roughly in 0.4V-to-0.6V level, which is

not a suitable input for an op-amp in a 1V-to-2.5V design. To overcome that the resistors R_1 and R_2 are divided into two series connected parts. Now the voltages V_3 and V_4, which are nominally set between 150 and 200mV, are in proper range for an op-amp with pMOS input transistors.

Fig. 5 (b) illustrates the structure of the native nMOS, which is easily fabricated by CMOS option process. The transistors, with V_3 and V_4 applied to the gates, are native nMOS transistors(V_{TH}=-0.15V) because the threshold voltages of the enhancement-mode nMOS transistors exceed $V_{-feedback}$ in the standard 0.25㎛ CMOS process.

A current which is proportional to the absolute temperature(PTAT) is generated and added into a base-emitter voltage of Q_3. From Fig. 5(a), M_1~M_6 form cascode current mirrors which can operate for lower supply voltage. The amplifier enforces V_3 and V_4 to have equal potential. As a result, V_1 and V_2 also have the same potential when R_{1a}=R_{2a} and R_{1b}=R_{2b}. Therefore, generated current is given by

$$Current_I = \frac{V_T \cdot \ln N}{R_3} + \frac{V_{EB1}}{R_1} \quad (7)$$

where N is the emitter area ratio, V_T is the thermal voltage, and $R_1 = R_{1a} + R_{1b} = R_2 = R_{2a} + R_{2b}$. The current I is injected to R_4 by the current mirror formed by M_3, M_4, and M_5, and this gives the reference voltage as follows:

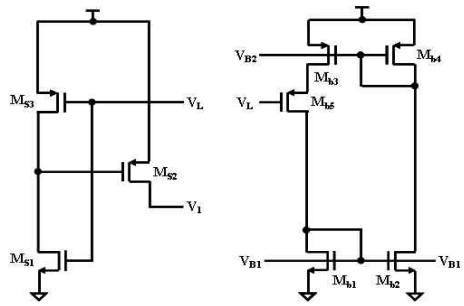
$$V_{ref} = V_{BE3} + \frac{R_4}{R_2} \cdot \left\{ V_{EB1} + V_T \cdot \left(\frac{R_2}{R_3} \ln N \right) \right\} \quad (8)$$

A scaled-down bandgap reference voltage can be obtained by an appropriate resistor ratio of R_4 to R_2. Moreover, trimming on the resistor ratio(ratio of R_2 to R_3) to achieve a good TC can be done on R_{1a} and R_{2a} simultaneously. This structure is suitable for any CMOS technology to implement low-voltage bandgap reference.

3.2.2 Proposed voltage-up converter

The proposed voltage-up circuit is shown in Fig.5 (c). The voltage-up circuit can be converted the output voltage of bandgap reference V_{ref} into a higher internal supply voltage V_{INT}. And it should have enough current supply capability and low output impedance so that the V_{INT} is not very much affected by the large loading current fluctuation. So the size of pass device M_P is relatively large.

The circuit is composed of a feedback amplifier and a M_P, R_{Drv}, M_A, M_{12}, and M_{13}, which plays an important role in obtaining further accuracy in the output voltage of the voltage-up circuit. The output voltage V_{INT} is $I_{PTAT} \cdot R_{Drv} + V_{TPA} + V_{TP12} + V_{SAT13}$



(a) Start-up circuit (b) Bias circuit

Fig. 6 Design of start-up and bias for the proposed VDC

where V_{TPA} is the built-in voltage of the threshold voltage of pMOS device. To minimize the voltage error of V_{INT} from the nominal value V_{DD} for a maximum V_{ref}-range, the trimming characteristics should be designed such that any two adjacent lines pass through points(V_{ref}, V_{DD}-ΔV_{INT}) and (V_{ref}, V_{DD}+ΔV_{INT}), as suggested by the vertical broken lines in Fig.5(c).

$$V_{INT} = |(I_{PTAT} \cdot R_{Drv}) + V_{TPA} + V_{TP12} + V_{TP13}| \quad (9)$$
$$= \left[2\sqrt{\frac{\beta_2}{\beta_1}} + 1 \right] [\, V_{ref} - |V_{TPA}| \,]$$

3.2.3 Start-up and bias circuitry

The start-up circuit of the proposed reference circuit is shown in Fig.6(a). The RVG circuit does not operate properly if V_{B2} and V_L follow the V_{DD} voltage because the bias current would become zero. That is the reason a start-up circuit is needed for the proposed RVG. The RVG circuit has two stable operation points: one desired operating point and the other one whose current is zero when V_1 and V_2 are equal in Fig.5(a). To ensure that the circuit always ends up in the correct operation point a startup circuit is included. In the desired operation point the voltage V_1 is above the threshold and thus the startup circuit has no effect on the RVG circuit.

The bias circuit of the proposed reference and

voltage-up circuit is shown in Fig.6(b). The op-amp and voltage-up circuit are biased by voltage bias of the bias circuit, the start-up circuit also ensures its bias current.

IV. Simulation Results

The proposed on-chip VDC is designed to provide a constant DC voltage around 1.0V with external supply voltage of 2.5V. Also, the proposed RVG can be successfully lowered in the HSPICE simulation when the threshold voltages are optimized for a low-voltage and a wide-range voltage operation. The proposed VDC is designed with a 0.25㎛ CMOS technology.

4.1 Simulation results of V_{ref}

For the temperature effects, the simulation results are shown in Fig.7. Here, in the conventional RVG, V_{ref} is about 1.25V, and the V_{DD} minimum is 3.3V. However, in the proposed RVG, the operation voltage is simply limited by the resistance ratio of R_1, R_2, and R_4 and little influenced by the absolute value of the resistance. So the V_{DD} minimum varies with the temperature. Fig. 7 shows the measured V_{ref} characteristics of the proposed RVG. V_{ref} is 0.575V(at 27℃)±0.015V from -20℃ to 100℃ at 2.5V supply voltage.

The proposed VDC using the designed bandgap reference voltage generator depends on the matching of current mirror. However when the supply voltage is changed, current matching of a simple current mirror will be degraded. Wide-swing cascode current mirror can be used to improve the performance. Another effective method is to make use of amplifier.

The amplifier enforces the two inputs having equal voltage and PTAT current can be obtained. The operational principle is the same as the one using current mirror. However, the supply dependence is greatly reduced since the amplifier is able to enforce the two inputs to be equal at different supply voltages. Fig. 8 shows the measured V_{ref} characteristics of the proposed RVG at V_{DD}(at 2.375V, 2.5V, and 2.625V) variations.

4.2 Simulation results of V_{INT}

The Voltage-up circuits should have enough current supply capability and a low output impedance so that the output voltage is not very much affected by the large loading current fluctuation. Fig. 9 shows the simulated gain and phase versus frequency for voltage-up with p-type pass transistor M_P. When the load impedance

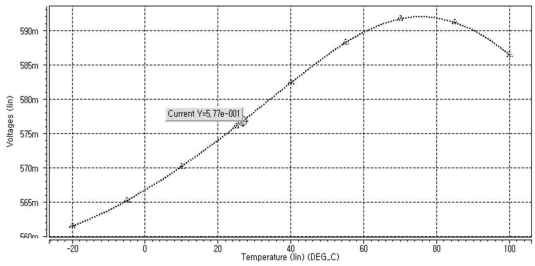


Fig. 7 Hspice result of V_{ref} voltage as a function of temperature

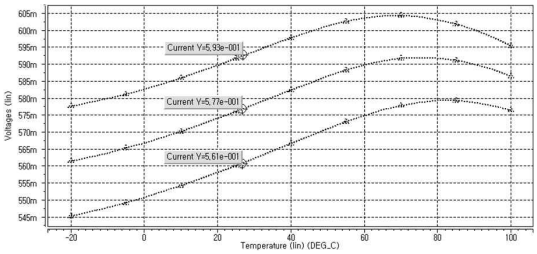


Fig. 8 Hspice result of V_{ref} voltage as a function of temperature at V_{DD} variations

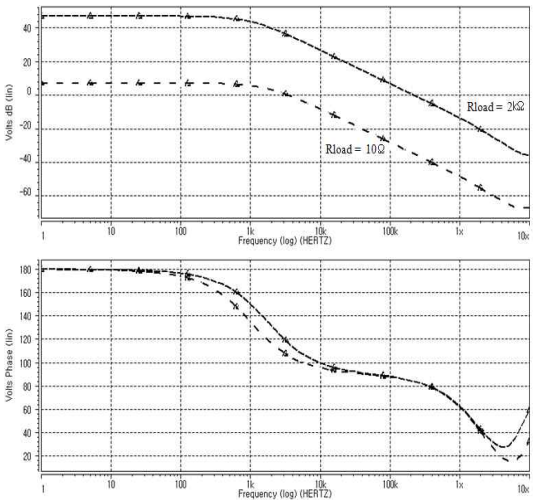


Fig. 9 Frequency response of the voltage-up converter

varies from 10Ω to 2kΩ(Rload from 100mA to 0.5mA), the phase margin is only among 60° to 90°, enough to ensure the loop stability for semi-conductor device. Fig.10 is the simulation result of V_{INT} for different supply voltages, which can provide a stable voltage around 1.0V with external supply voltage of 2.5V. A capacitance Cload=20pF and resistance Rload=3kΩ are used as the load impedance. Only ±0.12% deterioration of V_{INT} for ±5% variation of supply voltage VDD is achieved. For temperature effects, the simulation results shown in Fig.11 indicate that the temperature dependency of V_{INT} is only 0.2mV/℃ with the temperature ranging from -20 to 100℃. The simulation results shown in Fig.12 indicate that the proposed VDC can provide a maximum output current of 100mA when the output voltage V_{INT} is stabilized about 1.0V. Fig.12 shows the simulated result of V_{INT} for different load current. V_{INT} is among 1.0022V to 1.0044V when the load current changes from 0 to 100mA. Fig.13 shows the simulated transient response of the VDC. The output of the VDC can stabilize very quickly when the output impedance is varying. The transient response time is only 0.6μs. Besides the pMOS pass device(M_p), the total current of VDC 13.2μA, which requires standby power dissipation of 33.0μW.

The output voltage(V_{INT}) is stabilized around 1.0V. Because the negative feedback in the voltage-up circuit can offer an adequate phase margin, and the output of the VDC will stabilize very quickly when the output impedance is varying. If a shorter transient response time is required, the voltage-up circuit should be biased at a higher current, which will take a larger power dissipation on standby mode of the VDC. Finally, the performance comparison of existing VDC is summarized in Table. 1.

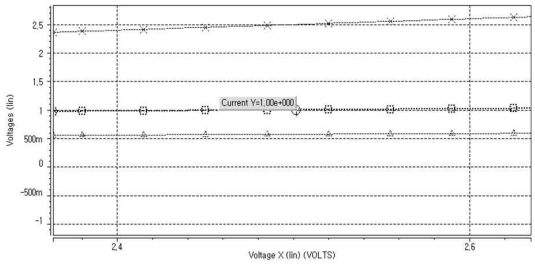


Fig. 10 Hspice result of V_{INT} and V_{REF} voltage as a function of V_{DD} variation

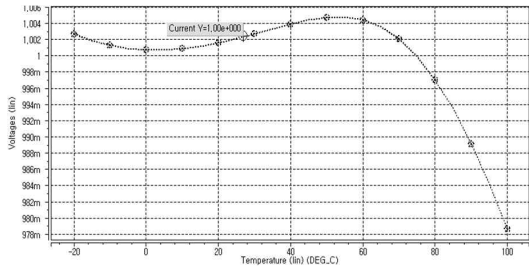


Fig. 11 Hspice result of V_{INT} voltage as a function of temperature

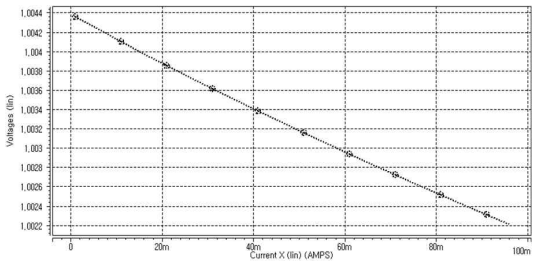


Fig. 12 Hspice result of V_{INT} as a function of output current

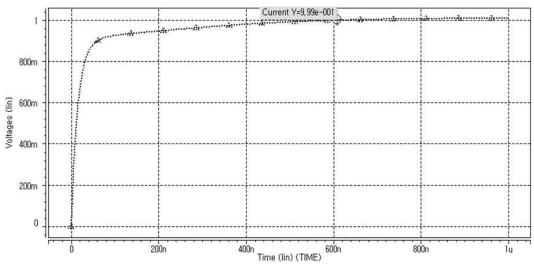


Fig. 13 The transient characteristic of the V_{INT}

Table 1. Performance comparison of proposed VDC

Key features list	[3]	[4]	Proposed
	5.0 -3.3[V]	3.3 -1.8[V]	2.5 -1.0[V]
Supply voltagvariation vs. Output voltage[V]	3.295~3.305	1.774~1.801	0.985~1.015
Temperature variation vs. Output voltage[V]	3.265~3.355 (-40~100℃)	1.778~1.801 (0~70℃)	0.979~1.005 (-20~100℃)
Load current variation vs. Output voltage[V]	3.266~3.3 (0~100mA)	1.793~1.801 (0~100mA)	1.002~1.004 (0~100mA)
Transient response[㎲]	0.6		0.6
Standby power[㎼]	98.32	37.32	33.0

V. Conclusion

An on-chip VDC for analog and digital mixed circuit has been developed. It uses a negative-type voltage-up circuit with stability, relatively small temperature dependency, and small standby power dissipation. Therefore, it is well suited for low power IC chip. It converts 2.5V supply voltage to 1.0V in the internal supply voltage. In HSPICE simulation results, internal voltage is bounded (about 1.0V) in the proposed circuit when transient rapidly increases during 0.6㎲. It has a couple of good characteristics such as low temperature dependency of only 0.2mV/℃ and small voltage deviation within ±0.12% for ±5% variation of power supply voltage. This circuit is designed with a 0.25㎛ CMOS technology.

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