A 1.2 V 7-bit 1 GS/s CMOS Flash ADC with Cascaded Voting and Offset Calibration

Young-Chan Jang*, Jun-Hyun Bae*, Ho-Young Lee, Yong-Sang You**, Jae-Whui Kim**, Jae-Yoon Sim*, and Hong-June Park***

Abstract—**A 1.2 V 7-bit 1 GS/s CMOS flash ADC with an interpolation factor of 4 is implemented by using a 0.13 μm CMOS process. A digital calibration of DC reference voltage is proposed for the 1st preamp array to compensate for the input offset voltage of differential amplifiers without disturbing the high-speed signal path. A 3-stage cascaded voting process is used in the digital encoder block to eliminate the consecutive bubbles up to seven completely, if the 2nd preamp output is assumed to have a single bubble at most. ENOB and the power consumption were measured to be 5.88 bits and 212 mW with a 195 MHz 400 mV_{p-p} sine wave input.**

Index Terms—**Flash ADC, offset, reference calibration, voting**

I. Introduction

Recently, the high speed flash ADCs with the resolution of 6 to 7-bits and the sampling rate up to 1 GS/s are widely used for the multi-band OFDM Ultra-Wideband (UWB) receiver[1] and the digital read-channel of optical and magnetic data storage devices such as DVD[2,3] Blu-Ray Disk and Hard Disk. Since these flash ADCs are usually integrated on the same chip with the large digital signal processing blocks and the supply voltage of digital blocks is reduced to a small value with scaling, it is convenient to reduce the supply voltage of ADC to the same value as the digital supply voltage. With a reduced supply voltage, flash ADCs are sensitive to the analog noise such as the input offset voltages of amplifiers and comparators, and the reference voltage fluctuation. Especially, when the flash ADC is implemented using the interpolation method to reduce the chip area, the input offset voltage of amplifiers can cause the consecutive bubbles which can not be removed by the conventional 3-input majority voter [4].

In this work, a 7-bit 1 GS/s CMOS flash ADC with the supply voltage of 1.2 V was implemented by using a 0.13 μm CMOS process. A reference voltage calibration scheme was used at the 1st preamp stage for the offset voltage control, and the 3-stage cascaded voting process was proposed to eliminate the consecutive bubbles up to seven in the thermometer code.

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II. Circuit Description

1. Architecture

Fig. 1 shows the block diagram of the proposed ADC. It consists of the arrays of 1st preamp, distributed track/hold (DTH), 2nd preamp, comparator, the resistor interpolation network, and the digital encoder block [3]. Although the signals and circuits are shown in the single-ended version in Fig. 1 for simplicity, they are implemented in the differential version for high noise immunity. The 1st preamp array consists of 39 4-input differential amplifiers (including 6 dummies). The circuit schematic of the differential amplifier is shown in Fig. 2 [2]. The differential output voltage of the amplifier can be represented by.

$$V_{outp} - V_{outn} = A_{v1} \cdot \{(V_{inp} - V_{inm}) - (V_{refp} - V_{refm})\} \quad (1)$$

The gain A_{v1} of the 1st preamp was adjusted to a constant value of about 10 dB by a replica biasing circuit. To

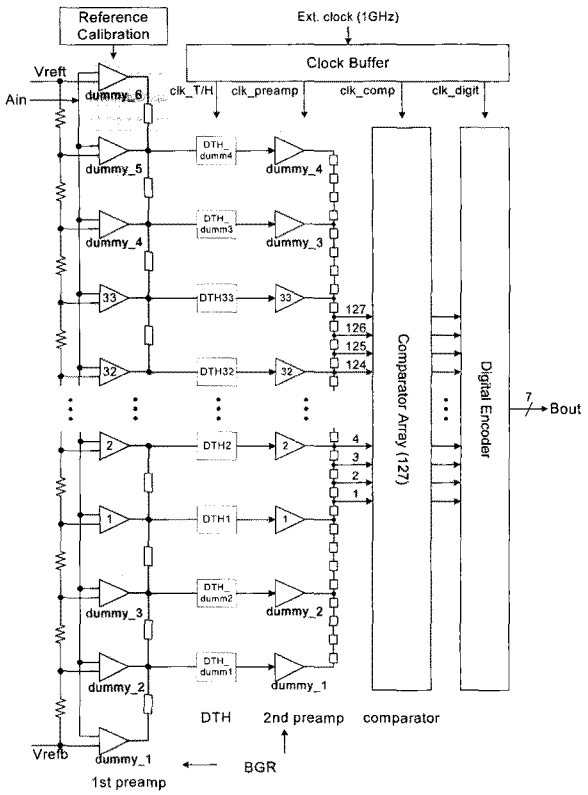


Fig. 1. Block diagram of proposed ADC.

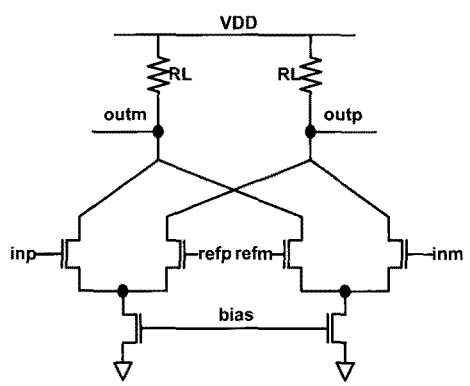


Fig. 2. 1st preamp circuit.

compensate for the input offset voltage of this 1st preamp array, the differential

DC reference voltage(V_{refp}-V_{refm}) is digitally calibrated after the power-on reset. Also the conventional resistor averaging scheme is applied to the output nodes of the differential amplifiers to further compensate for the input offset voltage [2,5].

The DTH array [3] consists of 37 pairs (including 4 dummies) of PMOS switches. The parasitic input capacitors of the 2nd preamp are used as the sampling capacitors. The 2nd preamp array consists of 37 differential pairs (including 4 dummies), each of which consists of an NMOS-input differential pair with resistive loads [2,3] and a PMOS switch for equalization.

A differential interpolation scheme with a factor of 4 was implemented as shown in Fig. 3(a). The output nodes of the two adjacent amplifiers in the 2nd preamp array are connected by a resistor string with four output nodes. Each output node of a resistor string is connected to a comparator input. This interpolation scheme reduces the number of 1st preamp, DTH and 2nd preamp, and hence the input capacitance of ADC into one fourth. The gain of the 2nd preamp array was adjusted to around 12 dB by a replica biasing circuit to compensate for the gain loss by

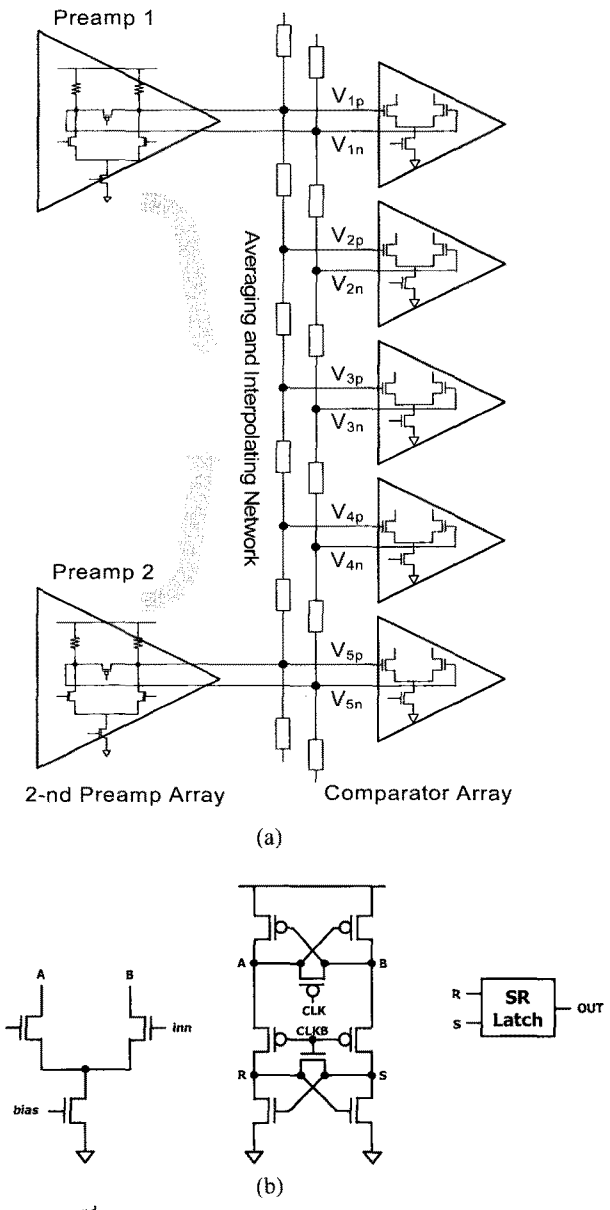


Fig. 3. (a) 2nd preamp array and interpolation with a factor of 4 (b) Schematic of comparator.

the resistor interpolation network [5]. The bandwidths of the 1st and 2nd preamps were about 800 MHz and 1.1 GHz at the 200 fF load, respectively. 33 amplifiers of the 1st and 2nd preamp arrays (excluding dummies) gave the 5-bit resolution and the resistor interpolation with a factor of 4 gave the additional 2-bit resolution, which gave the total 7-bit resolution.

The 127 comparators following the 2nd preamp array generate a 127-bit thermometer code, which is converted into a 7-bit binary code via a quasi-gray encoding by the digital encoder block. As shown in Fig. 3(b), a comparator consists of an input differential pair, a regenerative flip-flop and a SR latch [6].

The proposed ADC can generate consecutive bubbles in the thermometer code because of the interpolation scheme with the factor of 4. Since the conventional 3-input voting process[4] can eliminate only a single bubble, a 3-stage cascaded voting process was used in the digital encoder block of this work to eliminate the consecutive bubbles up to 7. The 2nd preamp output is assumed to have a single bubble at most. The bias and reference voltages were generated by a band-gap reference circuit.

2. Digital Calibration of Reference Voltage

Since a low supply voltage of 1.2 V is used in this work, the analog input voltage ranges from 750 mV to 1150 mV (400 mV swing, 800 mV differential swing). The 1st preamp is required to have a 5-bit resolution, which gives the input voltage resolution of 12.5 mV (25 mV differential). With a 10% variation of MOSFET gate length and a 15% variation of resistor load, however, the Monte Carlo simulation showed that the input offset voltage of the 1st preamp was about 20 mV, which was larger than the input voltage resolution.

To reduce the input offset voltage to a value smaller than 12.5 mV, two approaches were used. One is the conventional resistor averaging scheme applied to the output nodes of the 1st preamp array [2,5]. The other is a digital calibration scheme of DC reference voltage of differential amplifiers, which was proposed in this work. If the input offset voltage is larger than the input voltage resolution, the conventional resistor averaging network is no longer good enough to reduce the effect of input offset voltage.

The digital offset calibration schemes published in the literatures [7,8] adjust the relative driving strength of either branch of a differential pair. These methods increase the junction capacitance along the high-speed analog signal paths because of the added components, and hence they may slow down the circuit operation. In contrast to the above-mentioned published digital offset calibration schemes, the digital calibration scheme proposed in this work negligibly affects the high speed signal path because only the differential DC reference voltage of each 4-input differential pair of the 1st preamp array is adjusted without affecting the signal input voltage. Recently, the digital offset calibration scheme which adjusts the reference voltage was published in [9]. However, the on-chip calibration capability of this work was not implemented in [9].

During the initial calibration interval after the power-on reset, the input offset voltage of each differential pair is reduced to a value smaller than half of the input voltage resolution (0.5×12.5 mV) as long as the original input offset voltage is smaller than twice the input voltage resolution ($\pm$ 25 mV).

In this work, the digital offset calibration scheme was applied to the 1st preamp array. Fig. 4(a) shows the connectivity of a 4-input differential amplifier (*preamp30*) of the 1st preamp array during this normal operation before the digital offset calibration is performed. The analog input nodes (*inp*, *inm*) are connected to the differential analog input voltage(A_{in} of Fig. 1), The positive and negative reference voltage input nodes (*refp, refm*) are connected to the corresponding nodes of the reference resistor ladder (*ref30, ref4*), respectively. The reference resistor ladder is a single-line resistor ladder laid out in the U-shaped form. The *refp* and *refm* nodes of the adjacent amplifier (*preamp29*) are connected to the *ref29,* and *ref5* nodes of the reference ladder. The mid-point nodes such as *ref29.5* and *ref4.5* nodes are used for calibration only.

Fig. 4(b) shows the procedure of the digital offset calibration scheme proposed in this work. During the calibration mode, only one of the 39 amplifiers in the 1st preamp array is connected to the resistor averaging network with all the other amplifiers disconnected by the PMOS switches. Each amplifier of the 1st preamp array is calibrated one by one. When *preamp30* is enabled during the calibration mode, both *inp* and *inm* are connected to a common analog input voltage (0.95 V in this work, the mid-point of input voltage swing). Therefore the differential input voltage of *preamp30* is 0. The *refp* node of *preamp30* is connected to the *ref4* node of the reference ladder. The negative feedback loop composed of a comparator and a FSM

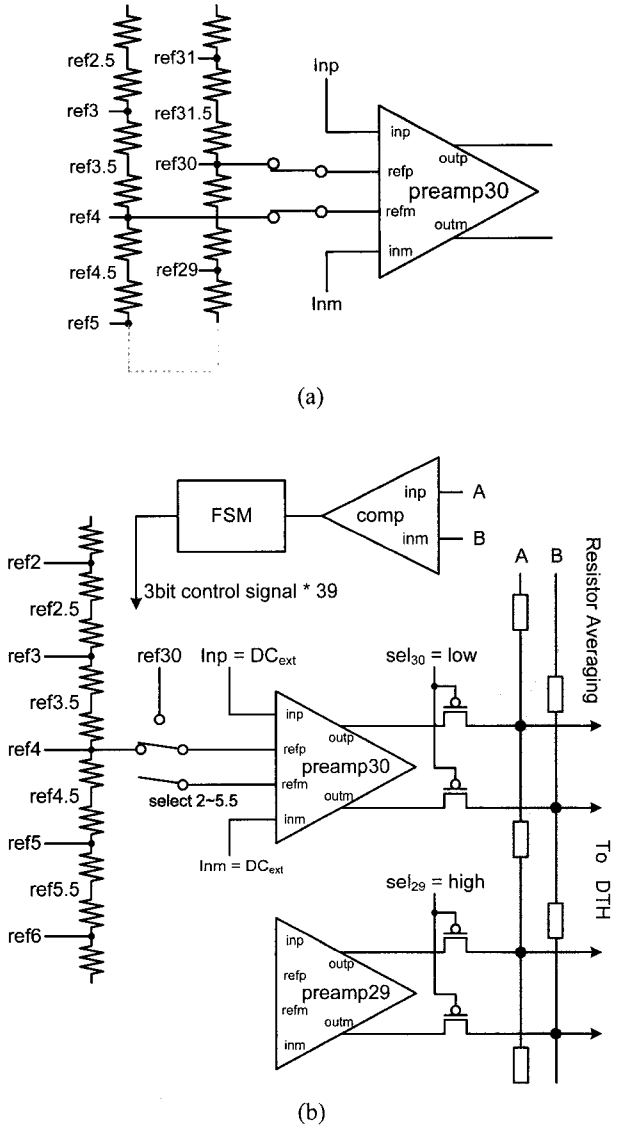


Fig. 4. (a) Operation of the 1st preamp before the offset calibration (b) Digital calibration procedure for input offset voltage control of 1st preamp.

which are implemented on chip determines the connection point of the *refm* node. At first, the *refm* node is connected to the *ref2* node. Then, the differential output voltage (V_{outp}-V_{outm}) of the *preamp30* is positive. After that, the *refm* node is moved to the next higher node (*ref2.5*). This sweep operation is continued until the differential output voltage (V_{outp}-V_{outm}) changes its polarity to negative or the *ref5.5* node is reached. This sweeping operation corresponds to the input offset voltage change of 43.75 mV with a resolution of 6.25 mV. During the normal operation, the *refm* node of *preamp30* is fixed at the node determined during the calibration mode.

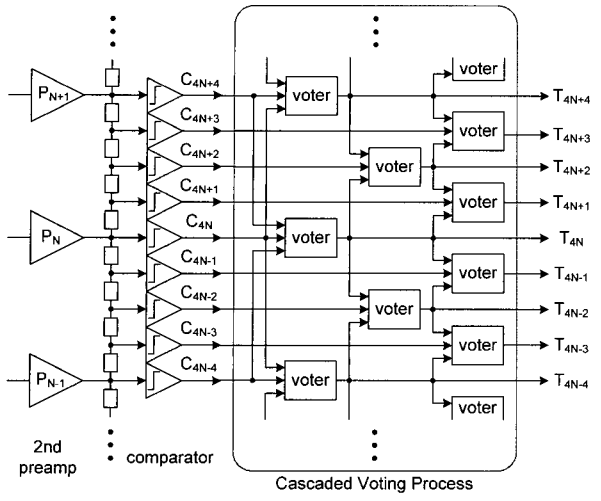
Although the mismatches among the resistors of the reference ladder may cause the non-linearity problem, they do not affect the monotonic property of the reference voltage. Therefore, the resistor mismatches do not affect the accuracy of the reference voltage calibration step. Also, the nonlinearity of the MOSFET switches between the reference ladder and the 1st preamp array do not increase the distortion of the 1st preamp, because the CMOS transmission gate switches are used to reduce the non-linearity of the switches and the signals which are selected by the switches are DC signal. Additionally, the resistance of the switches reduces the DC reference fluctuation caused by the external transient noise[10].

3. 3-Stage Cascaded Voting Process

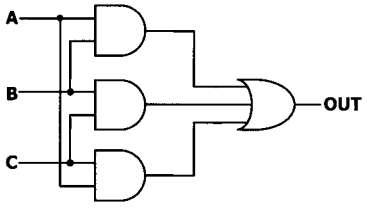
The input offset voltages of the 1st and 2nd preamps and comparators and the occasional meta-stability of comparators may generate bubbles in the thermometer code at the comparator output. Although the conventional 3-input majority voter can remove an isolated bubble, it cannot remove consecutive bubbles. Since the interpolation with a factor of 4 is used at the 2nd preamp output, it may generate consecutive bubbles at the interpolated output even though there is only a single bubble at the 2nd preamp output.

Fig. 5(a) shows the circuits performing the proposed 3-stage cascaded voting process. The voting is performed in three stages by using the conventional 3-input majority voters, shown in Fig. 5(b). The 3-input voter was implemented with static logic gates. The partial thermometer codes ($\cdots, C_{4N+4}, C_{4N}, C_{4N-4}, \cdots$) are the comparator output codes corresponding to the direct outputs from the 2nd preamps. It is assumed that there is only a single bubble at most in these partial codes ($\cdots, C_{4N+4}, C_{4N}, C_{4N-4}, \cdots$). Among the entire thermometer codes ($\cdots, C_{4N+4}, C_{4N+3}, C_{4N+2}, C_{4N+1}, C_{4N}, C_{4N-1}, C_{4N-2}, C_{4N-3}, C_{4N-4}, \cdots$), the above mentioned partial thermometer codes have the largest probability of bubble errors due to the use of interpolation.

Therefore, the codes $\cdots, C_{4N+4}, C_{4N}, C_{4N-4}, \cdots$ are voted first at the 1st stage. This generates the bubble-free codes $\cdots, T_{4N+4}, T_{4N}, T_{4N-4}, \cdots$. After the 1st stage voting, the 2nd stage voting was performed for the corrected codes ($\cdots, T_{4N+4}, T_{4N}, T_{4N-4}, \cdots$) and the interpolated codes ($\cdots, C_{4N+2}, C_{4N-2}, \cdots$) from the mid-point of the interpolation resistor string. This 2nd stage voting generates the bubble-free



(a)



(b)

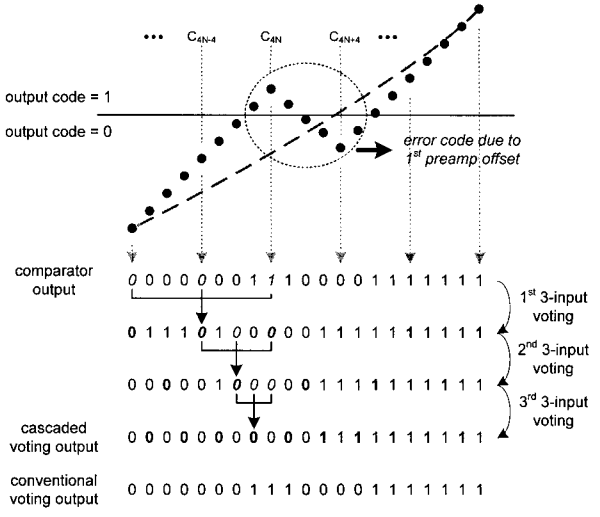
Fig. 5. (a) Cascaded voting process (b) Circuit of the 3-input voter.

codes $\cdots, T_{4N+2}, T_{4N-2}, \cdots$, since the 2 inputs out of 3 inputs of all the 2nd stage voters are bubble-free. Similarly, the 3rd stage voting generates the bubble-free codes $\cdots, T_{4N+3}, T_{4N+1}, T_{4N-1}, T_{4N-3}, \cdots$. Therefore, this 3-stage cascaded voting process eliminates all the bubbles in the resultant codes, as long as there are no consecutive bubbles in the original partial codes ($\cdots, C_{4N+4}, C_{4N}, C_{4N-4}, \cdots$).

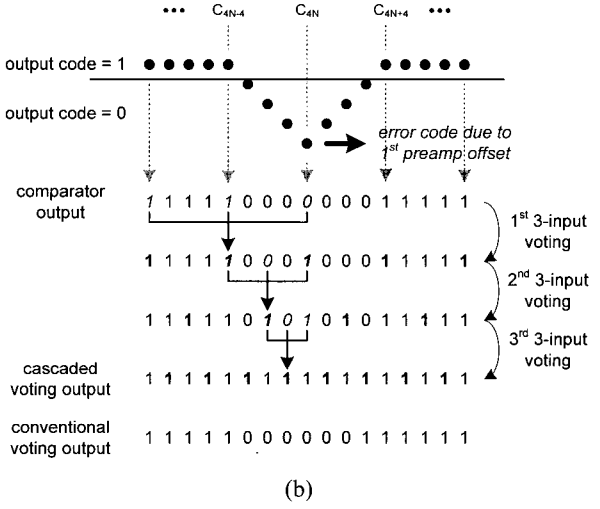
Fig. 6 shows the examples of cascaded voting process. We assumed that there is only a single bubble at most in the partial codes ($\cdots, C_{4N+4}, C_{4N}, C_{4N-4}, \cdots$) of Fig. 5, which are the comparator outputs directly corresponding to the 2nd preamp outputs. In this case, the maximum number of consecutive bubbles in the entire code is seven.

Fig. 6(a) and (b) show the cases of four and seven consecutive bubbles, respectively. The proposed 3-stage cascaded voting process eliminates the bubbles completely.

Since only a single 3-input voter was assigned to each comparator output in the proposed voting scheme, this scheme did not cause any hardware increase compared to the conventional 3-input voting scheme. Although the 5-input voter can eliminate completely up to 2 consecutive bubbles, it has the twice the gate count of the 3-input voter.



(a)



(b)

Fig. 6. Examples of the cascade voting process (a) the voting for the bubbles in the transition region (b) the voting for the maximum votable consecutive bubbles.

However, the cascaded voting can result in increased latency.

III. Measurement Results

To measure the output binary code, the decimation scheme was used at the output of the digital encoder. The decimation block reduces the frequency of the output binary code from 1 GHz to 100 MHz.

Table 1 shows the measured performance summary of the fabricated ADC chip. Fig. 7 shows the chip layout and the chip microphotograph.The active chip area is 1.28 mm^2. Fig. 8 shows the measured DNL and INL plots in LSB

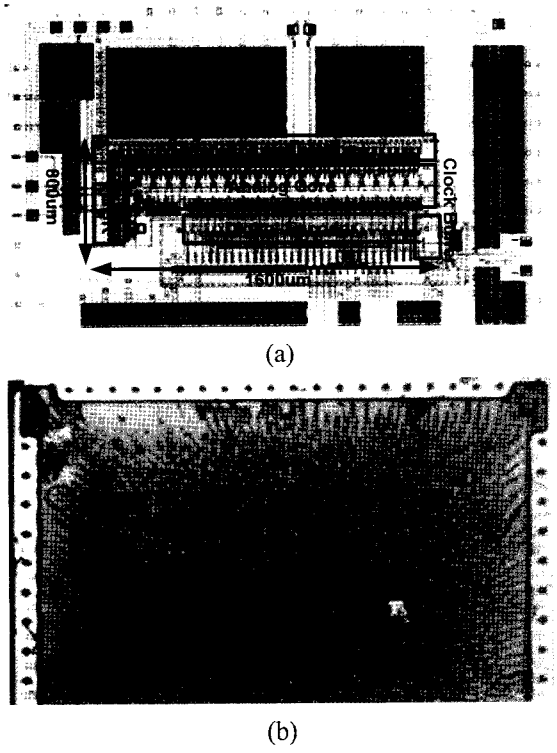


Fig. 7. (a) Chip layout (b) Chip microphotograph.

Table 1. Performance summary (measurements).

Conversion Rate	1 GS/s
Resolution	7-bit
Input Bandwidth	195 MHz
Input Range	400 mV_{P-P}
DNL @ 1 GS/s INL @ 1 GS/s	+0.38/-0.465 LSB, +0.454/-0.474 LSB
SNDR, ENOB @ fin = 195 MHz	37 dB, 5.86 bits @1 Gsample/s
Process	1 P 6 M 0.13-μm CMOS
Supply Voltage	1.2 V
Power Consumption	212 mW
Chip Area	1.28 mm^2 (800 μm × 1600 μm)

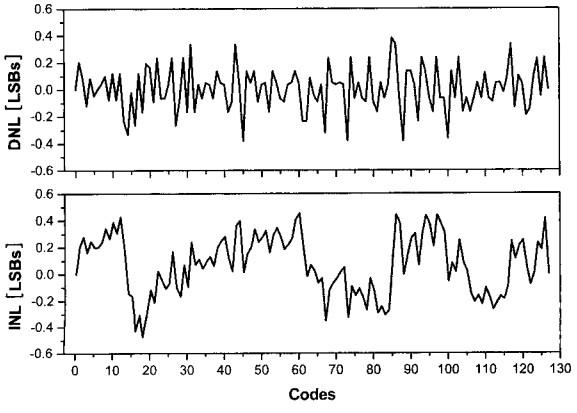


Fig. 8. Measured DNL and INL.

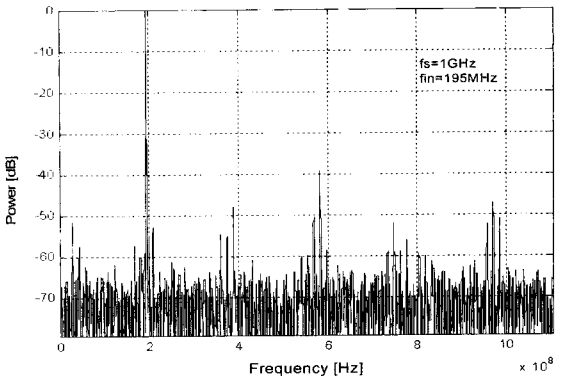


Fig. 9. Measured power spectrum.

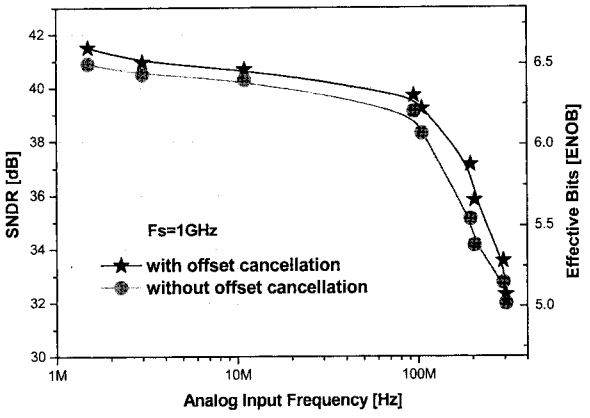


Fig. 10. SNDR versus input frequency at 1 GS/s.

units versus the input code. The maximum DNL and INL are +0.38/-0.465 LSBs and +0.454/-0.474 LSBs, respectively. Fig. 9 shows the power spectrum of the ADC output code at the sampling frequency of 1 GS/s, the supply voltage of 1.2 V, and the 400 mV_{p-p} 195 MHz sine wave input. Fig. 10 shows the measured SNDR versus the analog input frequency at the sampling rate of 1 GS/s, where the digital calibration of reference voltage for offset voltage control enhanced the SNDR from 35.13 dB to 37.14 dB with a 195 MHz 400 mV_{p-p} sine wave input. The power consumption was measured to be 212 mW at the sampling frequency of 1 GS/s.

IV. CONCLUSIONS

A 1.2 V 7-bit 1 GS/s CMOS flash ADC with the interpolation factor of 4 was implemented by using a 0.13 μm CMOS process. The input bandwidth was measured to be 195 MHz at the supply voltage of 1.2 V and the 400 mV_{p-p} sine wave input. ENOB, SNDR, and the power consumption were measured to be 5.88 bits, 37.14 dB, and

212 mW, respectively.

The ADC chip consists of the arrays of the 1st preamp, the distributed track and hold circuit, the 2nd preamp followed by the interpolation network, the comparator, and the digital encoder block.

A digital calibration of DC reference voltage was proposed for the 1st preamp array to reduce the input offset voltage without disturbing the high-speed analog signal path.

A 3-stage cascaded voting process was proposed for the digital encoder block to eliminate the consecutive bubbles generated by the interpolation scheme. The circuit for this voting process consists of the conventional 3-input majority voters. There is no hardware increase in this cascaded voting process compared to the conventional 3-input voting. The consecutive bubbles up to 7 bits can be completely eliminated with the proposed voting process, if the 2nd preamp output is assumed to have a single bubble at most.

ACKNOWLEDGMENTS

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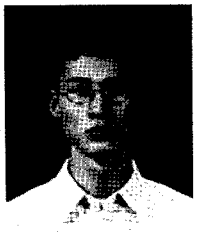

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