A 77 GHz 3-Stage Low Noise Amplifier with Cascode Structure Utilizing Positive Feedback Network using 0.13 μm CMOS Process

Choonghee Lee, Wooyeol Choi, Jihoon Kim, and Youngwoo Kwon

Abstract—**A 77 GHz 3-stage low noise amplifier (LNA) employing one common source and two cascode stages is developed using 0.13 μm CMOS process. To compensate for the low gain which is caused by lossy silicon substrate and parasitic element of CMOS transistor, positive feedback technique using parasitic inductance of bypass capacitor is adopted to cascode stages. The developed LNA shows gain of 7.2 dB, S11 of -16.5 dB and S22 of -19.8 dB at 77 GHz. The return loss bandwidth of LNA is 71.6 to 80.9 GHz (12%). The die size is as small as 0.7 mm × 0.8 mm by using bias line as inter-stage matching networks. This LNA shows possibility of 77 GHz automotive RADAR system using 0.13 μm CMOS process, which has advantage in cost compared to sub-100 nm CMOS process.**

Index Terms—**77 GHz, CMOS, low noise amplifier, positive feedback, macro model, MMIC**

I. INTRODUCTION

LNA monolithic microwave integrated circuits (MMICs) for automotive RADAR system have been implemented by using compound semiconductor processes such as GaAs [1], InP [2] or SiGe [3] due to their higher cutoff frequency and lower thermal noise than CMOS process. However, recent advance in CMOS process has scaled down the channel length of FET's to several tens of nanometer. Due to shortening the channel length of CMOS transistors, the maximum oscillation frequency is increased up to several hundreds giga-hertz [4]. Therefore, the performance of CMOS transistors is becoming comparable to that of compound semiconductor processes. This motivates implementing low cost millimeter-wave circuits like gigabit wireless personal area network (WPAN) [5] and automotive RADAR system [6] by using advanced CMOS processes.

In this paper, three stage CMOS LNA operating at 77 GHz is presented using common source and cascode structure with positive feedback. The first common source stage has lower gain compared to that of the cascode amplifier. However, since the noise performance of the first stage amplifier has a dominant effect on that of the LNA, the common source amplifier, which has superior noise performance compared to cascode amplifier, is utilized for the first stage. In the second and third stage, cascode structure is used for higher gain and isolation. Especially, positive feedback technique is employed at common gate cell of cascode structure, in order to compensate for the low gain due to lossy silicon substrate and parasitic elements of transistor. The size of LNA is as compact as 0.7 mm × 0.8 mm thanks to bias line which also functions as matching stub.

II. TRANSISTOR MODEL

Since the RF transistor model provided by a foundry is valid only up to 30 GHz, modified macro model was developed by applying the method described in [6]. Developed macro model employed additional components for high frequency accuracy. Then the values of the components are extracted from measured s-parameters up

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to 110 GHz. The substrate network, which extracted from measurement of s-parameter and via inductance, is applied to BSIM4 core model. As a result, we achieved macro model similar to measurement. Fig. 1 and Fig. 2 show schematic of macro model and test pattern layout of common source FET utilized in the LNA. Fig. 3(a) shows comparison between s-parameters of the foundry model and measurement of transistor with gate width of 2 × 30 μm. As shown in Fig. 3(a), small signal parameters of the foundry model and measurement are not matched in black dotted region over 30 GHz due to parasitic elements, which are not considered in the foundry model. Fig. 3(b) shows that the s-parameters of the developed macro model have good agreement with the measurement.

Though the macro model showed f_{MAX} of 90 GHz,

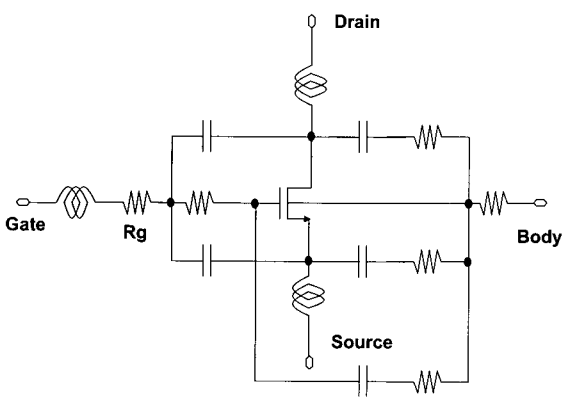


Fig. 1. Schematic of macro model utilized in designing LNA.

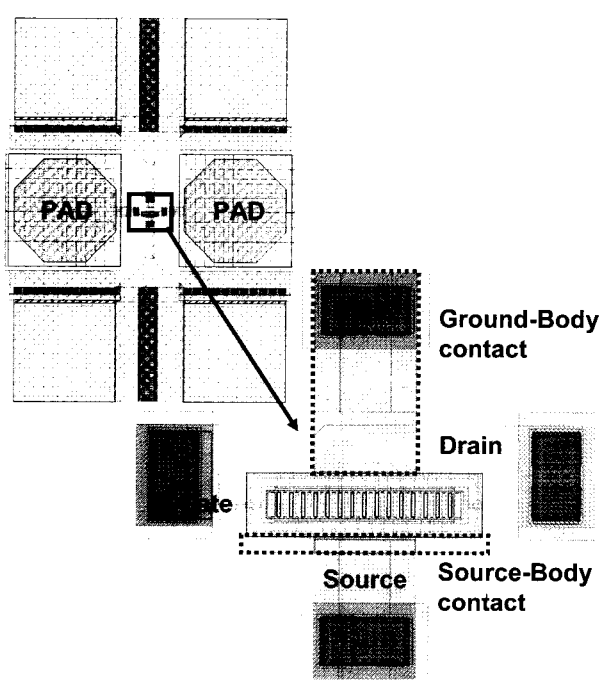
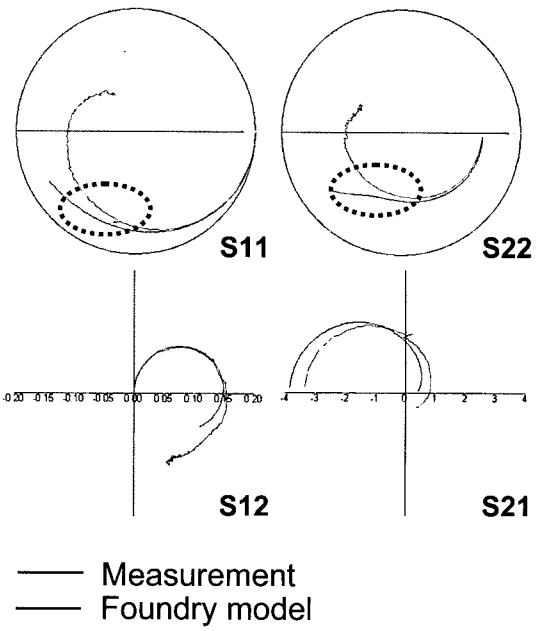
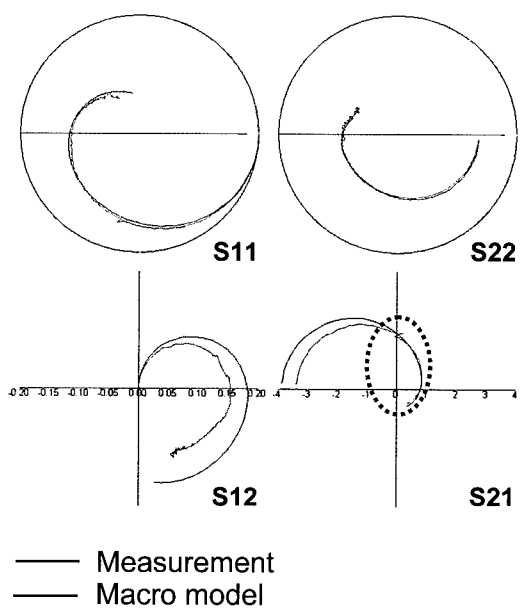


Fig. 2. Test pattern layout of common source FET.



(a)



(b)

Fig. 3. Comparison of the measured s-parameters (a) with foundry model (b) with developed macro model.

which is not sufficient for millimeter-wave circuit, we could overcome this problem applying positive feedback technology to common gate cell of cascode structure.

III. Gain Boosting Circuit with Positive Feedback

Cascode amplifier is preferred due to high gain perfor-

mance and excellent reverse isolation due to reduced Miller effect. However, CMOS process has inherent limitations to realize millimeter-wave circuits. For example, electron mobility of silicon is too low to operate millimeter-wave circuit. Various parasitic elements of CMOS process also cause the gain to become even lower. Furthermore, gain is decreased by lossy silicon substrate. To overcome these problems, cascode amplifier with positive feedback is utilized to implement LNA. Fig. 4 (a) shows conventional common gate amplifier of cascode structure. Voltage gain of conventional common gate amplifier is equation (1) with simple calculation:

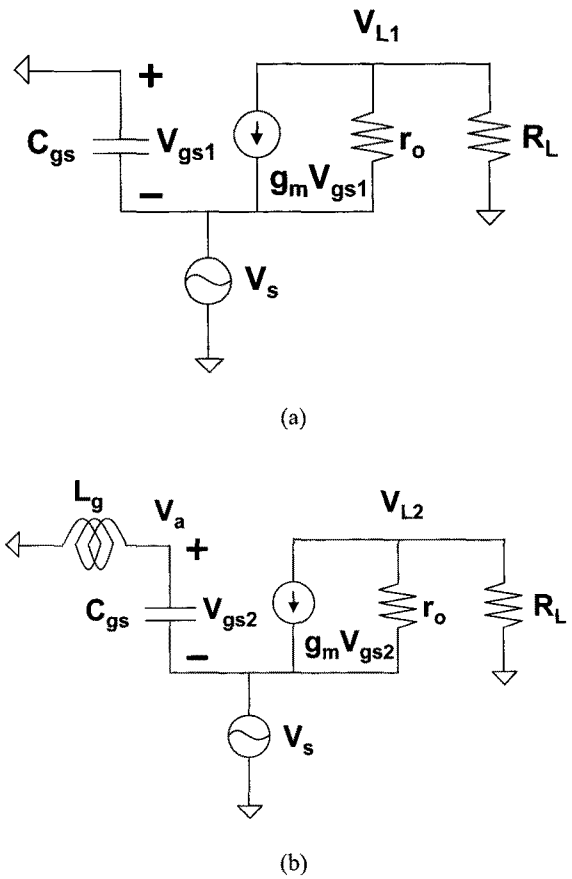


Fig. 4. (a) Small signal modem of conventional common gate amplifier (b) Small signal model of Common gate amplifier with positive feedback.

$$\frac{V_{L1}}{V_s} = (g_m + \frac{1}{r_o})(R_L // r_o) \tag{1}$$

Fig. 4 (b) presents common gate amplifier with positive feedback network. By small signal analysis, we can calculate voltage gain of common gate amplifier adapting positive feedback.

$$\begin{aligned} V_s &= (j\omega L_g + \frac{1}{j\omega C_{gs}})(-j\omega C_{gs} \times V_{gs}) \\ &= -(1 - \omega^2 L_g C_{gs}) V_{gs} \end{aligned} \tag{2}$$

$$\frac{V_s - V_{L2}}{r_o} = g_m V_{gs2} + \frac{V_{L2}}{R_L} \tag{3}$$

$$\therefore \frac{V_{L2}}{V_s} = (\frac{g_m}{1 - \omega^2 L_g C_{gs}} + \frac{1}{r_o})(R_L // r_o) \tag{4}$$

$$V_a = -\frac{\omega^2 L_g C_{gs}}{1 - \omega^2 L_g C_{gs}} V_s \tag{5}$$

Under the condition that operating frequency of common gate amplifier is lower than $1/\sqrt{L_g C_{gs}}$, small signal gain is boosted to be higher than one of conventional common gate amplifier. This can be verified by comparing equation (1) with (4). The main reason of the gain boosting is the effective increase of the trans-conductance. This can be explained in equation (5). When the operating frequency is lower than $1/\sqrt{L_g C_{gs}}$, in equation (5), node voltages V_a and V_s are out of phase. Therefore, amplitude of V_{gs2} is effectively larger compared to that of V_{gs1}.

IV. MMIC DESIGN

Fig. 5 shows that schematic of the LNA. This LNA is composed of single common source stage and two cascode stages, which have positive feedback for gain boosting. The first stage was configured by common source topology for low noise figure. The second and third stages are consisted of cascode amplifiers with positive

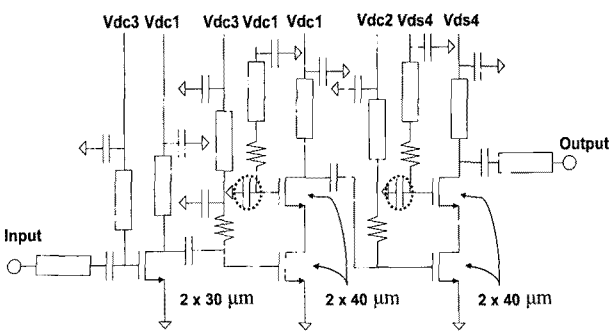


Fig. 5. Schematic of proposed LNA, larger capacitor than 77 GHz bypass capacitance in blue dotted circle.

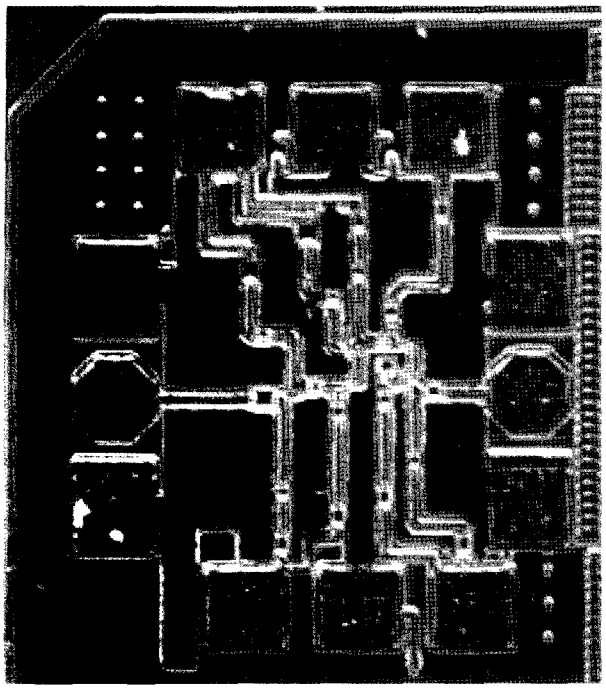
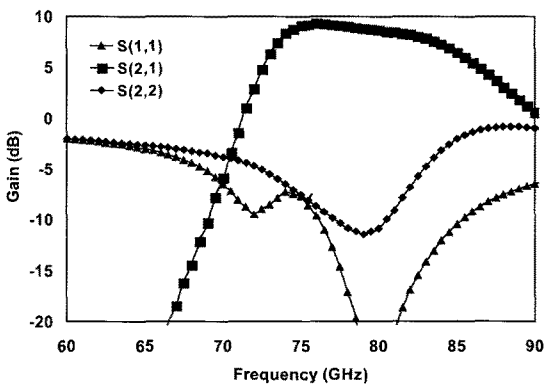


Fig. 6. Photograph of fabricated LNA.

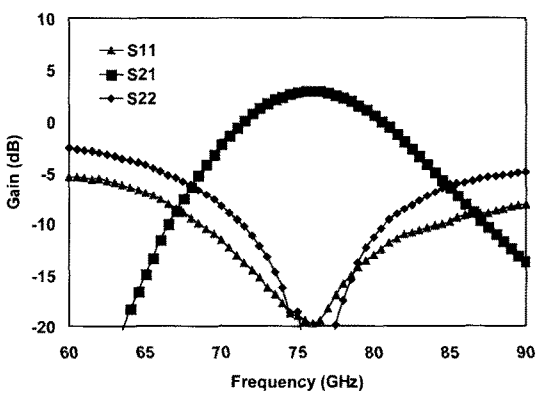
feedback network for high gain. A parasitic inductance of the bypass capacitor, which is in front of common gate amplifier, gives positive feedback to the cascode amplifiers. The value of the bypass capacitors are chosen to be 0.5 pF, which is larger than what is normally utilized as 77 GHz bypass capacitance. This effectively increases transconductance of transistor by making V_{gs} boosted compared to that of conventional common gate amplifier. Hence, positive feedback network compensates for the low gain caused by lossy silicon substrate and parasitic elements of transistor. Fig. 6 shows the photograph of fabricated LNA. The size of die is as compact as 0.7 mm × 0.8 mm thanks to bias lines as matching stub.

V. Measurement Results

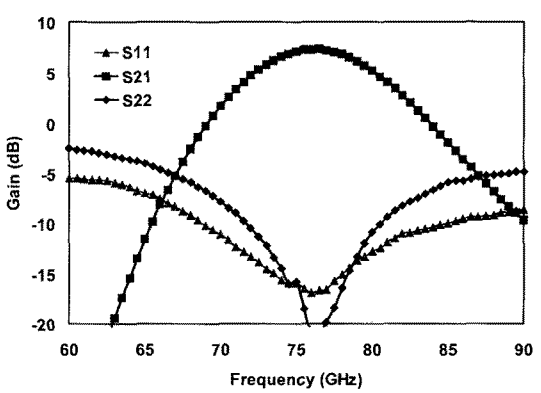
Fig. 7 (a) shows that simulated results of implemented LNA under normal bias condition. The gate of the first common source stage was biased at 0.8 V and the drain of the first common source stage was biased at 1.5 V. Both the gates of common source amplifier of cascode stages were biased at 0.8 V and the gates and the drains of common gate amplifier of cascode stages were 1.5V. Simulated result achieved gain of 9.2 dB, S11 of -12.7 dB and S22 of -10.3 dB at 77 GHz. Drain current corresponded between simulation and fabricated circuit. The Drain currents of common source and cascode amplifiers are 14 mA and 17 mA relatively. Fig. 7 (b) shows measured result under same bias condition as simulation. Under this bias condition, fabricated LNA has gain of 2.8 dB, S11 of -18.2 dB and S22 of -23.4 dB. Fig. 7 (c) demonstrates result of maximal gain. Under this bias condition, This LNA shows gain of 7.2 dB, S11 of -16.5 dB and S22 of -19.8 dB. Maximal bias point at the first stage is 1.5 V for gate and 3.5 V for drain. At cascode stage, gate bias of



(a)



(b)



(c)

Fig. 7. Measured S-parameter graphs (a) Simulation result under normal bias point (b) Normal bias point measurement result (c) Maximum gain bias point measurement result.

common source amplifier was 1.5 V. 3.5 V was applied for both gate and drain of common gate amplifier in cascode structure. Drain current of the first stage was 17 mA and that of cascode amplifier is equal to 22 mA.

VI. CONCLUSIONS

A 77 GHz three-stage LNA with positive feedback network is fabricated using 0.13 μm CMOS process that costs lower than sub 100 nm CMOS processes. This LNA has maximum gain 7.2 dB at 77 GHz, 8 GHz bandwidth. The die size of LNA is 0.7 mm × 0.8 mm. The LNA in this work can be applied to inexpensive automotive RADAR system due to relatively lower cost than that of compound semiconductor processes or sub-100 nm CMOS processes.

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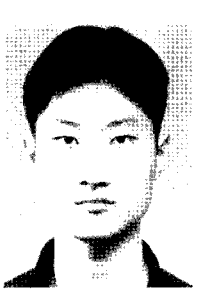

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