Post-Linearization of Differential CMOS Low Noise Amplifier Using Cross-Coupled FETs

Tae-Sung Kim*, Seong-Kyun Kim*, Jin-Sung Park, and Byung-Sung Kim***

***Abstract*—A post-linearization technique for the differential CMOS LNA is presented. The proposed method uses an additional cross-coupled common-source FET pair to cancel out the third-order intermodulation (IM_3) current of the main differential amplifier. This technique is applied to enhance the linearity of CMOS LNA using 0.18-μm technology. The LNA achieved +10.2 dBm IIP3 with 13.7 dB gain and 1.68 dB NF at 2 GHz consuming 11.8 mA from a 1.8-V supply. It shows IIP3 improvement by 6.6 dB over the conventional cascode LNA without the linearizing circuit.**

***Index Terms*—Complementary metal oxide semiconductor (CMOS), intermodulation distortion (IMD), low noise amplifier (LNA), post-linearization**

I. INTRODUCTION

The advanced scaling of CMOS technology enables us to design low noise, high gain amplifiers with low power consumption. However, the linearity of CMOS is getting worse as the process scales down [1], which has motivated several linearization techniques. Until now, the most efficient reported linearization method for CMOS LNA is the derivative superposition [or multiple gated transistor (MGTR)] technique [2-4] which nulls the negative 3rd-order derivative of the dc transfer characteristic (g_3) of the main FET by paralleling the auxiliary FET biased near the weak inversion region with the positive g_3. Despite the outstanding improvements in the linearity, the DS methods have difficulties in controlling the quality factor (Q) of the input matching network which plays a key role for low noise optimization [5,6]. Recently, post-linearization (PL) techniques have been reported where the control voltage of the IM_3 generator is adopted from the output node of the common source FET [7,8]. However, they accompany the slight gain reduction due to the fundamental current leakage through the linearization circuit.

In this paper, we present a post-linearization technique for differential CMOS LNA using cross-coupled post-linearization (CCPL) method [9]. In our approach, the noise performance of the CMOS LNA can be optimized independently and IM_3 currents generated by the LNA are cancelled out by the cross-coupled post distortion canceller (CCPDC). In the following, a simple analysis is given to explain how the linearization is achieved using CCPL technique. Finally, experimental results using 0.18-μm CMOS technology will be presented.

II. THEORY OF CROSS-COUPLED POST-LINEARIZATION METHOD

The drain current i_d of FET can be expressed in terms of the gate-source voltage v_{gs} around the operating bias point using the power-series expansion

$$i_d = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \cdots, \quad (1)$$

where g_i is the i_{th}-order derivative of the dc transfer characteristic. The 3rd-order derivative g_3 in (1) is a major source of IM_3 which restricts the linearity of an amplifier. In a typical LNA design, the bias point of the CS FET for low noise and high gain operation is selected in strong inversion region but below the edge of velocity saturation region, where the third order nonlinear coefficient has the

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negative value around the peak. Therefore, improvement of the linearity can be obtained by adding an additional sub-circuit which generates the positive third-order nonlinearity to cancel the negative 3rd-order nonlinearity of the main amplifier. In Fig. 1, FET M_A and M_B compose the differential amplifier which has the negative 3rd-order derivative, and M_C forms an auxiliary amplifier to remove the IM_3 generated by M_A [4]. M_C is biased in weak inversion region which has the positive g_3 to cancel the IM_3 of M_A. This linearization technique is called as DS (or MGTR) technique [2-4]. The DS method achieves the improvement of the linearity with a slight gain increase because the auxiliary amplifier operates in parallel with the main amplifier and its fundamental output current has the same phase with the main amplifier. However, it is difficult to perform a low noise optimization for the DS technique due to the difficulty in controlling the input quality factor, which is mainly determined by the device match for nulling the third order nonlinearity between the main and auxiliary FETs. Additionally, the auxiliary FET operating in weak inversion region is noisier than the main FET [3].

In the post-linearization structure shown in Fig. 1, the output drain voltage of the CS FET M_B has the same phase with the input voltage of M_A. Therefore, the cross-coupled FET M_D can replace the FET M_C of the DS method and cancel the IM_3 current of the main FET M_A. Then the input of the main amplifier composed of M_A and M_B is free from any loading caused by the linearization circuitry and can be optimized for low noise design apart from the linearization design. Fig. 2(a) shows a simple schematic of the proposed differential amplifier to explain the post-linearization method in detail. M_A, M_B, M_C, and M_D compose a conventional cascode differential amplifier and M_E and M_F form the CCPDC which generates the

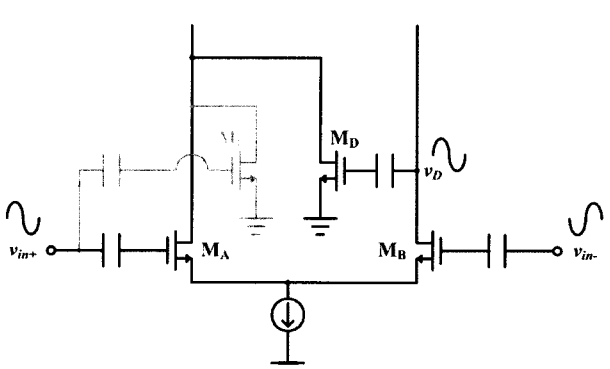
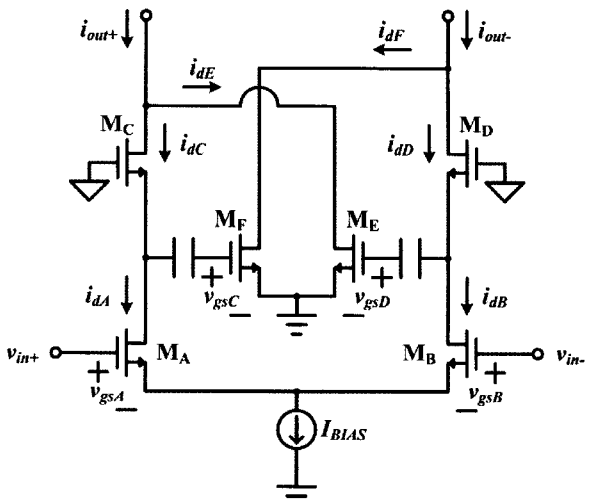
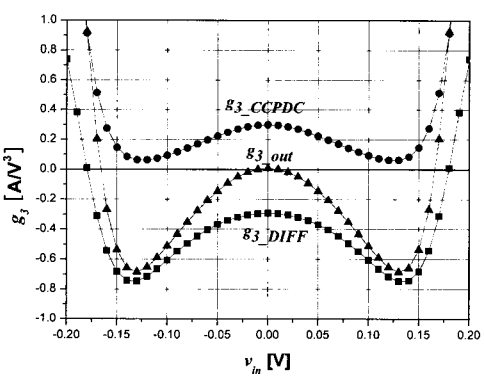


Fig. 1. Simple schematic of CCPL method.



(a)



(b)

Fig. 2. Differential amplifier with CCPL method. (a) Schematic. (b) 3rd-order power series coefficients of output current at DC.

nonlinear current to cancel out the IM_3 by the main differential amplifier. In the following analysis to explain the linearization principle, reactive components are ignored and the common-gate (CG) FETs, M_C and M_D, are assumed to work as linear current buffers. In addition, we assume that the output impedance of the tail current source is infinite and all pairs have no mismatches. Then the drain current of each FET can be expressed into the power-series with a gate-source voltage of FET respectively. For simplicity, the output current i_{out+} of the left half circuit composed of M_A, M_C, and M_E is considered. The drain current of M_A and M_B are expanded at a given bias current

$$i_{dA} = i_{dC} = g_{1A}v_{gsA} + g_{2A}v_{gsA}^2 + g_{3A}v_{gsA}^3, \quad (2)$$

$$i_{dB} = i_{dD} = g_{1B}v_{gsB} + g_{2B}v_{gsB}^2 + g_{3B}v_{gsB}^3. \quad (3)$$

The 2nd-order terms in (2) and (3) are common mode currents, but the ideal current source does not allow the common mode current. Therefore, the gate-source voltage v_{gsA} and v_{gsB} will be self-adjusted to compensate the common mode current and finally the resulting output currents of M_A and M_B are expected to have the fundamental and third order terms of the input voltage v_{in}.

$$i_{dA} = i_{dC} = g_{1A}\left(\frac{v_{in}}{2}\right) + g_{3A}\left(\frac{v_{in}}{2}\right)^3, \tag{4}$$

$$i_{dB} = i_{dD} = -i_{dA}, \tag{5}$$

$$i_{dE} = g_{1E}v_{gsE} + g_{2E}v_{gsE}^2 + g_{3E}v_{gsE}^3. \tag{6}$$

Ignoring the higher order terms, v_{gsE} in (6) can be approximated by

$$v_{gsE} \approx -\frac{i_{dB}}{g_{1D}}. \tag{7}$$

Assuming the perfect match of the differential pair (g_{iA}=g_{iB}), the output current i_{out+} using (2)-(7)

$$\begin{aligned} i_{out+} &= i_{dC} + i_{dE} \\ &= \left(g_{1A} + g_{1E}\right)\frac{v_{in}}{2} + g_{2E}\cdot\left(\frac{v_{in}}{2}\right)^2 \\ &+ \left(g_{3A} + g_{3E} + \frac{g_{1E}\cdot g_{3B}}{g_{1D}}\right)\cdot\left(\frac{v_{in}}{2}\right)^3. \end{aligned} \tag{8}$$

In (8), it is noticeable that the transconductance g_{1E} of the FET M_E is added to the main transconductance, while the previous PL methods in [7,8] reduce the fundamental gain. The third term in the last parenthesis of (8) represents the 3rd-order nonlinear current generated by CS FET M_B and amplified by M_E, but it is much smaller than the first term because g_{1E} is much less than g_{1D}. Therefore, the final output current i_{out} can be approximated as follows,

$$\begin{aligned} i_{out} &= i_{out+} - i_{out-} \\ &\approx 2\left(g_{1A} + g_{1E}\right)\frac{v_{in}}{2} + 2\left(g_{3A} + g_{3E}\right)\left(\frac{v_{in}}{2}\right)^3. \end{aligned} \tag{9}$$

The optimum size and bias point of the CMOS FET for low noise and low power operation yield the negative 3rd-order nonlinear coefficient. Therefore, the 3rd-order nonlinearity provided by CCPDC FET should be positive, which requires the bias of the FET M_E in the weak inversion region. The above analysis can be confirmed by simulation results shown in Fig. 2(b), where g_{3_diff}, g_{3_CCPDC} and g_{3_out} are the 3rd-order nonlinear coefficients of the main differential pair, CCPDC FET and i_{out} in (9) respectively.

It is found that the 3rd-order nonlinearity g_{3_diff} of the main differential amplifier can be cancelled out by g_{3_CCPDC} which is generated by CCPDC. As a result, at low frequencies the 3rd-order nonlinearity component can be cancelled around the operating point as shown in Fig. 2(b). At RF frequencies, the IM_3 is partially cancelled because an additional IM_3 is generated in the main differential pair due to the effects of the 2nd-order nonlinearity and feedback through the degeneration inductor [3]. However, a noticeable improvement can be obtained by just making g_3 zero as explained in [7]. Additionally, there may exist a secondary IM_3 due to the feedback through the gate-drain capacitance of the FET M_E in the CCPDC at RF. It can be investigated using the following relation [10]

$$\varepsilon\left(\Delta\omega, 2\omega\right) = g_3 - \frac{2g_2^2}{3}\left[\frac{2}{g_1 + g\left(\Delta\omega\right)} + \frac{1}{g_1 + g\left(2\omega\right)}\right], \tag{10}$$

$$g(\omega) = \frac{j\omega C_{gd}Z_S(\omega) + \left[1 + j\omega C_{gs}Z_S(\omega)\right]\left[1 + j\omega C_{gd}Z_L(\omega)\right]}{j\omega C_{gd}Z_S(\omega)Z_L(\omega)}. \tag{11}$$

where g_3 is g_{3E} in (9), and $Z_S(\omega)$ is the source impedance of CCPDC that can be substituted by $1/g_{1c}$ which normally has low impedance. $Z_L(\omega)$ is the load impedance that exhibits high impedance in the operation frequency, whereas it is low at out-of-band in a typical high-frequency amplifier. Because of the characteristics of the source and resonant load impedance, the second term in (10) due to the 2nd-order nonlinearity and feedback through the gate-drain capacitance is much smaller than g_3. Therefore the combined effects of the 2nd-order nonlinearity and feedback in the CCPDC can be neglected and then linearization using CCPDC can be effective at high frequency operation.

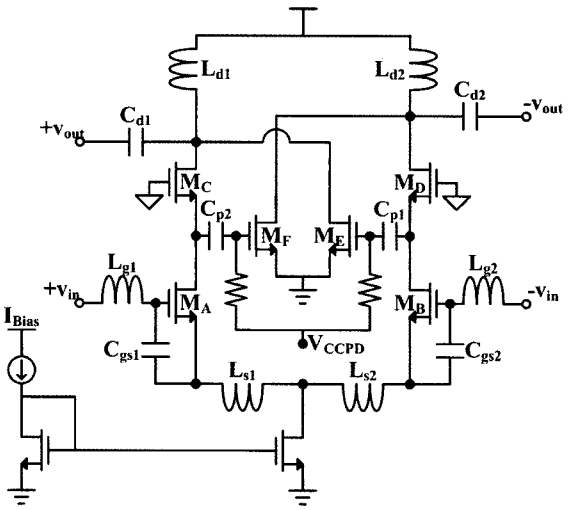
In the DS method, the linearization circuit directly affects the noise of the LNA because the auxiliary FET shares the input with the main FET. In [3], it is reported that the induced gate noise of the auxiliary FET rapidly degrades the noise figure of the LNA as the gate bias falls below the threshold voltage. On the other hand, in the proposed post-linearization technique, the linearization

circuit takes the control signal at the output node of the main FET, the noise performance is optimized through the optimum Q control of the input matching circuit according to the methods in [5,6]. Therefore, a better noise performance is expected in the post-linearization techniques. However, even for the post-linearization techniques, the previous implementation for the single ended LNAs as in [7,8] degrades the noise figure due to the reduction of the gain caused by the leakage of the fundamental current to the linearization circuit. For the differential LNA, direct application of the previous post-linearization techniques is not effective due to the gain reduction. The proposed CCPDC approach will show the better noise performance than not only the DS method but also the previous post-linearization techniques.

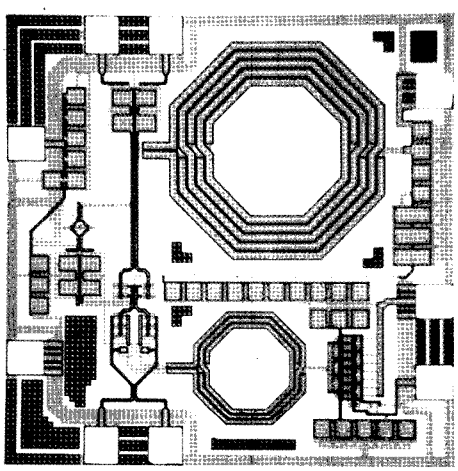
III. LNA Design and Experimental Results

The CMOS differential LNA using CCPL in Fig. 3 is designed and fabricated. Design guidelines are as follows: At first, the sizes of the CS FET and C_{gsi} are optimized considering the noise and bias current [5,6]. Then the size and bias point of the CCPDC FET are determined to cancel out the IM_3 currents that are generated by the main differential amplifier. Though the complete cancellation is not possible as explained in the previous section, the magnitude and phase match of IM_3s between the main amplifier and the CCPDC can be improved by adjusting the size and bias of CCPDC FET and the coupling capacitance of C_{pi}. Therefore, the optimum size and bias of CCPDC FET are different from those obtained from the dc simulation. The designed LNA was manufactured in a 0.18-μm TSMC RF CMOS process as shown in Fig. 3 (b) and tested in a chip-on-board (COB) form. All pads are electrostatic discharge (ESD) protected.

S-parameters were measured using 4-port VNA, and then 4-port data is converted to differential data. The differential input return loss is less than -10 dB with respect to 100 Ω as shown in Fig. 4. However, the output return loss is poor because the output matching is not made and directly connected to 50 Ω, which causes the broadening of the bandwidth and the deviation of the peak gain frequency. Noise figure and IIP_3 were measured using a ring hybrid. As indicated in the previous section, degradation of noise performance is negligible compared with the conventional



(a)



(b)

Fig. 3. LNA using CCPL method. (a) Schematic. (b) Microphotograph.

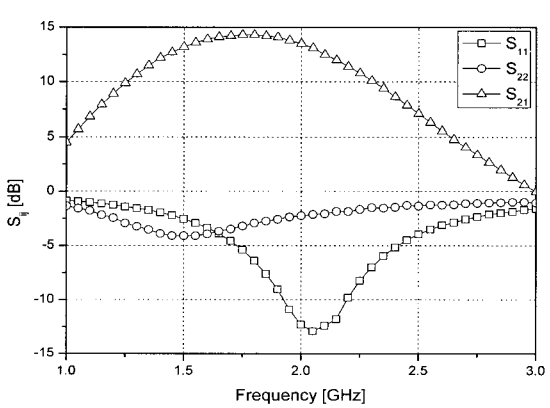


Fig. 4. S-parameter measurement results.

LNA operation with turning off the CCPDC. Table 1 summarizes the measured results. The IIP3 was improved by 6.6 dB and noise figure was degraded by 0.03 dB over.

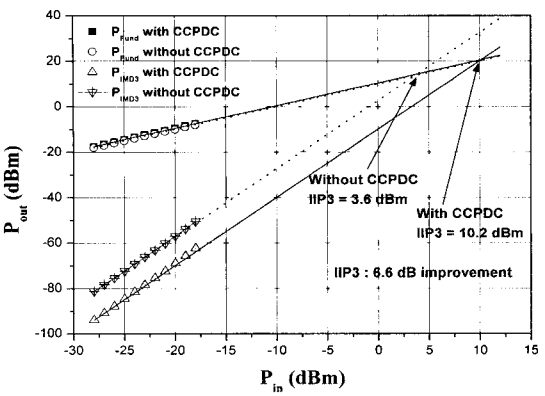


Fig. 5. 2-tone test results measured at 1.9995 GHz and 2.0005 GHz.

Table 1. Summary of Measured Results at 2 GHz.

	LNA using CCPL	Conventional LNA
Gain	13.7 dB	13.4 dB
NF	1.68 dB	1.65 dB
IIP3	10.2 dBm	3.6 dBm
I_{DC} @ 1.8 V	11.8 mA	11.2 mA

the simple LNA with turning off the CCPDC and the gain is slightly improved.

IV. CONCLUSIONS

We have proposed a new post-linearization technique for the CMOS differential LNA adopting a cross-coupled MOS pair biased at weak inversion region as a post-distortion canceller. The proposed technique enables the simultaneous optimization of low noise and high linear operation without a gain reduction, which is experimentally confirmed by the good noise performance and linearity improvement. The noise figure of the LNA with the CCPDC is almost same and the linearity is improved by 6.6dB consuming the similar power compared with the normal LNA operation.

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