

A 3-5 GHz Non-Coherent IR-UWB Receiver

Min Cheol Ha*, Young Jin Park**, and Yun Seong Eo*

Abstract—A fully integrated inductorless CMOS impulse radio ultra-wideband (IR-UWB) receiver is implemented using 0.18 μm CMOS technology for 3-5 GHz application. The UWB receiver adopts the non-coherent architecture, which removes the complexity of RF architecture and reduces power consumption. The receiver consists of inductorless differential three stage LNA, envelope detector, variable gain amplifier (VGA), and comparator. The measured sensitivity is -70 dBm in the condition of 5 Mbps and BER of 10⁻³. The receiver chip size is only 1.8 mm × 0.9 mm. The consumed current is 15 mA with 1.8 V supply.

Index Terms—Impulse radio UWB, CMOS receiver, LNA, non-coherent receiver, wideband

I. INTRODUCTION

Up to now, ultra wide band (UWB) system has been paid much more attention to for both high rate and low rate wireless applications. When compared with other narrow band wireless systems, the UWB system can occupy very wide signal bandwidth more than 500 MHz. The recent developments and designs of UWB systems can be classified into IR (impulse radio) and OFDM (orthogonal frequency division multiplexing) based systems. Whereas the OFDM based UWB system is suitable to high data rate communication, the IR-UWB is adequate solution for low rate and low power applications such as sensor networks. As for IR-UWB receiver, the coherent and non-coherent architectures have been reported in the literature [1-3].

The former needs many timing synchronization circuit blocks, which increases system complexity. However, the non-coherent receiver needs simpler architecture and can be operated with smaller current consumption [1,2].

The available frequency band of UWB is allocated as shown in Fig. 1. As seen from Fig. 1, 3.1~10.6 GHz band can be used except 5-6 GHz ISM band assigned for WLAN applications. Therefore, the overall bands are composed of 3.1~5 GHz lower band and 6~10.6 GHz higher band.

In this paper, an IR-UWB based non-coherent single chip CMOS receiver is presented. The receiver only covers 3.1~5 GHz that is the lower frequency band of UWB system.

The on chip receiver is implemented using 0.18 μm CMOS technology. In order to reduce chip size, there is no on-chip inductor, whereas active loads are used for LNA load. Moreover, the current consumption is optimized and minimized for low cost and low power receiver.

II. RECEIVER ARCHITECTURE

Fig. 2 shows the overall architecture of the designed differential CMOS IR-UWB receiver. The received UWB signal is amplified through 3-stage differential LNA, and the carrier is removed and impulse envelope is extracted at

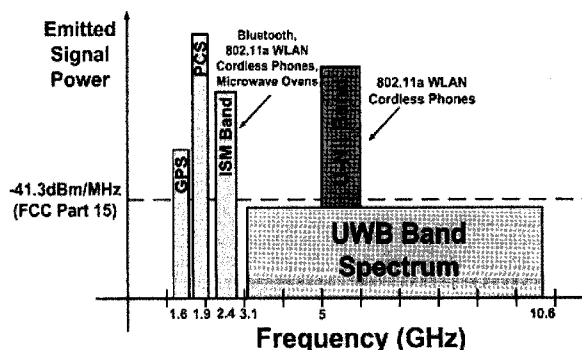


Fig. 1. The allocated UWB spectrum.

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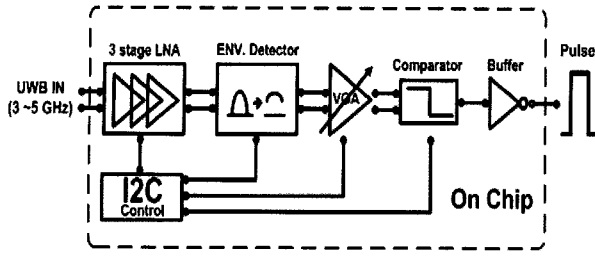


Fig. 2. The overall architecture of designed IR-UWB receiver.

the envelope detector circuit. The following stage is a single stage VGA, which amplifies signal level adaptively to achieve sufficient dynamic range. And finally the comparator outputs digital pulse data whenever the magnitude of impulse envelope exceeds the externally controllable threshold voltage level.

In order to calculate the overall link budget, it is assumed that EIRP (Effective Isotropically Radiated Power) is under -41.3 dBm/MHz regulated by FCC.

Therefore, at maximum -8.3 dBm can be radiated from transmitter within 2 GHz bandwidth. If the target distance is 10 m and antenna gain is 0 dBi, then the path loss can be calculated as following.

$$10 \log (4\pi f_c / c) + 20 \log (10) = 64.5 \text{ dB} \quad (1)$$

Therefore, at the 10 m distance away, the sensitivity of receiver has to be lower than -72.8 dBm. Because the input thermal noise power is -81 dBm within 2 GHz bandwidth and the required SNR for BER 10^{-3} is -9 dB, the target noise figure of receiver is lower than 17 dB, which is easily achieved with CMOS technology. The gain of 3-stage LNA is around 30 dB and the sensitivity of envelope detector is about -42 dBm.

III. UWB RECEIVER CIRCUIT DESIGNS

1. Low Noise Amplifier (LNA) Design

The schematic of fully differential inductorless LNA is shown in the Fig. 3. The input impedance of LNA is matched to 100 ohm, the impedance of external balun. The shunt feedback resistance R_f that is added to conventional differential source degenerated topology provides 3-5 GHz wideband input matching and gain at the cost of some degradation of noise figure and gain [4].

The source degeneration inductors are realized with bond wires whose value is 0.7 nH approximately. The

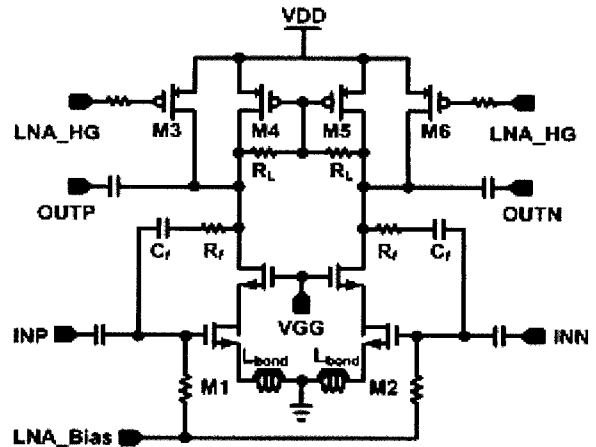


Fig. 3. Designed differential LNA topology.

transistor M4 and M5 are parts of active load and the small signal equivalent load resistance becomes $R_L || r_{o5}$. Using active load, inductorless LNA is possible in spite of some gain loss. However, the noise figure degradation is negligible. The M3 and M6 are load impedance switch transistors that changes LNA gain mode from high gain to low gain. Fig. 4 shows the simulated noise figure of the 3-stage LNA over the band. The simulated NF is lower than 3.5 dB up to 5 GHz.

2. Envelope Detector Design

Fig. 5 shows circuit schematic of designed envelope detector whose minimum detectable pulse signal amplitude dominantly determines the receiver's sensitivity. The output load of envelope detection circuit is an active load with parallel R_f resistors, which independently controls the load impedance free from output node DC bias. The detected envelope is amplified once again at the final stage and RF frequency components are filtered out by the

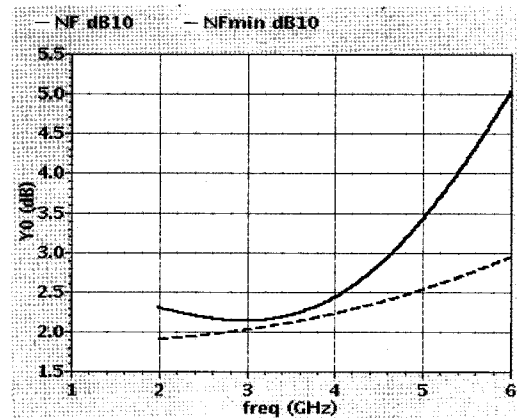


Fig. 4. The simulated results of LNA noise figure.

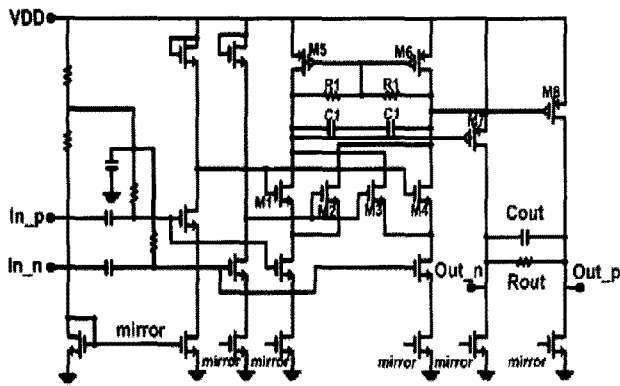


Fig. 5. The circuit schematic of designed envelope detector.

low pass filter composed of R_{out} and C_{out} . The simulated results show that the minimum detectable input envelope voltage is below 10 mVpp or less, which satisfies the required detector's sensitivity.

3. VGA (Variable Gain Amplifier) Design

Fig. 6 shows the topology of designed VGA. The proposed VGA is to obtain high gain and sufficient variable gain range so that the total receiver achieves the desired dynamic range. The VGA core adopts a differential cascode scheme, but M1 and M2 operate in triode region in order to control gain linearly with control bias V_{cont} [5]. Because M1 and M2 are biased at triode region, the transconductance g_m of M1 and M2 is proportional to the drain-source voltage V_{DS1} and V_{DS2} , which is equal to $V_{cont} - V_t - V_{DS9}$, where V_t is the threshold voltage. Since the VGA gain is approximately $g_m r_{o5}$, the gain can be linearly controlled by changing the input gate voltage of M3 and M4. Therefore, both gain control and DC bias for M1 and

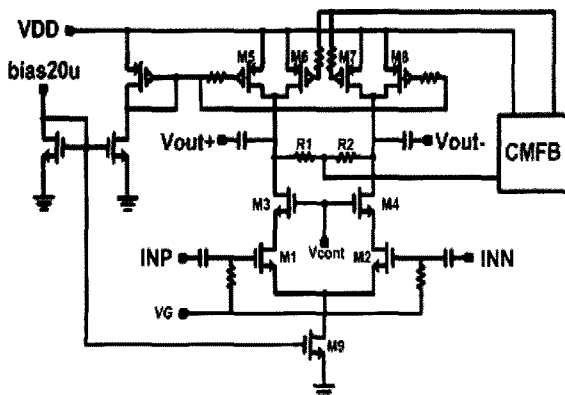


Fig. 6. The circuit schematic of designed VGA.

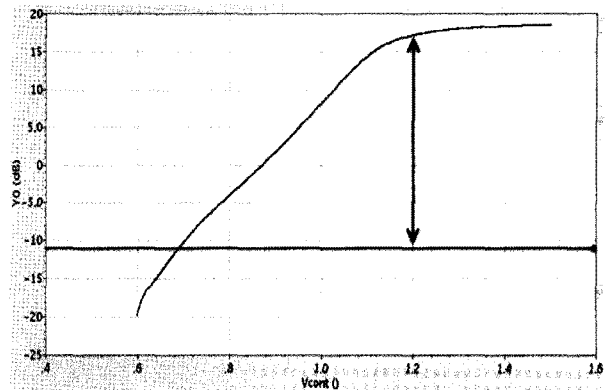


Fig. 7. The gain dynamic range of VGA.

M2 are achieved by trimming V_{cont} . Moreover, a constant current bias is used for linearity and wideband performance regardless of control voltage. The active load consists of PMOS transistors M5-M8. The resistors R_1 and R_2 sense common mode voltage at the output nodes and it is compared with a reference voltage and then common mode feedback (CMFB) circuit can stabilize the output common mode voltage by adaptively controlling the current of M6 and M7, which in turn causes the change of V_{DS5} and V_{DS8} . Fig. 7 shows the gain dynamic range of VGA with control voltage from 0.6 V to 1.5 V and about 36 dB can be controlled with only single stage VGA.

4. Comparator Circuit Design

As a final stage, the comparator consists of differential amplifier (or limiter) and buffering inverter. The envelope signal is applied to the positive input port and compared with the controllable reference threshold voltage at the negative input. Moreover, because the overall gain of two stage amplifier is much higher, the digital pulse signal with some duration time is generated at the output node, whenever the amplitude of input pulse signal is highly peaked enough to invoke the comparator output. The duration time of output digital pulse can also be tuned by threshold voltage control.

IV. MEASUREMENT RESULTS

The IR-UWB receiver is composed of 3-stage LNA, envelope detector, VGA, and comparator, and fabricated on a chip using 0.18 μm CMOS technology.

Because only 3-stage LNA is not sufficient, an external LNA is used additionally to increase the receiver gain.

The measurement results show the return loss of receiver chip is under -10 dB and around 30 dB gain in 3~5 GHz range. And the noise figure is about 3.5 dB. Fig. 8 shows the output voltage of envelope detector and differential signal represents the carrier removed pulse envelope signal. The VGA gain can be varied in the range of -20 ~ +16 dB while controlling V_{cont} from 0.6 to 1.2 V. Beyond 1.2 V, the gain is saturated and not increased any more.

Fig. 9 presents the measured output voltage of comparator circuit whose pulse width is 50 ns and can be tuned with control threshold voltage of comparator. There is additional buffer at the output of comparator circuit and helps receiver drive properly.

The sensitivity is measured with help of assistance of digital modem board. The pre-designed and fabricated transmitter is used for measurement and the attenuator is connected between transmitter output and receiver input. Once the power of transmitter is known, the received power can be calculated by means of attenuator loss. The measured sensitivity for BER 10^{-3} is -70 dBm on condition

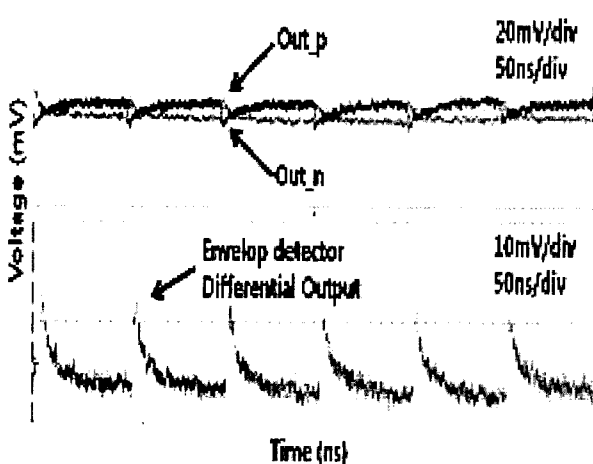


Fig. 8. The measured pulse trace at the output of envelope detector.

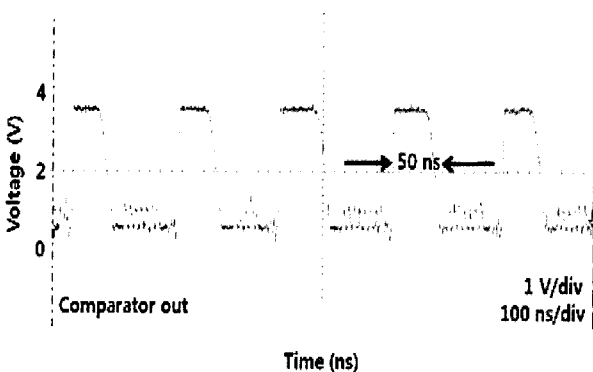


Fig. 9. The resultant pulse output of the comparator.

Table 1. The summary of the measured results of UWB Receiver.

| Parameter | Results |
|--|--------------|
| BW [GHz] | 3.1-5.1 |
| Rx noise Figure (Rx Front-end) | < 3 dB |
| Front-end Gain (MAX) | 30 dB |
| VGA Gain (MAX) | 16 dB |
| VGA Gain Range | 36 dBm |
| Sensitivity @ data rate 5Mbps | -70 dBm |
| Rx Power consumption @ excluding external LNAs | 1.8V @ 15 mA |
| Pulse width | 50 ns |

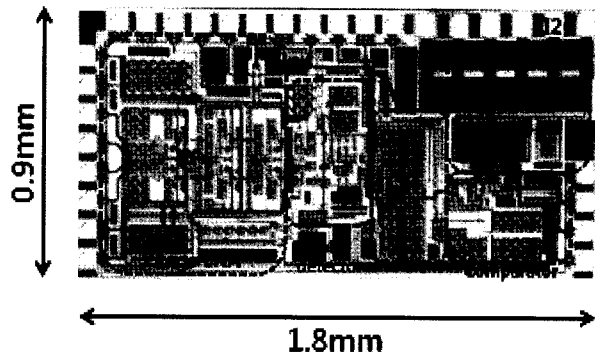


Fig. 10. The microphotograph of fabricated IR-UWB receiver.

that the data rate of transmitted signal is 5 Mbps. The current consumption is 15 mA at 1.8 V supply.

Table 1 below summarizes the overall performance of our inductorless differential IR-UWB single chip receiver.

Fig. 10 shows the microphotograph of the fabricated CMOS single chip receiver. The chip design removes large sized on-chip inductor and shows the feasibility of small sized fully integrated inductorless receiver. The size of receiver is only 1.8 mm × 0.9 mm with chip pads.

V. CONCLUSIONS

An inductorless and differential IR-UWB RF receiver compliant with 802.15.3a standard is fabricated on a single chip using 0.18 μm CMOS technology. The receiver chip covers the lower band allocated from 3 to 5 GHz and 3-stage LNA is realized without on-chip inductor, which reduces the chip size dramatically down to 1.8 mm × 0.9 mm. The input signal is differential type in order to improve the immunity from common mode noise and undesired harmonic noise caused by detector and comparator circuit. The sensitivity of receiver is -70 dBm at data rate of 5 Mbps at the condition of BER 10^{-3} . The actual test shows that the UWB communication is properly operated

up to 8 m distance. The consumed power is 24 mW and thought to be a useful chip solution for low power sensor network.

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REFERENCES

- [1] Tiuraniemi, S., Stoica, L.; Rabbachin, A., and Oppermann, I., "Front-end receiver for low power, low complexity non-coherent UWB communication system," *IEEE International Conference on Ultra-Wideband*, pp. 339-343, Sept. 2005.
- [2] Yuanjin Zheng, Yan Tong, Jiangnan Yan; Yong-Ping Xu, Wooi Gan Yeoh, and Fujiang Lin, "A low power non-coherent CMOS UWB transceiver ICs," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers*, pp. 347-350, June 2005.
- [3] Yang Tong, Yuanjin Zheng, and Yong-Ping Xu, "A Coherent Ultra-Wideband Receiver IC System for WPAN Application," *IEEE International Conference on Ultra-Wideband*, pp. 60-64, Sep. 2005.
- [4] Garuda, C., Xian Cui, Po-Chih Lin, Seok Joo Doo, Pengbei Zhang, and Ismail, M, "A 3-5 GHz fully differential CMOS LNA with dual-gain mode for wireless UWB applications," *48th Midwest Symposium on Circuits and Systems*, pp.790-793, Aug. 2005.
- [5] Hui Dong Lee, Kyung Ai Lee, and Songcheol Hong, "Wideband VGAs Using a CMOS Transconductor in Triode region," *European Microwave Conference*, pp.1449-1452, Sept. 2006.



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