Design of Next Generation Amplifiers Using Nanowire FETs

Sotoudeh Hamedi-Hagh*, Sooseok Oh*, Ahmet Bindal* and Dae-Hee Park†

Abstract – Vertical nanowire SGFETs (Surrounding Gate Field Effect Transistors) provide full gate control over the channel to eliminate short channel effects. This paper presents design and characterization of a differential pair amplifier using NMOS and PMOS SGFETs with a 10nm channel length and a 2nm channel radius. The amplifier dissipates 5μW power and provides 5THz bandwidth with a voltage gain of 16, a linear output voltage swing of 0.5V, and a distortion better than 3% from a 1.8V power supply and a 20aF capacitive load. The 2nd and 3rd order harmonic distortions of the amplifier are -40dBm and -52dBm, respectively, and the 3rd order intermodulation is -24dBm for a two-tone input signal with 10mV amplitude and 10GHz frequency spacing. All these parameters indicate that vertical nanowire surrounding gate transistors are promising candidates for the next generation high speed analog and VLSI technologies.

Keywords: Nanowire, Amplifier, Low Voltage, High Frequency

1. Introduction

The speed of silicon integrated circuits is reaching beyond 100GHz to enable wireless communications with wideband channels [1]. Even though the current VLSI technology has approached its scaling limits necessitating a replacement technology, silicon based devices are still favored to realize large scale circuits and systems because of their low cost.

Downscaling of the Bulk MOSFETs (metal oxide semiconductor field effect transistors) to nanometer dimensions has increased the leakage current and short channel effects. Therefore, alternative silicon compatible transistor devices such as SOI (silicon on insulator) MOSFETs, FinFETs, and nanotube FETs have been investigated for improved performance.

Vertical SGFETs (surrounding gate field effect transistors) have full gate control around the channel and have minimized short channel effects [2]. The elimination of bulk in these transistors reduces latchup and substrate noise. The layout views of a vertical nanowire SGFET and a planar Bulk MOSFET are shown in Fig. 1 for comparison. Both transistors have identical channel widths of 13nm and channel lengths of 10nm and are designed with similar layout design rules. The area of the vertical transistor is (40nm×40nm) 1600nm^2 and the area of the planar transistor is also 1600 nm^2 (76nm×21nm) with body contact.

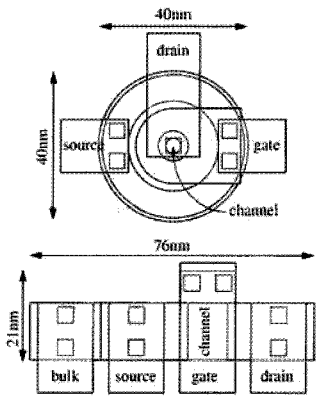

Fig. 1. Layout Views of (a) Vertical Nanowire SGFET and (b) Planar Bulk MOSFET

2. High Frequency Modeling

The three dimensional view and the corresponding parasitic components of the vertical nanowire SGFET are shown in Fig. 2. Only, the dominant parasitics are considered to simplify the circuit model.

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The intrinsic transistor M is modeled using a BSIM-SOI compatible model to ensure that all the input and output transfer characteristics of the circuit and device simulators match each other. The parasitic capacitance between the source contacts and the metal gate is denoted as C_{gs2} in the figure. The parasitic capacitance, C_{gs1}, between the metal gate and the concentric source make contact and the junction well is the largest dominant capacitor of the SGFET device. The gate and drain capacitors (C_{gd1} and C_{gd2}) and the drain and source capacitors (C_{ds1} and C_{ds2}) can be lumped into C_{gd} and C_{ds}, respectively. Compared to planar bulk transistors, C_{gd} is very small and there is no junction to bulk capacitance, therefore, C_{ds} is quite linear. The well resistance, R_s, can be quite large and is the major drawback of the vertical SGFETs compared with planar transistors. The magnitude of this resistance can be reduced drastically by placing a concentric (ring shape) source contact in parallel with the well, as shown in the figure.

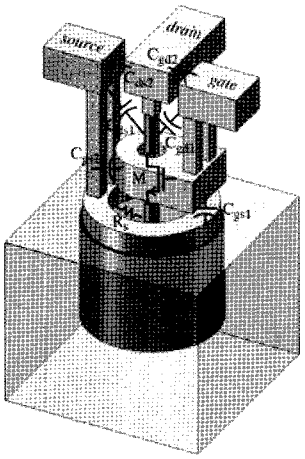

Fig. 2. The 3D View of Nanowire Transistor

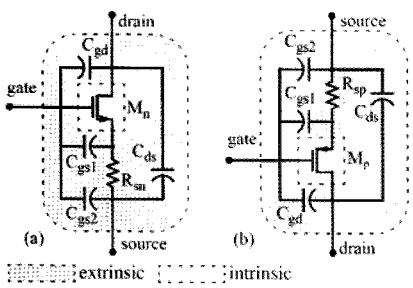

Fig. 3. Simplified Parasitic Components of (a) NMOS and (b) PMOS SGFETs

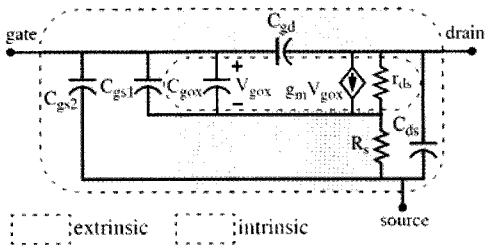

Fig. 4. Linearized Small-Signal Model of SGFET

The simplified parasitic components associated with NMOS and PMOS SGFETs are shown in Figs. 3(a) and (b). For accurate circuit level simulations, the intrinsic SGFETs (M_n and M_p) are modeled using BSIM-SOI.

For simplified hand calculations and finding the AC parameters of the amplifiers, designed using SGFETs, the linearized small-signal model shown in Fig. 4 can be used. Using this model at low frequencies, the DC voltage gain and output resistance of various amplifier stages can be calculated. The model shown in Fig. 4 is valid for transistors biased in the active operating region and transistor models in triode or cutoff regions can be easily constructed from this model by minor modifications.

3. High Frequency Modeling

Operational amplifiers are one of the most important building blocks of analog integrated circuits while differential pair amplifiers are the input building blocks of any opamp, as demonstrated in Fig. 5. Therefore, the performance of a differential pair amplifier, designed using SGFETs, needs to be measured before designing an opamp and will be investigated in this work.

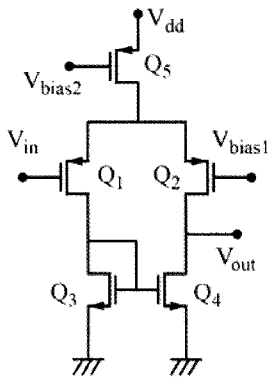

Fig. 5. Schematic of a Differential Pair Amplifier

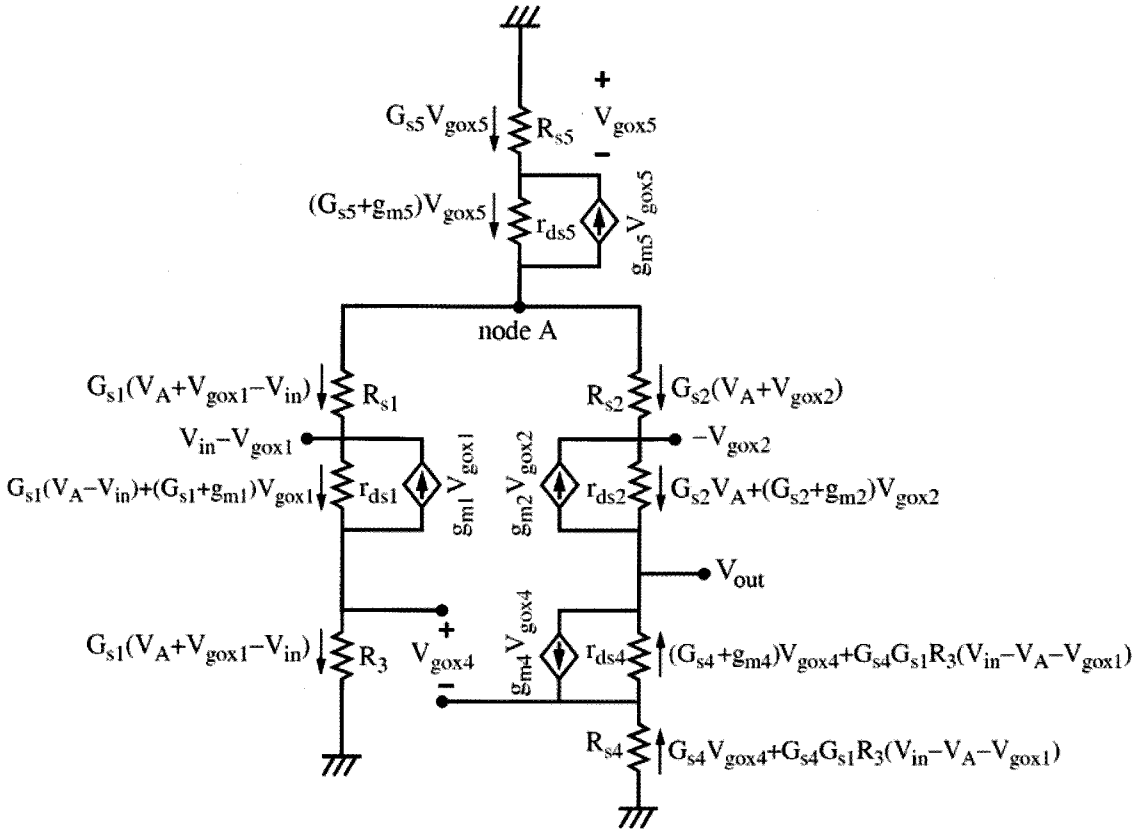

Fig. 6. The Low Frequency Small-Signal Model of the Differential Pair Amplifier

The low frequency small signal model of the differential pair amplifier designed using SGFETs is shown in Fig. 6.

The resistor R_3 is given by

$$R_3 = R_{s3} + \left(r_{ds3} \left\| \frac{1}{g_{m3}} \right. \right) \tag{1}$$

The voltage gain of the differential pair amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m2} r_{ds2} + \dfrac{r_{ds2}(g_{m2}+G_{s2})}{r_{ds5} G_{s2}}}{1 - \dfrac{g_{m2} r_{ds2} \left[r_{ds1}(g_{m1}+G_{s1}) + G_{s1} \left(R_{s3} + \dfrac{r_{ds3}}{1+g_{m3} r_{ds3}} \right) \right]}{g_{m1} r_{ds1} G_{s1} G_{s4} r_{ds4} \left(R_{s3} + \dfrac{r_{ds3}}{1+g_{m3} r_{ds3}} \right)}} \tag{2}$$

For $G_s \gg g_m \gg g_{ds}$, the voltage gain is approximately given by

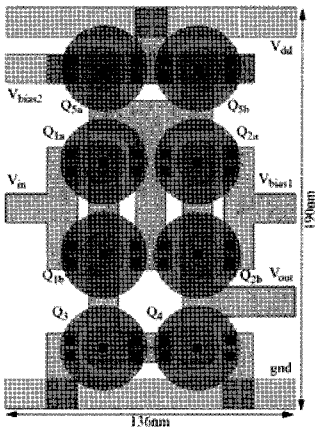

Fig. 7. Layout of the Differential Pair Amplifier

$$\frac{V_{out}}{V_{in}} \approx g_{m2} r_{ds2} \tag{3}$$

For $G_s \gg g_m \gg g_{ds}$, the output resistance is approximately given by

$$R_{out} \approx \left[r_{ds2} \left(1 + \frac{g_{m2}}{g_{m1}} \right) \right] \| \; r_{ds4} \tag{4}$$

The layout of the differential pair amplifier realized using 3 metallization layers is presented in Fig. 7. All interconnect parasitics are extracted and added to the amplifier netlist for postlayout simulations.

The main transistors of the input differential pair amplifier are realized by parallel combination of two p-type SGFETs to ensure a large transconductance. The width of the metal interconnects are selected to be 14nm to reduce their resistivity, and four parallel vias are used to connect metal-2 and metal-3 layers to minimize the signal loss. Each via with 4nm by 4nm dimension and 36nm height has a resistance of 400Ω. Overlap capacitance between metal-1 and metal-2 routing interconnects is 0.2aF for 14nm by 14nm dimension and 36nm height. The layout area of the differential pair amplifier is x=136nm and y=190nm.

4. Postlayout Characteristics

The transient and frequency responses of the SGFET differential pair amplifier are shown in Fig. 8. The amplifier provides a gain of 16 with the first pole located at 100GHz and the second pole located at 100THz. To attain high accuracy in the transfer functions of various analog circuits such as switch capacitor filters and amplifiers, it might be necessary to cascade multiple stages in nested Miller architectures and achieve a voltage gain higher than 1000.

The spectrum of the output waveform of the amplifier is given in Fig. 9. It has very good linearity characteristics and the total harmonic distortions of the amplifier are only 3% for ±233mV output swing. Such a high linearity is due to the source resistance, R_s, acting as the degeneration resistance and minimizing the harmonic distortions of input differential pair transistors.

The postlayout characteristics of the opamp are listed in Table 1. The good performance of the SGFET amplifier indicates that these transistors are good choices for future integration of high speed and low power analog and mixed signal circuits.

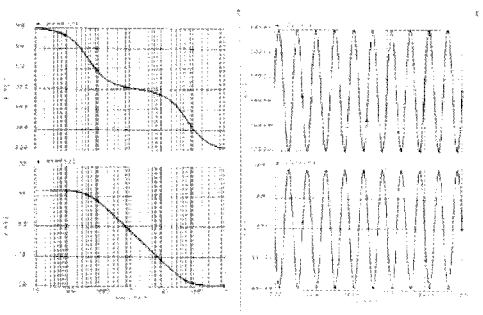

Fig. 8. Frequency and Transient Responses of the Differential Pair Amplifier

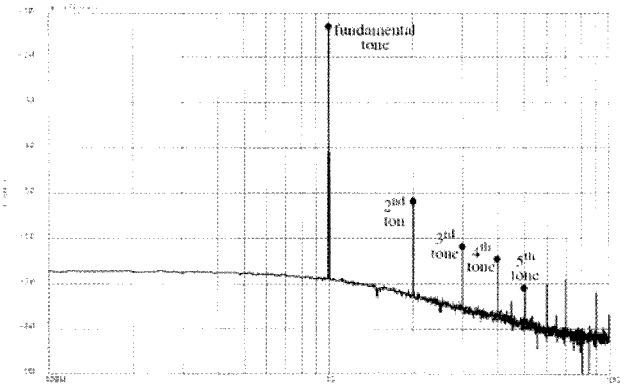

Fig. 9. Spectrum of the Output Transient Waveform

Table 1. Postlayout Characteristics of the Differential Pair Amplifier

Supply Voltage	1.8V
Maximum Output Linear Signal Swing	0.5V
Input DC Voltage Level	0.6V
Voltage Gain (at 1 GHz)	16
Phase Margin	>90°
Unity Voltage Gain Cutoff Frequency	5.1THz
Third Order Intermodulation Distortion (10mV two-tone signals with 1GHz spacing)	-24dBm
Second Order Harmonic Distortion	-40dBm
Third Order Harmonic Distortion	-52dBm
Total Harmonic Distortion	3%
Load Capacitor	20aF
Power Dissipation	5μW
area	136nm×190nm

5. Conclusions

The design and characteristics of a differential pair amplifier designed using nanowire SGFETs having channel length of 10nm and channel radius of 2nm were presented. The amplifier dissipates 5μW power and provides 5THz bandwidth with a voltage gain of 16 and a distortion better than 3%. All these parameters indicate that vertical nanowire SGFETs are promising candidates for realizing next generation high speed analog integrated circuits.

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Sotoudeh Hamedi-Hagh

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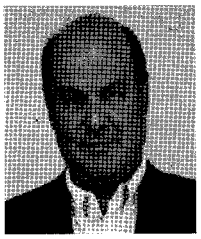

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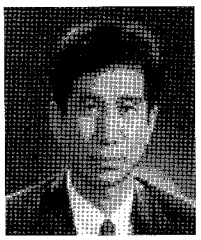

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