

Phase Angle Control in Resonant Inverters with Pulse Phase Modulation

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ABSTRACT

High frequency AC (HFAC) power distribution systems delivering power through a high frequency AC link with sinusoidal voltage have the advantages of simple structure and high efficiency. In a multiple module system, where multiple resonant inverters are paralleled to the high frequency AC bus through connection inductors, it is necessary for the output voltage phase angles of the inverters be controlled so that the circulating current among the inverters be minimized. However, the phase angle of the resonant inverters output voltage can not be controlled with conventional phase shift modulation or pulse width modulation. The phase angle is a function of both the phase of the gating signals and the impedance of the resonant tank. In this paper, we proposed a pulse phase modulation (PPM) concept for the resonant inverters, so that the phase angle of the output voltage can be regulated. The PPM can be used to minimize the circulating current between the resonant inverters. The mechanisms of the phase angle control and the PPM were explained. The small signal model of a PPM controlled half-bridge resonant inverter was analyzed. The concept was verified in a half bridge resonant inverter with a series-parallel resonant tank. An HFAC power distribution system with two resonant inverters connected in parallel to a 500kHz, 28V AC bus was presented to demonstrate the applicability of the concept in a high frequency power distribution system.

Keywords: Resonant inverter, Pulse phase modulation, High frequency AC power distribution system, Circulating current

1. Introduction

High frequency alternative current power distribution systems (HFAC PDS) have been developed for a number of specific applications to deliver power to points-of-use. One example is the space power distribution architectures [1]. Other examples include airplane entertainment, engine power supply systems [2-3], contact-less power

delivery systems [4-6], desktop computers and telecommunication power supply systems [7-15]. An HFAC PDS includes a front-end, a full-bridge resonant inverter (FBRI) or half-bridge resonant inverter (HBRI). The HFAC bus and AC VRM are shown in Fig.1. A resonant inverter is used to generate the HFAC sinusoidal waveform, differing from the traditional sinusoidal pulse-width-modulated (SPWM) inverters. Hence the HFAC bus frequency determines the switching frequency of the DC/AC inverters. The overall efficiency of the front-end and the inverter can be 95%, while the AC VRM can achieve efficiency of 90% or more. In order to

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increase the power density, HFAC power distribution architecture has evolved from tens of kilohertz systems to hundreds of kilohertz systems, and the 1MHz is expected to go further beyond 1MHz. The high frequency DC/AC resonant inverter is used to generate high frequency AC voltage for the HFAC bus, with features like soft-switching of the main switches and low THD in the output voltage. One half-bridge resonant inverter topology^[11] is shown in Fig. 2. It consists of a half-bridge switch network, a series-parallel resonant tank, and a high frequency transformer. The feedback control includes the control error detection K_{DV} , a linear voltage controller K_V , and an asymmetrical pulse width modulator (APWM). With proper design, both switches achieve zero voltage switching. The waveform quality of the output voltage can be improved by using an additional high pass filter.

The current sharing in a HFAC system requires tight control of the phase angle of the output voltage of individual resonant inverters. Unlike the sinusoidal PWM inverters, the resonant inverters use pulse shift modulation or pulse width modulation to control the inverters. In these conventional modulation methods, the phase angle of the inverter output voltage is free of control. Therefore, even for the same pulse modulation signal, the output voltage phases can be different because of power stage diversity such as load conditions and component tolerance of the resonant and switch components. Another source of phase difference is the time delays in the control and gate drive circuits.

A pulse phase modulation concept was investigated based on the phase angle control of the output voltage of the resonant inverters. The mechanism of the pulse phase modulation will be described. Based on the topology of the half-bridge resonant inverter in Fig. 2, a phase angle controlled resonant inverter will be designed, analyzed, simulated and prototyped.

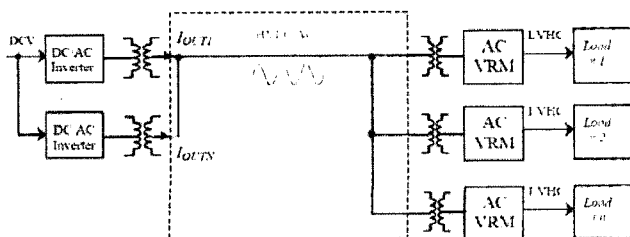


Fig. 1 Conceptual HFAC power supply system

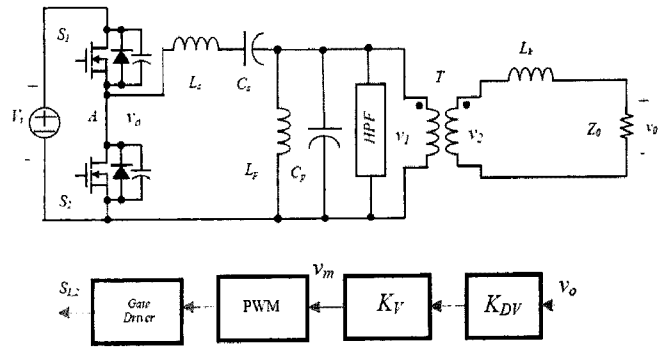
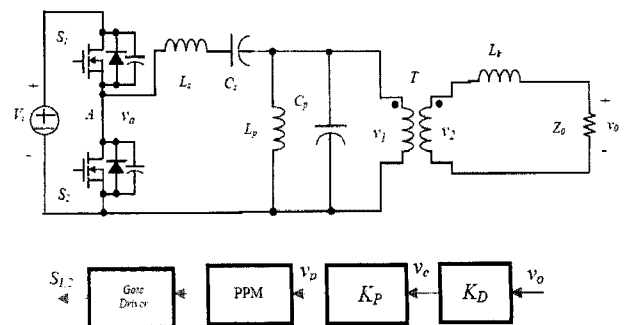


Fig. 2 Simplified schematics of a resonant inverter system

2. Principal Mechanism of the Pulse Phase Modulation

The phase angle of the resonant inverter is determined by the phase of the modulation pulses as well as the impedance of the equivalent load and the resonant tank. For different load conditions, the phase angles of individual inverters differ because of the component tolerances of the resonant tanks, connection inductances and gate delay time of the gate drivers. However, the phase angle between the load terminal and the bridge voltage is solely determined by the impedance of the network; such an angle is fixed for a given load condition. Therefore, by controlling the pulse phase, the phase angle of the output voltage can be regulated against the load or the line perturbation and component tolerance. In this way, the inverter behaves as a pulse phase modulated (PPM) voltage source. A PPM controlled resonant inverter is shown in Fig. 3, where the power stage is the same as the voltage controlled half-bridge resonant inverter (Fig. 2), while the control includes three basic blocks, a phase angle detector K_D , a phase angle controller, and a pulse phase modulator.



L_s, C_s	Series resonant tank inductor and capacitor
L_p, C_p	Parallel resonant tank inductor and capacitor
S_1, S_2	Two switches in the half bridge
K_D	Phase angle detector
K_p	Phase angle controller
PPM	Pulse phase modulator
V_p	Phase modulation signal
V_e	Phase error
V_o	Output voltage

Fig. 3 PPM controlled resonant inverter system

2.1 Phase angle detection

Assume the reference signal of the resonant inverter is sinusoidal with amplitude V_r and phase angle φ_r as given in (1), where φ_r is constant, although in a current sharing control system, it is time varying and responds to the input of the controller. The output voltage of inverter v_o should follow the phase of reference signal v_r as closely as possible. Also assume that the filtering performance of the inverter resonant tank is so perfect that all of the harmonics are well attenuated in the inverter output terminal. Therefore, only the fundamental frequency (operation frequency) component is considered.

$$v_r = V_r \sin(\omega t + \varphi_r) \quad (1)$$

Suppose the output voltage has amplitude V_o and phase angle φ_o , as represented by cosine in (2), where φ_o is time varying during transient.

$$v_o = V_o \cos(\omega t + \varphi_o(t)) \quad (2)$$

The actual phase error φ_e between these two signals is given in (3). Therefore, the objective of the phase angle control is to minimize the phase angle difference between the reference signal v_r and inverter output voltage v_o in both the steady state and transient state. From (1) and (2), apply the multiplier operation to the two signals, and the output voltage of the multiplier is derived in (4).

$$\varphi_e(t) = \varphi_o(t) - \varphi_r \quad (3)$$

$$v_e = 0.5V_r V_o (\sin(-\varphi_o(t) + \varphi_r) + \sin(2\omega t + \varphi_o(t) + \varphi_r)) \quad (4)$$

The expression in (4) has two terms, a DC term, and an

AC term, with frequency twice the switching frequency, which can be easily filtered out by a low pass filter. Therefore, if the harmonics are filtered out, then the output of the multiplier is related to the phase difference between the reference signal v_r and the real inverter output voltage v_o by a sinusoidal function as given in (5). It is noted that because the phase angle of the output voltage is time varying, the phase error after the low pass filter, V_e , is still a function of time.

$$V_e = 0.5V_r V_o \sin(-\varphi_o(t) + \varphi_r) \quad (5)$$

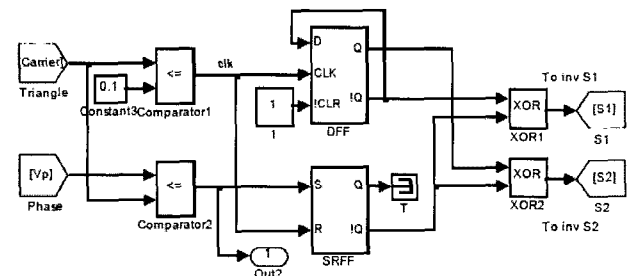
The sine function can be linearized near zero. For small phase difference, V_e is approximately in proportion to the phase difference by a factor K_D , which is the gain of the phase detector.

$$V_e(t) \approx K_D (\varphi_r - \varphi_o(t)), \quad \|\varphi_r - \varphi_o(t)\| \rightarrow 0 \quad (6)$$

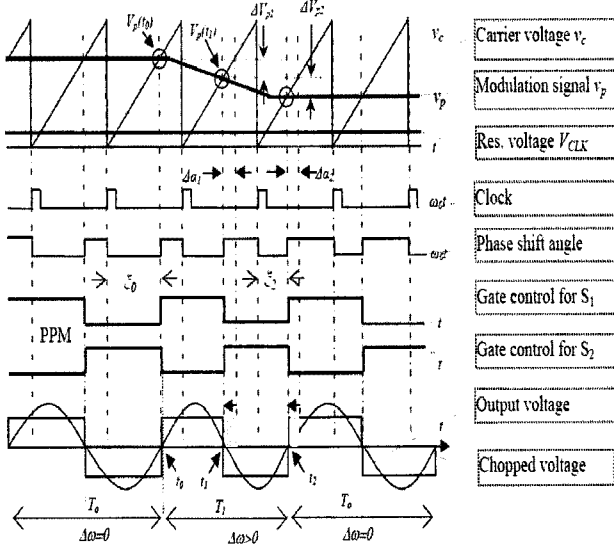
Hence the phase angle difference between these two signals can be easily detected with an analog multiplier and a low pass filter of cut-off frequency lower than the operation frequency of the resonant inverter.

2.2. Pulse phase modulation

The logic scheme for the pulse phase modulation is shown in Fig. 4(a), which consists of a DFF, a SR FF, two comparators and 2 XOR gates. The input signals to the PPM include the carrier signal v_c , which is a saw-tooth waveform, and the phase modulation signal v_p . The carrier waveform modulates the phase modulation signal and generates a PWM signal in reverse proportion to the modulation signal, which is then used to generate the gate signals.



(a) The logic circuit for the PPM



(b) Principal waveforms of the pulse phase modulation

Fig. 4 Schematic of PPM controller and the operation waveforms

The mechanism to shift the phase angle for a change of the phase angle modulation signal is explained with the operation waveforms in Fig. 4(b), where the modulation signal has a transient within one operation period. For one complete PPM pattern of period T_0 , it needs two pulses of the carrier signal to finish. The modulation signal is assured consistency before and after the transient. The PPM for the inverter has a duty ratio of $D=0.5$. The initial phase angle with respect to the clock signal is ξ_0 . The initial switching period is T_0 . The phase modulation signal v_p is time varying.

Let the gain K_M be the change of the PPM phase angle to the modulation signal variation Δv_p , which is the slope of the carrier signal v_c , according to the geometry relationship in Fig. 4(b).

$$K_M = \frac{\Delta\alpha}{\Delta v_p} = \pi / V_{pp} \quad \text{or} \quad \Delta\alpha = K_M \Delta v_p, \quad (7)$$

$$\text{where } \|\Delta v_p\| < V_{pp}$$

Assume at t_0 transient begins. The phase modulation signal is $v_p(t_0)$ at t_0 . $v_p(t)$ intersects with the carrier signal v_c at t_1 . The corresponding modulation signal at t_1 is $v_p(t_1)$, which is given in (8).

$$v_p(t_1) = v_p(t_0) - \Delta V_{p1} \quad (8)$$

The pulse reduction $\Delta\alpha_1$ corresponding to the modulation signal change is determined by K_M , and is given by (9).

$$\Delta\alpha_1 = K_M \Delta V_{p1} \quad (9)$$

Then $v_p(t)$ intersects the successive pulse of the carrier signal v_c at t_2 . At t_2 , the modulation signal is given by (10), corresponding to phase reduction $\Delta\alpha_2$ (11).

$$v_p(t_2) = v_p(t_1) - \Delta V_{p2} \quad (10)$$

$$\Delta\alpha_2 = K_M \Delta V_{p2} \quad (11)$$

Altogether, the phase angle is shifted forward by $\Delta\alpha$, which is given in (12), or in the time domain, this corresponds to the reduction of the switching period by ΔT , which is given in (13), together with the new PPM period. The final phase angle with respect to the clock signal is ξ_2 , as indicated in Fig. 4(b).

$$\Delta\alpha = K_M (\Delta V_{p1} + \Delta V_{p2}) \quad (12)$$

$$\Delta T = \frac{\Delta V_{p1} + \Delta V_{p2}}{2V_{pp}} T_0 \quad (13)$$

$$T_1 = T_0 - \Delta T = T_0 \frac{2V_{pp} - \Delta V_p}{2V_{pp}}$$

Therefore, the equivalent frequency of this switching period is different from the original one, and the increase of frequency is $\Delta\omega$, which is given in (14)

$$\Delta\omega = \omega_0 \frac{\Delta V_p}{2V_{pp} - \Delta V_p} \quad (14)$$

The corresponding equivalent frequency of the PPM for this period is increased and given in (15). After the transient, the frequency restores to the original frequency ω_0 .

$$\omega_{(1)} = \omega_{(0)} + \Delta\omega \quad (15)$$

The duty ratio during this transient period is time

varying, and is determined by the modulation signal variations, as is given in (16). Since ΔV_p changes from zero to V_{pp} , the range of the duty ratio D is from 0 to 1 during transient.

$$D_{(1)} = \frac{V_{pp} - \Delta V_{p1}}{2V_{pp} - (\Delta V_{p1} + \Delta V_{p2})} \quad (16)$$

Since the inverter can be treated as an LTI network, the frequency of the output voltage is the same as the PPM signal. Therefore, the output voltage can be written in (17) for the next period. Obviously, the phase angle of the output voltage can be controlled through the phase angle modulation signal v_p . The phase angle with respect to the clock signal is ζ_2 .

$$v_o = V_o \cos(\omega_0 t + \Delta\alpha + \varphi_0) \quad (17)$$

The phase angle controller K_p calculates the phase modulation signal v_p from the phase error signal V_e which is from the phase angle detector circuit. As long as the phase angle of the output voltage approximates that of the reference signal, the output of the phase detection will be approximately constant after a certain time. Then the frequency change of the PPM will be zero also, indicating the end of the transient.

The theoretical range of phase angle control is from 0 to π . However, it is noted that there is no interval overlap between the PWM pulse and the clock signal. And the modulation signal should be kept below the peak of carrier v_c . Therefore, the relationship between the modulation signal and the phase shift angle is shown in Fig. 5. α_{\min} is given in (18) where V_{CLK} is the voltage level compared with the carrier signal and it generates the clock signal.

$$\alpha_{\min} = \frac{V_{CLK} T}{2V_{PP}} \quad (18)$$

In order to adjust the phase angle towards both positive and negative directions to $\pi/2$, it is suggested that the saw-tooth waveform rises from $-V_{pp}/2$ to $+V_{pp}/2$. Then the phase angle control range is $[-\pi/2, \pi/2]$.

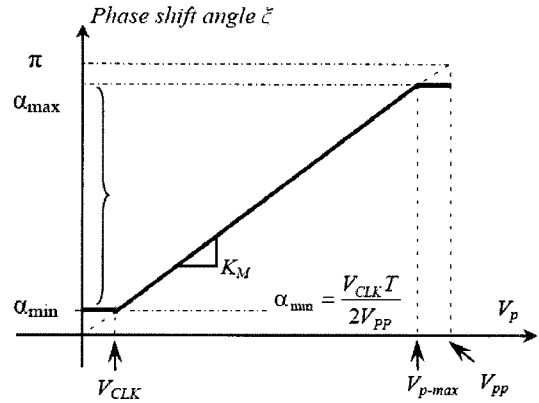


Fig. 5 Relationship between modulation signal and PPM phase shift

2.3 Small signal analysis

The system of the PPM controlled resonant inverter (in Fig. 3) is nonlinear because of the pulse phase modulation and the multiplier operation for the phase angle detection. It is necessary to derive a linear model so that the controller can be designed. Assume at a certain operation point the system reaches a steady state. If small perturbations and linearization are applied to the system, it can be simplified as a small signal linear system.

The phase angle error between the inverter output voltage and the reference signal is detected by a multiplier and a low pass filter in combination and represented as a voltage signal, according to (5). Around any steady state operation point, the phase difference is very small, that is, $\|\varphi_o - \varphi_r\| \ll 1$.

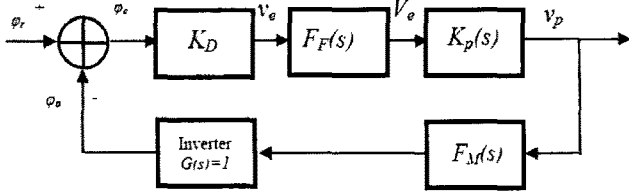
In the small signal sense the phase error is linearly related to the phase angle difference of the two signals. Therefore, the error signal or the phase modulation signal is given in (19), where $K_F(s)$ is the transfer function of the low pass filter.

$$V_e = F_F(s) K_D (\varphi_o - \varphi_r) \quad (19)$$

Since the resonant tank of the inverter has no amplification on the phase shift angle, it is treated as a unity gain unit and the impedance phase angle of the resonant tank is treated as perturbation.

The small signal model of the system is shown in Fig. 6, where K_D is the gain of the multiplier, $K_p(s)$ is the phase angle controller, $F_M(s)$ is the transfer function of the PPM,

$F_F(s)$ is the low pass filter. The closed loop system transfer function is hence given in (20).



- K_D Phase angle detector gain
 $F_F(s)$ Low pass filter transfer function
 $K_p(s)$ Phase angle controller
 $F_M(s)$ PPM modulator transfer function

Fig. 6 Small signal model of PPM controlled resonant inverter

$$H(s) = \frac{K_D F_F(s) K_p(s) F_M(s)}{1 + K_D F_F(s) K_p(s) F_M(s)} \quad (20)$$

The transfer function of the inverter output voltage phase angle tracking error is given by (21), from which the phase angle tracking error can be evaluated.

$$H_e(s) = 1 - H(s) = \frac{1}{1 + K_D F_F(s) K_p(s) F_M(s)} \quad (21)$$

The phase angle controller can be designed with the gain-phase margin approach. A simple design is to use a *PI* controller with proportion K_c and time constant T_c , for the detection and control. The low pass filter can be replaced with an integral K_F/s . The transfer function from the input phase angle to output phase angle can be written in (22), which is a 2nd order system.

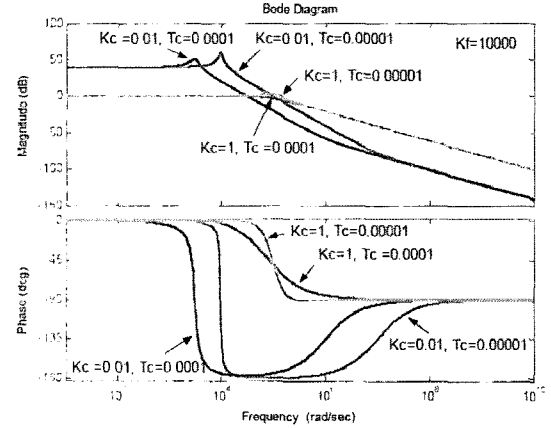
$$H(s) = \frac{K_D K_F K_c K_M s + K_D K_F K_M / T_c}{s^2 + K_D K_F K_c K_M s + F_M K_D F_F K_c / T_c} \quad (22)$$

The natural resonant frequency of the system is given in (23), and the damping factor is given in (24), which are solely determined by the controller parameters T_c and K_c , and the integral time constant K_F .

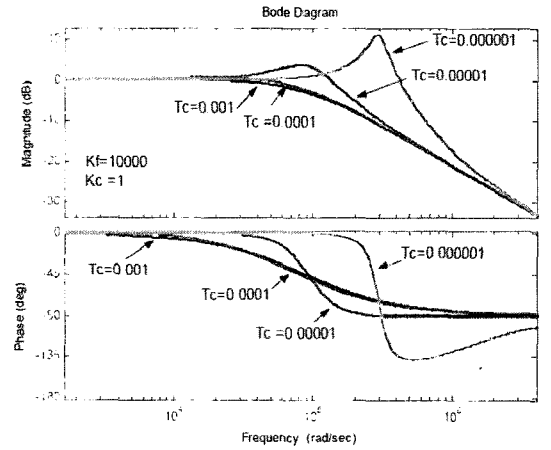
$$\omega_n = \sqrt{K_M K_D} \sqrt{K_F K_c / T_c} \quad (23)$$

$$\zeta = \sqrt{K_M K_D} \sqrt{K_F K_c T_c} \quad (24)$$

The frequency responses of the PPM-controlled resonant inverter are plotted for different parameters of K_c , T_c and K_F in Fig. 7. The damping factor can be increased with large time constant T_c . And the bandwidth of the system can be increased with a large K_c .



(a) $K_c=0.01, 1, 10k$; $K_F=10k$



(b) $K_c=1$; $K_F=10k$; $T_c=10^{-3}, 10^{-4}, 10^{-5}, 10^{-6}$

Fig. 7 Frequency domain response of the PPM-controlled system

3. PPM-controlled Half-bridge Resonant Inverter

A PPM-controlled half-bridge (HB) series-parallel resonant inverter as shown in Fig. 3 is designed. The input to the HB resonant inverter module is 38V. The two switches in the half bridge are driven by complementary gate signals of frequency 500 kHz. To prevent a short in the DC source, enough dead time is mandatory. The output power of the inverter is 100W. The output voltage is 500 kHz sinusoidal with amplitude 39V (Peak). A high frequency transformer of turns-ratio 1:2.2 is used. $L_s = 3.9 \mu\text{H}$, $C_s = 27\text{nF}$; $L_p =$

0.98μH, $C_p = 85$ nF

The resonant tank not only filters out the harmonics in the semi-square voltage, but also offers soft-switching for the power switches. A resonant tank with two energy storage components is usually used in DC/DC conversion topologies, for example, the parallel resonant converter and the series resonant converter. A sinusoidal voltage waveform with very small THD is desirable in an HFAC system to avoid Electromagnetic Interference (EMI) in the HFAC bus. The series-parallel resonant tank with four energy storage components gives more design freedom in the soft-switching design. Such a resonant tank also has better filtering performance than an LCC or LC tank. Therefore, it is a reasonable choice for HFAC applications. In Fig. 3, L_s and C_s are the series resonant network inductor and capacitor, respectively. L_p and C_p are the parallel resonant network inductor and capacitor, respectively. The resonant frequencies of the series and parallel resonant tank are determined by the series and parallel inductor and capacitors as given in (25).

$$\omega_s = 1/\sqrt{L_s C_s}; \quad \omega_p = 1/\sqrt{L_p C_p} \quad (25)$$

The series resonant tank is tuned to above 0.95 of the operation frequency. The parallel resonant tank is tuned to 1.2 of the operation frequency. Therefore, the impedance viewed from the input port of the resonant tank is inductive at operation frequency. Since the pulses are symmetrical, there is no even order harmonics in the chopped voltage. Therefore, no high order filter is needed.

The impedance viewed from the input port of the resonant network depends on both the parameters of the resonant tank and equivalent load of the HFAC bus, and is given in (26), where Z_s and Z_p represent the impedances of the series resonant tank and parallel resonant tank, respectively.

$$Z_{ih} = Z_{sh} + Z_{ph} \quad (26)$$

The impedance of the series and parallel resonant tanks are given in (27) and (28), respectively, in which the equivalent resistance R_e and equivalent reactance X_e are the equivalent load impedances of the HFAC bus reflected

from the secondary side of the transformer to the primary side.

$$Z_{sh} = R_s + j(hX_{L_s} - X_{C_s}/h) \quad (27)$$

$$Z_{ph}^{-1} = \frac{R_e}{R_e^2 + X_{eh}^2} + j\left(\frac{h}{X_{C_p}} - \frac{1}{X_{L_p}h} - \frac{X_{eh}}{R_e^2 + X_{eh}^2}\right) \quad (28)$$

In a general case with a non-resistive equivalent load of the AC bus, the AC gain of the resonant tank A_h is given in (29).

$$A_h = \left\| \frac{Z_{p,h}}{Z_{s,h} + Z_{p,h}} \right\| = \left(\frac{R_{p,h}^2 + X_{p,h}^2}{(R_s + R_{p,h})^2 + (X_{s,h} + X_{p,h})^2} \right)^{1/2} \quad (29)$$

In the above, $R_{p,h}$ is the equivalent resistance of the parallel resonant tank, R_s is the equivalent resistance of the series resonant tank, $X_{s,h}$ is the equivalent reactance of the series resonant tank, and $X_{p,h}$ is the equivalent reactance of the parallel resonant tank.

The instantaneous voltage of the primary winding of the transformer can be expressed in (30), where γ_h is the phase difference between the bridge voltage $V_{a,h}$ and the voltage of the parallel resonant tank $V_{l,h}$ of h^{th} order harmonic components, and is given in (31).

$$v_{1,h}(t) = \sum_h A_h \frac{2V_{in}}{h\pi} \sin \frac{h\pi}{2} \sin(h\omega_o t - \gamma_h) \quad (30)$$

$$\gamma_h = a \tan \frac{X_{p,h}(R_s + R_{p,h}) - R_{p,h}(X_{s,h} + X_{p,h})}{R_{p,h}(R_s + R_{p,h}) + X_{p,h}(X_{s,h} + X_{p,h})} \quad (31)$$

The phase angle difference $\Delta\gamma$ between a nominal inverter and that with a different series inductor L_s ($= L_{s0} + \Delta L_s$) are plotted in Fig. 8 for different load conditions. It is obvious that both the load impedance and the impedance of the resonant tank determine the value of the phase angle difference $\Delta\gamma$. For the same bridge voltage, the phase angle of the output voltage can be different because of the component tolerance of the power circuit, and the load variations.

A prototype PPM controlled half-bridge resonant inverter was built in the lab. The circuit specifications and component parameters are given in Table 1. The MOSFET devices are IRF540N. The resonant capacitors

are Wima FKP, and the magnetic core of the transformer is TDKPC44LP22/13. The thermal resistors are used in parallel as the equivalent load for the resonant inverter. The power factor of the equivalent load at the operation frequency is corrected by series connection capacitors.

Table 1 Circuit specifications and component parameters

Output voltage V_o	18V (Peak)
Input voltage V_m	38V (Average)
Frequency f_s	0.5 MHz
Efficiency η	92%
Output Power P_o	100W
Series resonant tank	$L_s=3.9 \mu\text{H}$, $C_s=27\text{nF}$
Parallel Resonant tank	$L_p=0.98\mu\text{H}$, $C_p=85 \text{ nF}$
Switches	IRF540N
Transformer T	1:2.2, Input 18V/Output 38V
Core	TDKPC44LP22/13
Gate drivers	HIP2101

Therefore, the resonant current flows in the anti-parallel diode of the switch S_1 , and the voltage across the drain and source is clamped to zero. Therefore, S_1 is turned on under zero voltage. The turning off of the switches is softened with snubber capacitors. The magnetizing inductance current of the high frequency transformer offers enough current for open-load conditions.



Fig. 9 Circuit diagram for the PPM

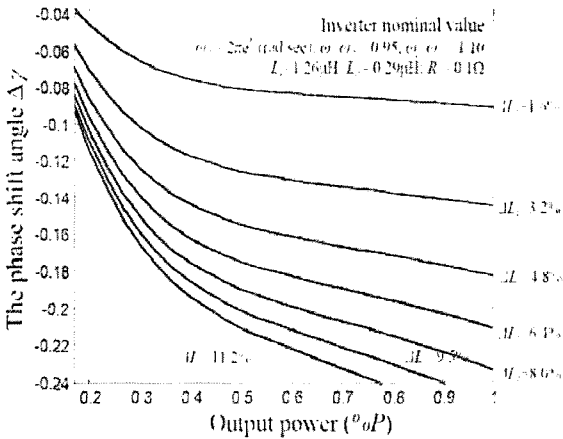


Fig. 8 Phase angle difference $\Delta\gamma = \gamma_1 - \gamma_0$, where, γ_0 is the phase shift angle of the nominal inverter (L_{s0}), γ_1 is that of the inverter with a different L_s , $L_s = L_{s0} + \Delta L_s$

The circuit diagram of the pulse phase modulation is given in Fig. 9, where the commercial available discrete components including 74F08, 74F86, and 74F74 have very small time delays. The dead time is set to 80ns by the RCD circuit.

The verification waveforms are given in Figures 10 and 11. In Fig. 10, the voltages across the drain and source of the main switches, and the currents are shown. From these waveforms, it is observed that both of the switches achieve zero voltage switching. For instance, at the instant switch S_1 is turned on, the resonant current is negative.

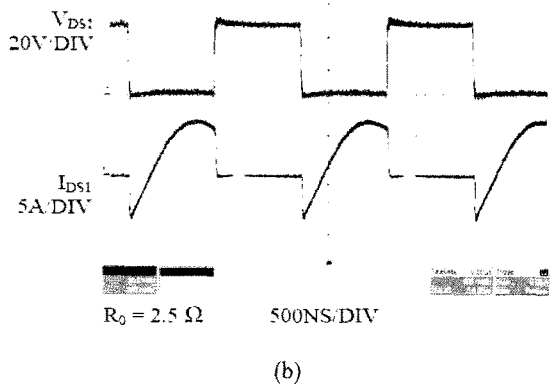
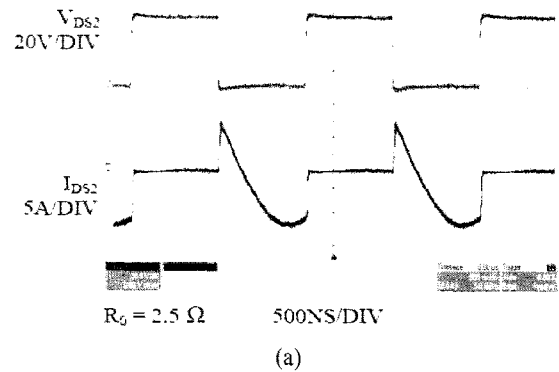


Fig. 10 Voltages and currents of the main switches (a) FET S_2 , (b) FET S_1 in the second stage $R_o = 2.5\Omega$

The operation waveforms for the resonant inverter with different phase modulation levels are given in Fig. 11, where the phase modulation signal, clock signal and the output voltages of the inverters are given. The top waveforms are the phase modulation signals V_p , the middle ones are the Clock signals Clock, which are synchronized to the same for all inverter modules, and the bottom ones are the output voltages V_o . For a large modulation signal ($V_p = 0.8V$), the phase angle of the output voltage with respect to the clock signal is $\xi_1 \approx 365\text{ns}$. For a small modulation signal ($V_p = 0.1V$), the phase angle of the output voltage with respect to the clock signal is $\xi_2 \approx 250\text{ns}$.

Obviously with the PPM control, the output voltage phase angles can be controlled through a phase angle feedback control. Some application examples of the PPM control include: synchronize the output voltage phase angles of the inverters; control the active and reactive power flow by controlling the phase angles; minimize the circulating current by combining the PPM with certain current sharing control scheme. In the next section, it will be shown through experiments that by controlling the phase angles of the output voltages of individual inverters in a multiple inverter system, the circulating current can be reduced.

4. Two-stage Resonant Inverter with Phase and Magnitude Control

Two resonant inverter modules as shown in Fig. 12 were built in the lab to make up a two-inverter system. Each resonant inverter consists of two stages. The second stage of each resonant inverter module is the same as the half-bridge resonant inverter that we have discussed in the previous section. It operates at 500 kHz, and the output of each inverter module is 100W, 28V (RMS). To avoid the phase shift problem, this stage is not for voltage magnitude control. Since the duty ratio is kept 50%, the switches in this stage are always soft-switched. The resonant tank and the switches are optimized for minimum conduction loss. The first stage is a two-switch buck converter running at 1 MHz, and is solely for voltage magnitude control. Compared with the single-stage full-bridge topology, the two-stage provides

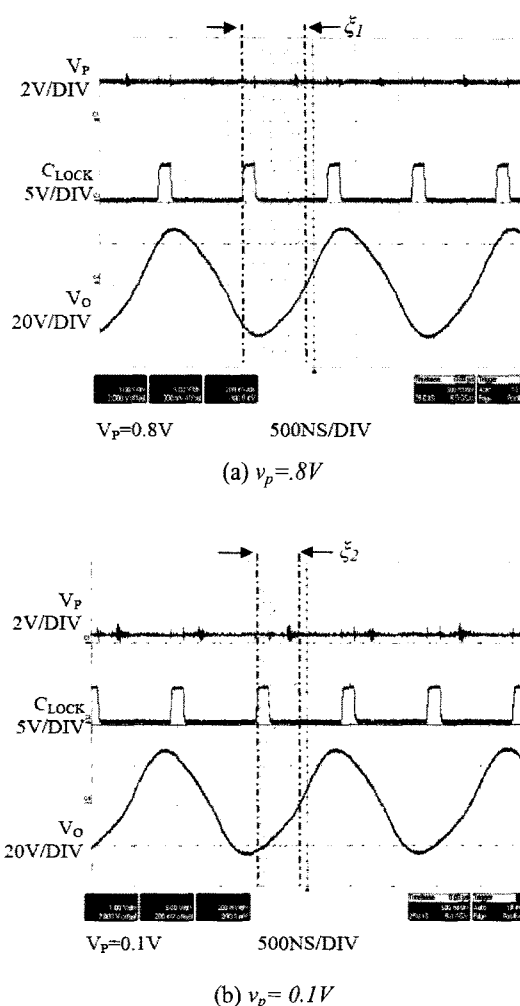


Fig. 11 Waveforms for the pulse phase modulation

similar efficiency, while offering much more flexibility in the topology and pulse modulation design.

Although both inverters use the same parameters, there are component tolerances. For instance, the component tolerance for the commercial resonant inductors is above 10%. The internal conduction resistance of the MOSFET can be as high as 50%.

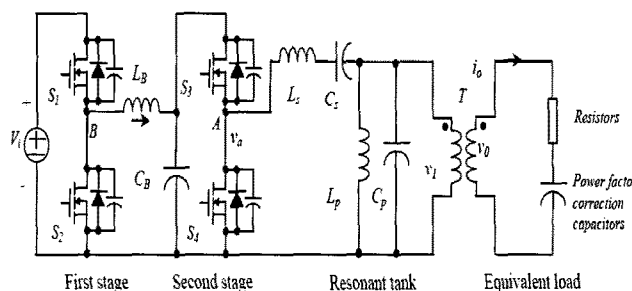


Fig. 12 Simplified circuit schematics of a 2-stage inverter system

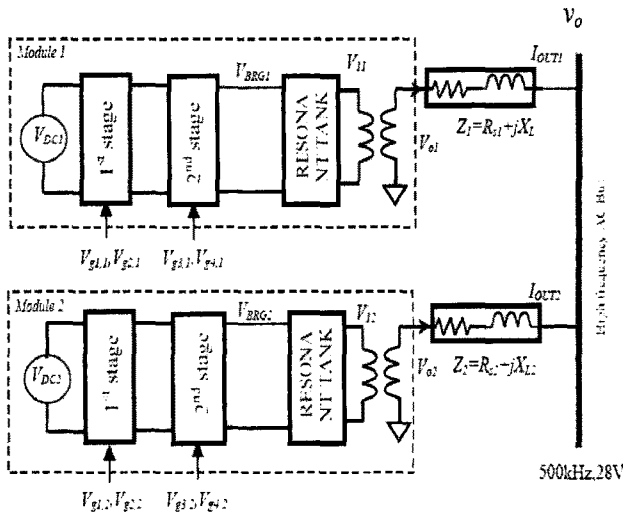


Fig. 13 Control and power stage layout of the system

The two resonant inverters are connected to the high frequency AC bus through small connection inductors. The system layout is shown in Fig. 13, where the topology of each inverter module is shown in Fig. 12. A connection inductor Z_k is used and is modeled as a resistance and reactance in series, $Z_k = R_k + jX_k$. Assuming that the equivalent load of the HFAC bus is resistive, based on AC analysis, the circulating current between the two inverter modules is given in (32), where C is a coefficient, V_{O1} and V_{O2} are the terminal voltages of the resonant inverters, which are functions of the input voltages, impedance of the resonant tanks, and the switching functions of the switching networks, according to (30). R is the equivalent load resistance of the HFAC bus.

$$\frac{2\Delta I}{C} = 2V_{O1}\angle\phi_1 - 2V_{O2}\angle\phi_2 + j\left(\frac{Z_{k2}}{R}V_{O1}\angle\phi_1 - \frac{Z_{k1}}{R}V_{O2}\angle\phi_2\right) \quad (32)$$

Obviously, both the discrepancy of phase angles and magnitudes of the output voltages of the inverters cause circulating current. In addition, the difference in the connection inductors can also cause uneven current distribution. Therefore, paralleling multiple resonant inverters in a high frequency AC system is much more complicated than paralleling multiple converters in a DC system.

The connection inductance is critical to limit the circulating current in the HFAC power system. The size of

the connection inductor should be compromised for output voltage regulation as well as for space and cost. Furthermore, the conduction resistance must be very small to minimize thermal losses. Generally, the connection inductors should meet the following conditions in (33) and (34).

$$X_{L_{k1}} \approx X_{L_{k2}} \quad (33)$$

$$X_{L_{k1}} \gg R_{k1}; X_{L_{k2}} \gg R_{k2} \quad (34)$$

In practice, the connection inductance consists of both the leakage inductance of the high frequency transformer, and external inductance, both of which have large component tolerance. The measured inductances are as follows: $L_1 = 0.23\mu\text{H}$, $L_2 = 0.27\mu\text{H}$. The discrepancy of the connection inductance is an important cause of circulating current, according to (32).

In order to reduce the circulating current between the inverter modules, three possibilities exist. 1) Using large connection inductors. However, this causes large voltage drop over the connection inductors. 2) Using components (including the connection inductors) with small component tolerance. This increases the cost of the system, and can not eliminate the circulating current caused by the control circuit discrepancy. 3) Using proper current sharing control with PPM.

1) Output voltage magnitude is controlled through the first stage with PWM

In the PWM-controlled inverter, the first-stage voltage is regulated through $V_{g1,n}$, $V_{g2,n}$, $n = 1, 2$. The second stage is free of control, but uses the same gate drive pulses as the other module. $V_{g3,1} = V_{g3,2}$, $V_{g4,1} = V_{g4,2}$. Because of the component tolerance in the second stage, there is phenomenal phase discrepancy between the output voltages V_{O1} and V_{O2} . Together with the connection inductance difference, it will cause large circulating current. In Fig. 14(a), the DC inputs V_{DC1} and V_{DC2} are different. $V_{DC1} = 55\text{V}$, $V_{DC2} = 75\text{V}$. With the PWM control in the first stage, the first stage output voltages of both the two inverters are 38V. However, the circulating current is about 25% of the load current.

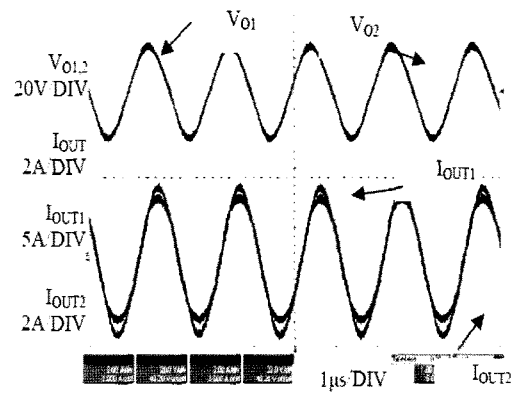
The circulating current is caused by the asymmetry existing in the second stages of the two inverter modules.

As can be seen from (31) and Fig. 8, phase discrepancy may be a result of the component tolerance of the power stage, even using the same pulses to drive the two second stages.

Another factor is the delay in the control, including the gate drive circuit, and the modulation circuit. The rising time and falling time of the commercial gate drivers change with operation conditions, like temperature, operation voltages, and output capacitances. Delay differences also exist in the modulation circuit. For example, the component tolerance in the RCD dead-time setting circuit can cause the drive pulses to differ from each other, even with the same modulation signal.

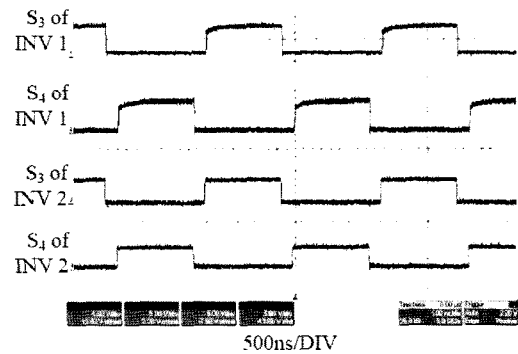
2) Output voltage phase angle is controlled with PPM

In contrast, the PPM-controlled resonant inverter regulates the phase angle of the output voltage against any possible perturbations and defects of the circuits, as shown in Fig. 14(b). The first stages are controlled with PWM control $V_{g1,n}$, $V_{g2,n}$, $n = 1,2$. The DC voltages applied to the second stages are 38V. The magnitudes of the output voltage are, however, free of control. The second stage is PPM-controlled. The circulating current between the two modules is effectively reduced to about 12% of the load current. The remaining small current distribution error is caused by the voltage magnitude discrepancy of the two modules, and the connection inductor difference. The corresponding voltage V_{01} , V_{02} , and the gating signals $V_{g3,1}$, $V_{g3,2}$, $V_{g4,1}$, and $V_{g4,2}$ are given in Figures 15(a) and (b), respectively.

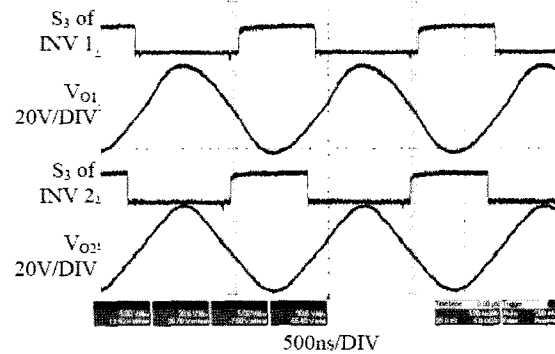


(b) With PPM control

Fig. 14 Current sharing improvement with phase angle control

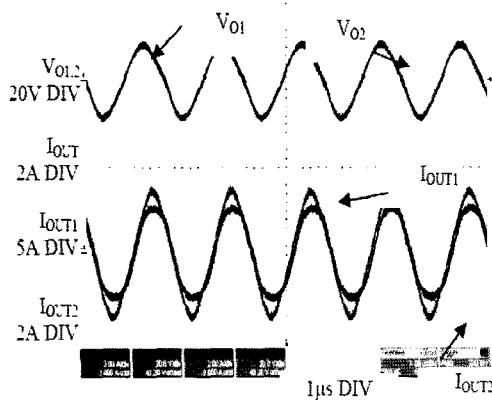


(a) Gating signals



(b) Output voltages of two modules

Fig. 15 Detailed experimental waveforms of the inverters system



(a) Without PPM control

5. Conclusions

The phase angles of the output voltage of the resonant inverters are different from each other, making it very

difficult for parallel operation of multiple resonant inverters. There are mainly three factors that contribute to the phase discrepancy. 1) The phase angle of the inverter output voltage is free from control in the conventional modulation methods. Therefore, even for the same pulse modulation signal, the output voltage phases can be different because of the power stage diversity such as load conditions and component tolerance of the resonant and switch components. 2) The time delays in the control and gate drive circuits make it impossible to synchronize the pulses. 3) For all the conventional resonant inverters, the phase angle of the output voltage changes with the modulation levels of the modulators, which changes for voltage regulation. In other words, the phase angle of the output voltage is coupled with the magnitude control. The differences in the output voltage phase angles of individual inverters cause circulating currents, and decrease the system efficiency. In order to reduce the circulating currents, effective control of the phase angle of the resonant inverter is expected.

A pulse phase modulation concept was proposed for the resonant inverter, so that the phase angle of the output voltage can be regulated. The mechanism of the pulse phase modulation was explained, and the PPM-controlled half-bridge resonant inverter was analyzed, and experimentally verified. The PPM control can be used to control the phase angles of the two-stage resonant inverters in a multiple resonant inverter system to reduce the circulating current, which is caused by phase discrepancy between modules. It can also be used in combination with PWM control to regulate both the phases and magnitudes of the output voltages, to minimize the circulating current in a multiple resonant inverter system. Experimental verification was presented with prototype resonant inverters of 100W, 500 kHz and output voltage 28V (RMS).

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