A Quadrature VCO Exploiting Direct Back-Gate Second Harmonic Coupling

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Abstract

This paper proposes a novel quadrature VCO(QVCO) based on direct back-gate second harmonic coupling. The QVCO directly couples the current sources of the conventional *LC* VCOs through the back-gate instead of front-gate to generate quadrature signals. By the second harmonic injection locking, the two *LC* VCOs can generate quadrature signals without using on-chip transformer, or stability problem that is inherent in the direct front-gate second harmonic coupling. The proposed QVCO is implemented in 0.18 μm CMOS technology operating at 2 GHz with 5.0 mA core current consumption from 1.8 V power supply. The measured phase noise of the proposed QVCO is −63 dBc/Hz at 10 kHz offset, −95 dBc/Hz at 100 kHz offset, and −116 dBc/Hz at 1 MHz offset from the 2 GHz output frequency, respectively. The calculated figure of merit(FOM) is about −174 dBc/Hz at 1 MHz offset. The measured image band rejection is 46 dB which corresponds to the phase error of 0.6°.

Key words : Back-Gate Coupling, CMOS, Injection Locking, Quadrature VCO, Second Harmonic Coupling.

I. Introduction

With the demand for lower cost and higher integration of wireless transceiver building blocks, a low power design is a great concern for radio frequency integrated circuit(RFIC) designers. For the digital wireless transceivers, a quadrature voltage controlled oscillator(VCO) plays an important role to down-convert the received radio frequency signal or up-convert the baseband analog signal with mixers.

Many papers have described how to generate accurate quadrature signals[1]~[4]. The most popular method is to use a differential VCO running at double the frequency of the desired frequency, and then to obtain quadrature waveforms via frequency division. However, a higher oscillation frequency and the frequency division result in increased power consumption. As well, this approach generally shows poor quadrature accuracy, as it requires an accurate 50 % duty cycle VCO[4].

Another way is to force two cross-coupled differential *LC* VCOs to run in quadrature by coupling transistors. This technique exploits a good phase noise performance of *LC*-oscillators. Examples of quadrature VCO(QVCO) topologies have been published by directly coupling two *LC* VCOs[2]~[5] as shown in Fig. 1(a) and (b). The third way is based on two injection locked oscillators with a second harmonic coupling using an on-chip transformer[6]. However, the on-chip transformer occupies a large die area while achieving a good phase noise performance. The fourth way is to exploit the direct front-gate second harmonic coupling as shown in Fig. 1(c)[7]~[10]. In this method, the source nodes of each current source should be degenerated with resistors to reduce the transconductance of the current source coupling transistor, *Mc*, which is necessary for stability. If the loop gain of the current source is higher than one, then a parasitic oscillation occurs and thereby results in an AM modulated output waveform[7]. Furthermore, the degenerated resistor consumes voltage headroom.

In this paper, a direct back-gate second-harmonic coupling quadrature VCO is proposed, in which the current source coupling transistors are coupled through body-terminals called back-gates. By doing that, the new QVCO does not use the large size on-chip transformer, and overcomes the stability problem since the back-gate input gives a lower gain[11].

II. Circuit Design

Quadrature VCO based on back-gate coupling is verified in [5] as shown in Fig. 1(b). By the same token, the technique can be utilized for the second harmonic coupling. Fig. 2 shows the proposed direct back-gate second-harmonic QVCO. The oscillator design is based on the complementary cross-coupled differential pair that uses a symmetric inductor that has a differential value of 5.9 nH with a differential Q factor of 11 around 2 GHz, which is 1.5 times higher than that of the singled

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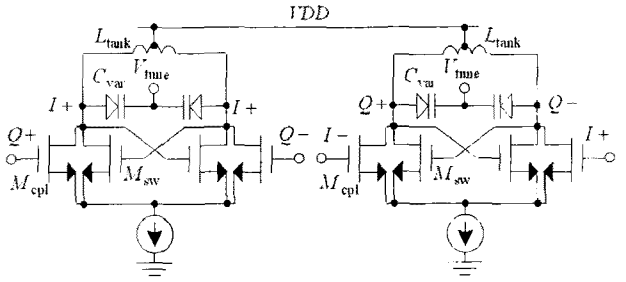
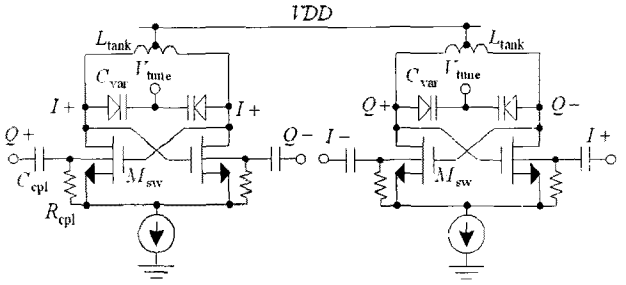
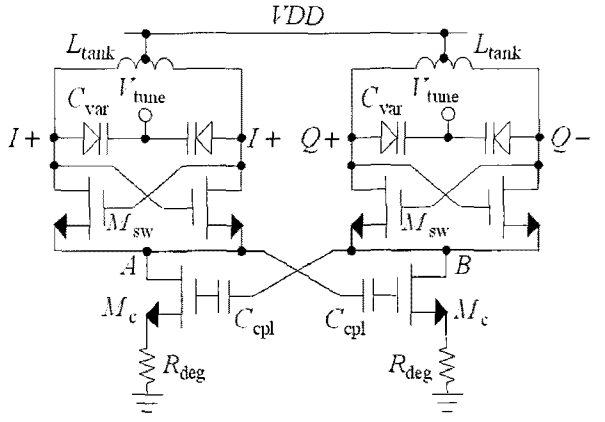


(a) Conventional parallel-coupled QVCO



(b) Parallel back-gate coupled QVCO



(c) Direct front-gate second harmonic coupling (bias is not shown)

Fig. 1. Several quadrature VCO topologies.

ended inductor. The MOS varactor with a total width of 60 μm and a channel length of 1 μm has a minimum value of 170 fF and a maximum value of 470 fF with tuning voltage of ±0.3 V gate bias voltage around 0 V.

The two LC oscillators are direct coupled at common nodes of V_{s1} and V_{s2} through the back-gate terminal with the resistor and capacitor network.

Without using a large size transformer or resistors for source degeneration, the proposed QVCO reduces the power consumption while achieving the low phase noise and quadrature waveforms. When the current source of M_c are cross-coupled with C_c and R_c, the coupling forces the second harmonic to be 180° out of phase, which in turn forces each LC oscillator to generate quadrature signals. During the first period of oscillation, the coupling would try to force each second harmonic signal to

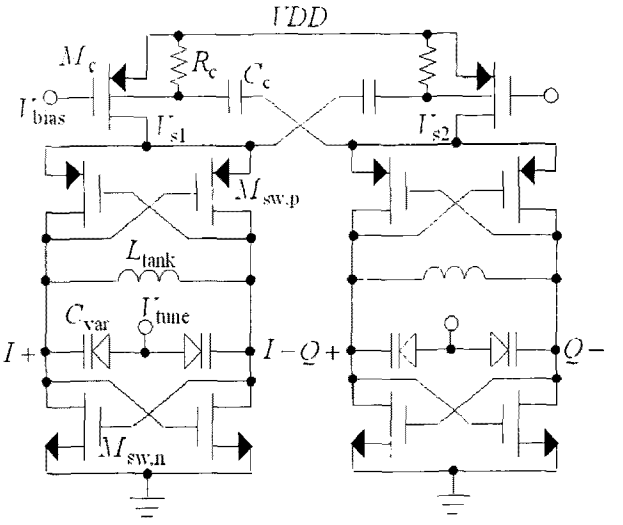


Fig. 2. Proposed direct back-gate second-harmonic coupling QVCO.

180° out of phase, but actually would be less than 180°. During the following period, the injection locking would continuously force the two oscillators to run at 180° out of phase, and finally generate quadrature signals.

As the inherent device noise causes small perturbation in the waveforms, the injection locking forces the two oscillators to generate quadrature signals. These phenomena are the same with those presented in using transformer or front-gate injection locking[4],[5].

It can be verified by forcing the two oscillators to start in-phase and finally generate quadrature signals. Perfect quadrature signals can be achieved when the two oscillators match perfectly. However, for small tank mismatches, the injection-locking will still force the two oscillators in quadrature with a small quadrature error. To set the sequence of in-phase and quadrature signals, a small size PMOS ring oscillator is added in parallel with the tank[4]. The ring oscillator is designed to consume around one-seventh of the oscillator core current and thereby degrades the overall phase noise performance very little. Simulation results show that the QVCO can be designed to have the phase error less than 5° by setting up ±0.5 % inductor mismatch and choosing appropriate ring oscillator size.

Ⅲ. Measurement Results

To verify the proposed idea, the circuit has been fabricated in SMIC's 0.18 μm CMOS technology. The fabricated chip is shown in Fig. 3. The chip size is 700× 1,200 μm^2 including the pads. All the pads are electrostatic discharge(ESD) protected to prevent from an unexpected high voltage discharge.

For the buffers, small size transistors are used to mi-

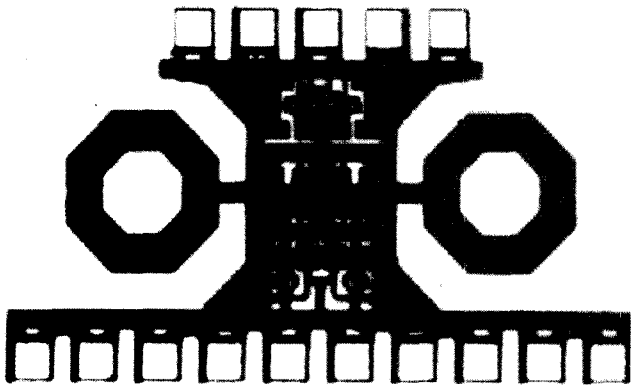
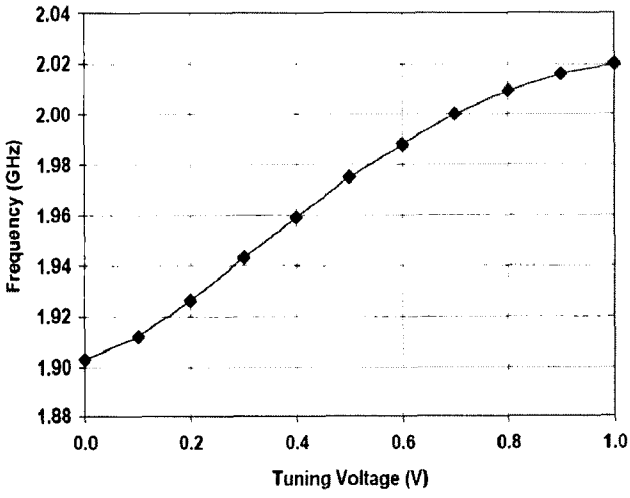
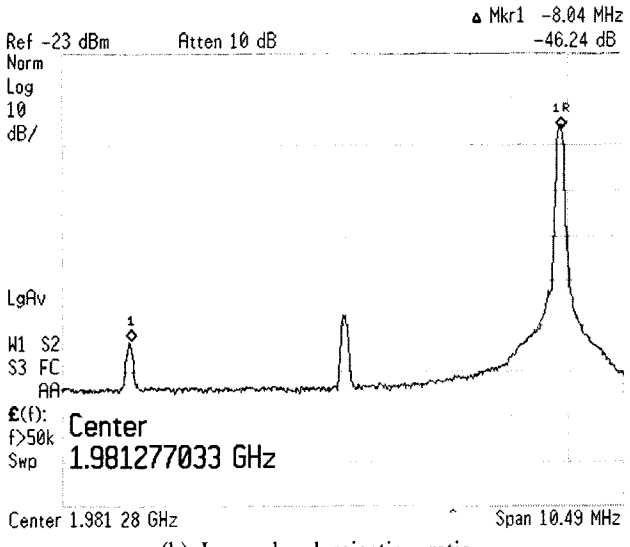


Fig. 3. Chip micrograph. The die size is 700×1,200 μm^2.

nimize the frequency shift of the oscillation frequency. Also, a passive single sideband(SSB) mixer is implemented on-chip to measure the image band rejection (IBR) which is directly related to the in-phase (I) and quadrature (Q) mismatch in real chip implementation.



(a) Tuning range



(b) Image band rejection ratio

Fig. 4. Measurement results from the SSB mixer output.

Octagonal-shape symmetric inductors are implemented for the tank to have higher quality factor rather than using single-ended inductors.

Fig. 4 shows the measured tuning range, and the output spectrum of the SSB mixer up-converter. An accurate 4 MHz baseband signal is applied to the SSB mixer from the Agilent Vector Signal Generator to measure the IBR. As shown in Fig. 4(b), the measured IBR is 46 dB, which corresponds to the phase error of about 0.6° assuming the IBR is entirely caused by I/Q phase error.

Fig. 5 shows the phase noise performance. The measured phase noise is −63 dBc/Hz at 10 kHz offset, −95 dBc/Hz at 100 kHz offset, and −116 dBc/Hz at 1 MHz offset from the 2 GHz output frequency, respectively. Table 1 summarizes the measurement results of the proposed QVCO compared to those of other low phase noise VCOs.

Ⅳ. Conclusion

In this paper, a novel quadrature VCO is proposed by exploiting an injection locking through a direct back-gate coupling between the two LC VCOs. Operating at around 2 GHz, the proposed VCO is implemented using 0.18 μm CMOS technology. With 5.0 mA core current consumption from a 1.8 V power supply, the proposed VCO achieves the phase noise performance of −116

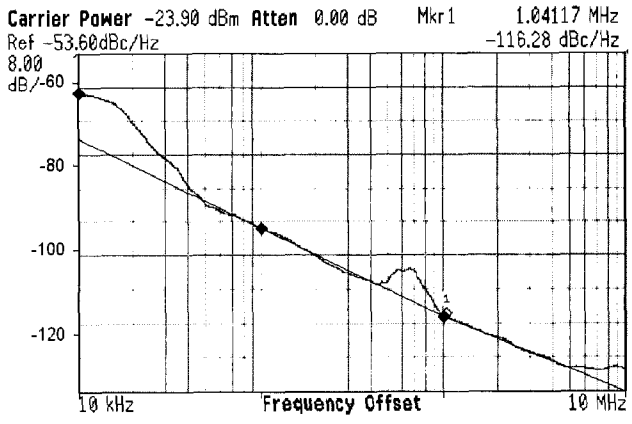


Fig. 5. Measured phase noise performance.

Table 1. Performance comparison of low phase noise VCOs.

Ref.	Freq. [GHz]	Power [mW]	Phase noise [dBc/Hz]	FOM [dBc/Hz]	Tech. [μm]
[5]	1.1	5.4	−120 [@1M]	−173.5	0.18
[8]	2	26.5	−126.5 [@1M]	−178.3	0.13
[12]	2.45	7.2	−119 [@1M]	−178.0	0.18
This work	1.91~2.01	9	−116 [@1M]	−174	0.18

dBc/Hz at 1 MHz offset frequency and the phase error of about 0.6°. The calculated figure of merit(FOM) of the proposed VCO is about −174 dBc/Hz at 1 MHz offset, which is comparable to other low phase noise VCO performance.

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