High Performance Wilkinson Power Divider Using Integrated Passive Technology on SI-GaAs Substrate

Cong Wang · Cheng Qian · De-Zhong Li · Wen-Cheng Huang · Nam-Young Kim

Abstract

An integrated passive device(IPD) technology by semi-insulating(SI)-GaAs-based fabrication has been developed to meet the ever increasing needs of size and cost reduction in wireless applications. This technology includes reliable NiCr thin film resistor, thick plated Cu/Au metal process to reduce resistive loss, high breakdown voltage metal-insulator-metal(MIM) capacitor due to a thinner dielectric thickness, lowest parasitic effect by multi air-bridged metal layers, air-bridges for inductor underpass and capacitor pick-up, and low chip cost by only 6 process layers. This paper presents the Wilkinson power divider with excellent performance for digital cellular system(DCS). The insertion loss of this power divider is −0.43 dB and the port isolation greater than −22 dB over the entire band. Return loss in input and output ports are −23.4 dB and −25.4 dB, respectively. The Wilkinson power divider based on SI-GaAs substrates is designed within die size of 1.42 mm^2.

Key words : Integrated Passive Devices, Wilkinson Power Divider, SI-GaAs Substrate, DCS.

I. Introduction

Integral passive is an emerging technology, primarily due to the needs of handheld wireless devices to further decrease in cost and size and increase in performances [1],[2]. Radio transmit modules for cellular phones continue to shrink in die size and cost, requiring novel approaches for integration of the numerous passive elements of the radio front-end. Many functional blocks, such as harmonic filters, couplers, baluns, and power combiners/dividers, in the RF modules can be realized by using IPD technology[3]~[5]. Fig. 1 indicates IPD technology widely used in today's mobile phone front-end RF sections, due to the facts that IPDs are generally fabricated using standard wafer fabrication technologies such as thin film and photo-lithography processing; they can be manufactured with low cost and small size with excellent reproducibility. In this paper, the design and fabrication of a 3 dB Wilkinson power divider assembly for the DCS radio band is described.

II. GaAs Integrated Passive Device Process

In this paper, RF integration passive device such as MIM capacitors, thin film resistors, high Q inductors and a Wilkinson power divider is implemented and used only 6 masks to realize the design. Fig. 2 presents a cross-sectional view of GaAs integrated passive devices. To achieve cost and size reductions, a low cost manufac-
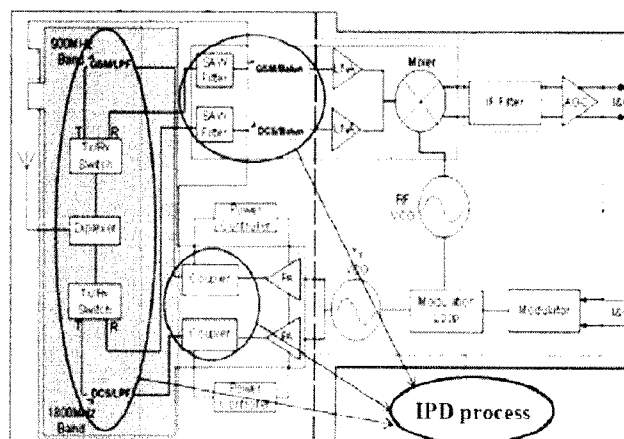

Fig. 1. Integrated transceiver architecture.

turing technology for RF substrates and a high performance passive process technology are developed for RFIPDs.

The fabricated substrate is a conventional 6 inch SI-GaAs wafer with 0.625 mm thickness. This substrate is advantageous to avoid the capacitive and inductive loading of the other conductive substrate for high speed micro-electronics applications[6] and shows a good permittivity of 12.85, and a loss tangent of 0.006.

NiCr with a thickness of 700 Å is used to form resistors and MIM capacitors are formed by sandwiching 2,000 Å of Si$_3$N$_4$ between two thick Cu/Au plates. All components are measured and equivalent electrical models are established in ADS simulator. Therefore, every
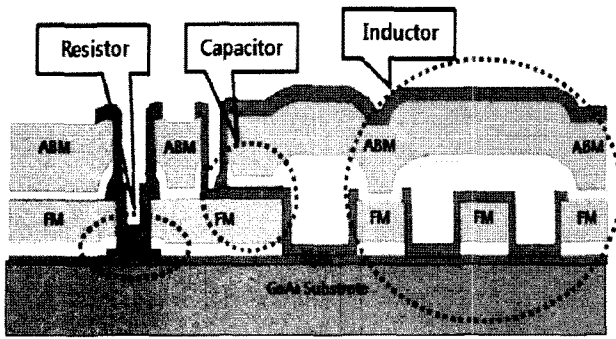
Fig. 2. Cross-sectional view of GaAs IPDs.

passive functional block such as divider, filter, balun, coupler, matching network can be implemented using IPD technology.

The process features two levels of plated Cu/Au metal with thicknesses of Cu 4.5 μm and Au 0.5 μm for first metal and Cu 3.0 μm and Au 2.0 μm for second metal. All plated metals use Ti/Au 200 Å/800 Å seed sputtering prior to plating in order to increase the metal adhesion of the substrate[7]. The whole process starts with a bottom passivation layer which is composed of Si_3N_4 and is deposited by plasma enhanced chemical vapor deposition(PECVD) to thickness of 2,000 Å with permittivity of 7.5, and loss tangent of 0.002. And then a 700 Å deposition of NiCr metallization is used for thin film resistors. This transition metal alloy exhibits a wide range of resistivity, low temperature coefficient of resistance (TCR) from +80 to -250×10^{-6} /°C, high stability of electrical properties and is reactively evaporated. Usually the NiCr contains 80 % Ni and 20 % Cr to get the optimal performance. 3 sigma variationsm of the resistor values is 1.2 % in this process. The variation depends on the width and length of the resistors and also thickness of NiCr. Wider and longer resistors and thicker thickness exhibit smaller variations[8]. After evaporating NiCr, conventionally Cu/Au first metal is used as the contact metallization for NiCr resistors, as the first metal layer for MIM capacitor and also as metal beelines and rings for spiral inductor. The reason for using copper is that it has a relatively higher conductivity, high-speed operation, less expensive compared to gold and is easily solder-able[9]. After patterning the resistors and the bottom metal part of capacitor/inductor with reactive ion etch, 2,000 Å of PECVD is deposited as the capacitor middle dielectric part. And then, an air-bridge photo process is performed prior to Cu/Au second metal definition and plating for making top metal for capacitors and interconnection between metal beelines and rings for inductors. So capacitors are formed with first metal bottom plate and second metal top plate and a dielectric result in density of 330 pF/mm² which depends on the dielec-

tric part thickness. Inductors consist of 5 μm Cu/Au metal rings and underpass of a stack of first metal and second metal. Finally, all components are passivated with thickness of 3,000 Å Si_3N_4.

III. Components and Process Optimization

NiCr resistance is very sensitive to deposition parameters, pre-clean, and substrate conditions. In-wafer and wafer-to-wafer uniformity and NiCr reactivity have been the biggest manufacturing challenge for both types of processes. In order to solve this issue, a thicker NiCr deposition 700 Å and a slower deposition rate 1 Å/s are selected. It shows very good sheet resistance uniformity from 20.55 to 21.16 $\Omega/\square$ than the other process[10].

Through the above manufacturing process, inductors with air-insulated planar metal interconnections having low parasitic constant is achieved. Using thick plated low-resistance Cu/Au air-bridge metal layer can provide a very low resistance loss, thereby providing improved RC time constants and accordingly the transmission characteristic of inductor was increased. And also various parameters such as inner diameter, metal thickness and width have been optimized to provide inductors with high quality factors in excess of 27 over the frequency range 1~5 GHz than the other process[11]. Fig. 3(a) and (b) show the comparison between Freescale Semiconductor Inc. and this work in Q factor of inductor with 250 μm inner diameter.

Due to increasing capacitance per unit area by reducing thickness of the dielectric film, MIM capacitors die size can be reduced. In this process, a pre-cleaning for the bottom metal by ultrasonic methanol and isopropyl alcohol is used. This treatment produces smoothness improvement and dielectric reduction.

IV. Wilkinson Power Divider Design

The basic divider schematic circuit is shown in Fig. 4, which consists of π lumped-element equivalent net-

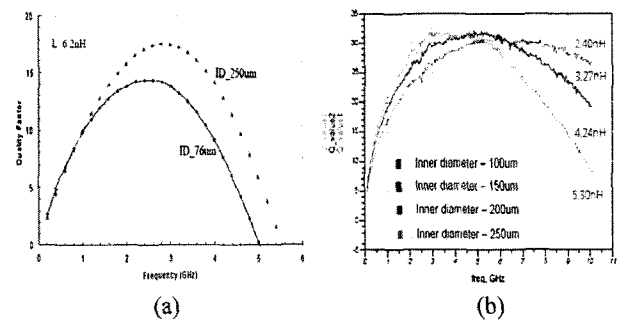(a)   (b)

Fig. 3. (a) Q factor of inductor fabricated by Freescale,
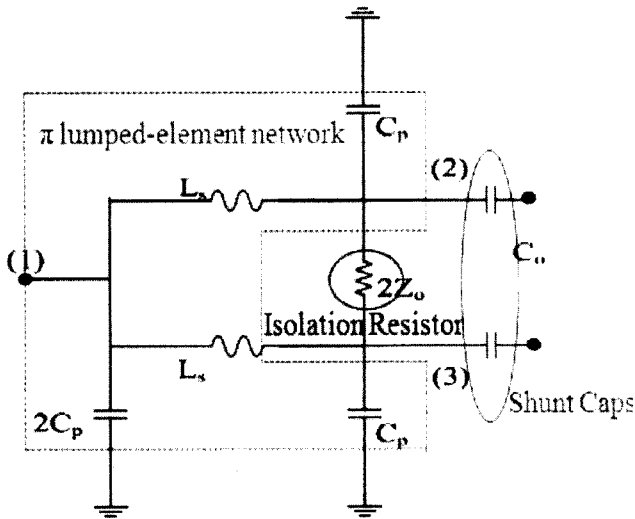(b) Q factor of inductor fabricated in this work.

Fig. 4. Schematic circuit of Wilkinson power divider.

Fig. 5. Simulation of S-parameters.

works, and a 100 Ω isolation resistor. The circuit is designed for application to DCS band and the design has input and output impedance of 50 Ω using shunt capacitors C_o tuning out the resistor and pad parasitic to avoid performance degradation in the output ports.

This design uses 6.25 nH inductor Ls and appropriate 1.25 pF capacitors C_p which are selected through optimization with Agilent's ADS for the π lumped-element equivalent networks. The shunt capacitor C_o values are tuned using EM simulator Sonnet. EM simulation is essential, particularly as die size is reduced by compacting components to meet the targets, since coupling effects of compact components cannot capture by the ADS software alone.

V. Wilkinson Power Divider RF Characterization

The power divider circuit as presented above is implemented in π lumped-element circuit. Simulation results are superimposed in Fig. 5 respectively. S_{11} and S_{22} represent the return loss; S_{21} and S_{31} represent the insertion loss at ports 2 and 3. S_{23} is the isolation between ports 2 and 3. Detailed circuit layout and photograph of the fabricated power divider are shown in Fig. 6 with a die size of 1.42 mm^2. The Wilkinson power divider is fabricated using the aforementioned IPD technology on a SI-GaAs wafer and the RF characterization is performed using a network analyzer. Fig. 7 shows plots of the measured characteristics. In this case, the insertion loss is below 0.5 dB and the port isolation close to and greater than 20 dB over the entire frequency band. And return loss in input and output port are less than -20 dB, respectively. The detailed measurement results compared with the specifications are shown in Table 1.
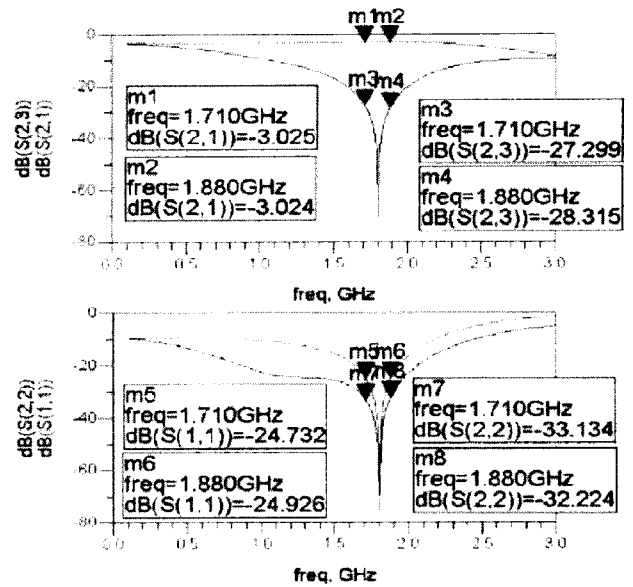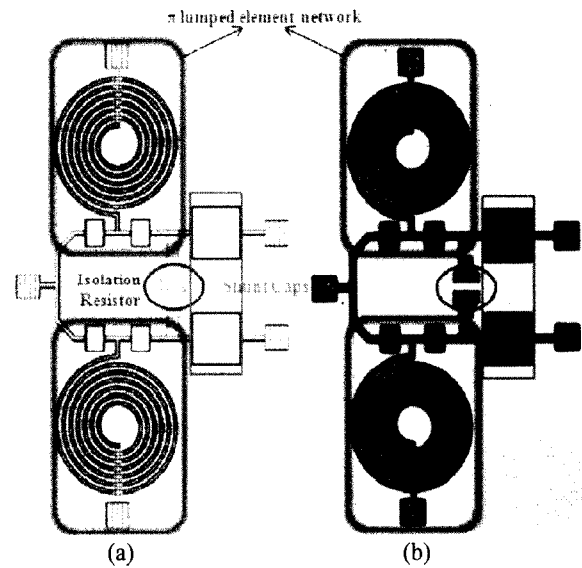

Fig. 6. (a) Layout of the designed power divider, (b) Fabricated of the same power divider.

Table 1. Summary of the measurement results.

Requirement	Standard	Unit	Measurement
Frequency	1.710~1.880	GHz	1.62~1.92
Center freq.	1.800	GHz	N/A
Insertion loss	-3.5 dB max	dB	-3.43
Return loss (Input)	-20 dB min	dB	-23.4
Return loss (Output)	-20 dB min	dB	-25.4
Isolation	-20 dB min	dB	-22.3
Port impedance	50	Ohm	50
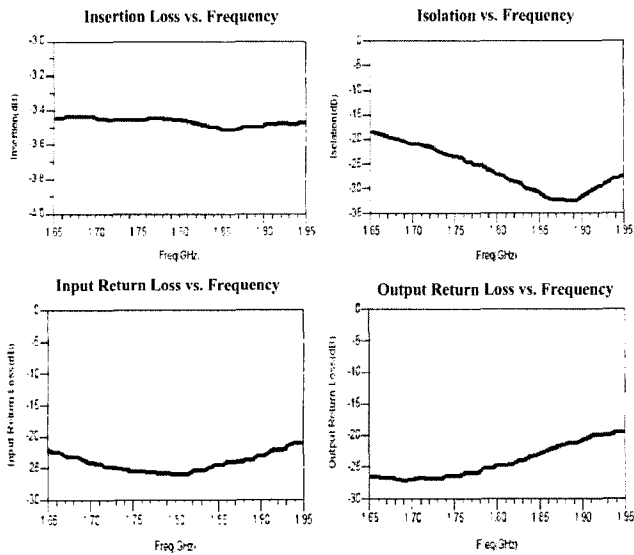
Fig. 7. Measured RF performance of 3 dB Wilkinson power divider.

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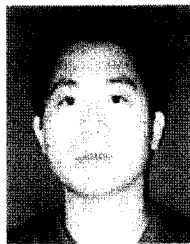
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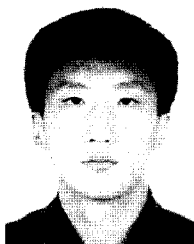
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