A 3~5 GHz UWB Up-Mixer Block Using 0.18-μm CMOS Technology

Chang-Wan Kim

Abstract

This paper presents a direct-conversion *I/Q* up-mixer block, which supports 3~5 GHz ultra-wideband(UWB) applications. It consists of a VI converter, a double-balanced mixer, a RF amplifier, and a differential-to-single signal converter. To achieve wideband characteristics over 3~5 GHz frequency range, the double-balanced mixer adopts a shunt-peaking load. The proposed RF amplifier can suppress unwanted common-mode input signals with high linearity. The proposed direct-conversion *I/Q* up-mixer block is implemented using 0.18-μm CMOS technology. The measured results for three channels show a power gain of −2~−9 dB with a gain flatness of 1 dB, a maximum output power level of −7~−14.5 dBm, and a output return loss of more than −8.8 dB. The current consumption of the fabricated chip is 25.2 mA from a 1.8 V power supply.

Key words : CMOS, Driver Amplifier, Direct-Conversion, Mixer, Wideband, Ultra-Wideband, UWB.

I. Introduction

The ultra-wideband(UWB) system has emerged as a major technology for high data-rate service in wireless communication systems. The unlicensed UWB band has been allocated between 3.1 GHz and 10.6 GHz, and the spectrum shape of modulated output power and maximum power level are limited(−41.3 dBm/MHz) by the Federal Communications Commission(FCC)[1],[2]. Currently, two UWB approaches for the Wireless Personal Area Network(WPAN) use carriers, similar to conventional wireless systems : MB-OFDM(Multi-Band Orthogonal Frequency Division Multiplexing)[3]~[7] and DS-CDMA(Direct-Sequence Code Division Multiple Access)[8]. The MB-OFDM approach has inherent robustness against narrow-band interferers and multi-path environments when compared to the DS-CDMA approaches. In addition, the MB-OFDM approach divides the UWB band(3.1~10.6 GHz) into several sub-bands with a bandwidth of 528 MHz, and then once again classifies them into six groups[2]. In this way, the MB-OFDM approach can use its frequency band more flexibly. The lowest group(3,168 ~4,752 MHz) is decided as a mandatory mode(Mode 1) in the MB-OFDM system, which can provide a more than 480 Mb/s data-rate[2]. Mode 1 UWB devices support three channels, 3,168~3,696 MHz(Channel 1), 3,696~4,224 MHz(Channel 2), and 4,224~4,752 MHz(Channel 3), as shown in Fig. 1. Each channel is hopped within 9.5n sec to increase data capability. Recently, many CMOS UWB transceivers for mode 1 have been reported[3]~[7].

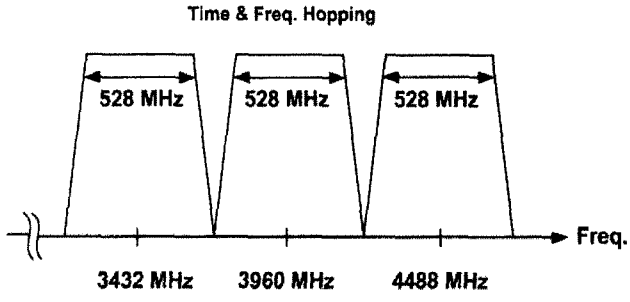

Fig. 1. Frequency location for Mode 1 UWB devices.

This paper proposes an UWB direct-conversion *I/Q* up-mixer block, which can support the MB-OFDM transmitters(Mode 1). The proposed *I/Q* up-mixer block adopts a VI converter to process a large input voltage signal from baseband circuits like a baseband VGA or a LPF, a proposed RF amplifier to improve the mixer gain, and a differential-to-single(D2S) converter for converting differential output signals from the RF amplifier into single-ended signals.

II. Design of Circuits

The transmitters for the MB-OFDM UWB system can be implemented by using heterodyne or direct conversion architecture. Comparing with the heterodyne architecture[6], the direct conversion architecture has conventionally several advantages like high integration, low dc-power consumption, low cost, and so on [3]~[8]. In addition, the direct conversion transmitters generate less amounts of unwanted transmit-signals(LO harmonics, IM

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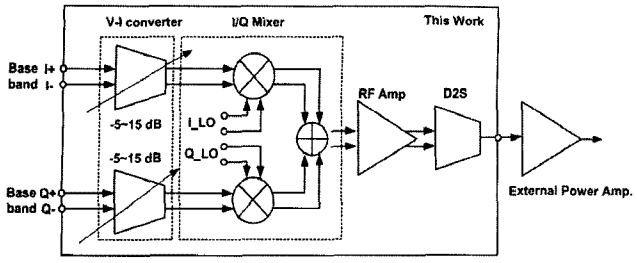


Fig. 2. Block diagram of the proposed direct-conversion *I/Q* up-mixer block.

components, and other mixing products) form the up-mixer, because it converters the baseband input signals to RF carriers using only a LO oscillator.

Fig. 2 shows a simplified block diagram of the proposed direct-conversion *I/Q* up-mixer block. It consists of an *I/Q* VI converter, an *I/Q* double-balanced mixer, a RF amplifier, and a differential-to-single(D2S) converter. In Fig. 2, the *I/Q* baseband voltage input signal is first converted into a current signal by the *I/Q* VI converter, and then up-converted into RF frequency by the *I/Q*-mixer. Three *I/Q*-LO tones(3,432 MHz, 3,969 MHz, and 4,488 MHz) are externally provided from a multi-LO tone generator for the *I/Q* up-mixer in Fig. 2. The RF amplifier follows the *I/Q*-mixer to provide more power gain and suppress unwanted common-mode noises generated from the output node of the mixer. The D2S converts the differential output signal of the RF amplifier into a single-ended signal, which is also matched to 50 over 3~5 GHz frequencies.

To accommodate a large input voltage baseband signal, the proposed *I/Q* mixer circuit adopts a VI converter in Fig. 3 as its transconductance stage. In Fig. 3, by negative feedback operation, constant current I_1 flows through the input transistor M_1 and M_2 such that the individual gate-source voltage v_{GS1} and v_{GS2} always re-

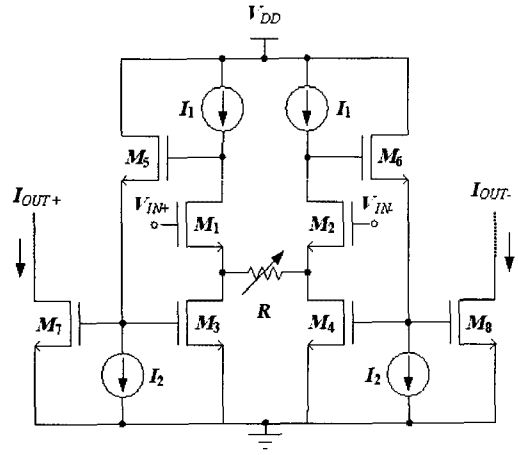


Fig. 3. CMOS VI converter(*I*-path).

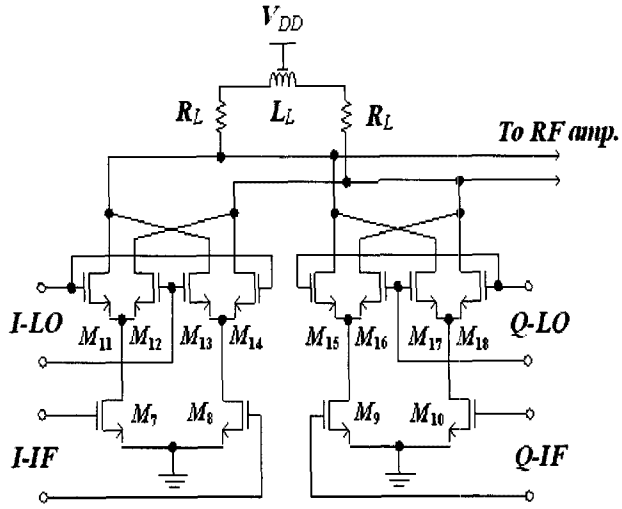


Fig. 4. Proposed CMOS *I/Q* double-balanced mixer.

main constant[9]. As a result, input transistor M_1 and M_2 can operate in a saturation region up to a large input voltage swing of 300 m V_{pp}, leading to high input linearity. As shown in Fig. 3 and 4, the baseband input voltage signal V_{in+} and V_{in-} are converted to the current signal by NMOS transistors M_7 and M_8(Fig. 4), and then provided to the common-source node of switching transistors M_{11}~M_{14} in the up-mixer in *I*-path for frequency up-conversion. With the same operation, the converted current signal from the VI converter in *Q*-path is also provided to the common-source node of M_{15}~M_{18} in the *Q*-path up-mixer. The overall transconductance of the VI converter in Fig. 3 is approximately $1/R$ with low dc current consumption with 1 mA from a 1.8 V supply voltage. The resistor R is implemented using a NMOS transistor in the triode region, which is controlled by an external voltage source to provide a voltage gain variation from −5 dB to 15 dB. In Fig. 4, the modulated output currents from the *I/Q* mixer are summed and converted into a voltage signal at the shunt-peaking load (L_L and R_L)[10], which provides a flat gain over 3 GHz to 5 GHz frequencies. In Fig. 4, the value of R_L is 50 ohm and L_L is 2 nH. the *I/Q* mixer draws 14 mA from a 1.8 V supply.

Fig. 5 shows the proposed RF amplifier, which combines the common-source(M_1 and M_2) amplifier and common-drain(M_3 and M_4) amplifier. A general differential amplifier with a tail-current source is the most widely used circuit in RF and analog circuits because it can suppress common-mode noise signals. In high linear applications, the common-source node of input transistors in the differential amplifier is usually directly connected to the ground to achieve high linearity. However, this configuration degrades its common-mode rejection ability.

The proposed RF amplifier, as shown in Fig. 5, can

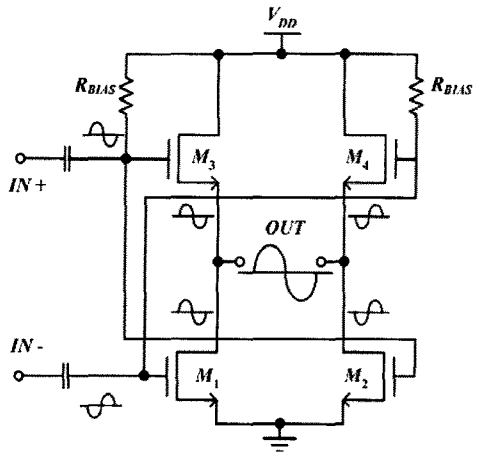


Fig. 5. The proposed CMOS RF amplifier.

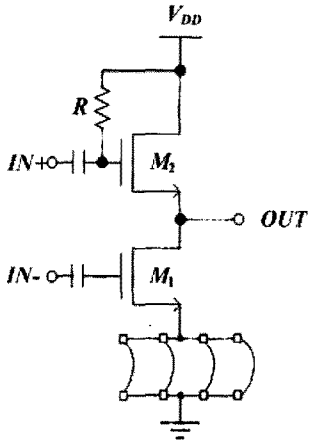


Fig. 6. Schematic of D2S.

suppress unwanted common-mode signals with high linearity. In Fig. 5, the common-source node of M_1 and M_2 is directly connected to the ground in order to achieve sufficient linearity. This topology can suppress unwanted strong common-mode input signals generated from the mixing operation of the *I/Q* double-balanced mixer, while providing high voltage gain for wanted differential input signals. The operation of this amplifier can be described as follows: when an incoming signal is in differential mode, NMOS transistors M_1 and M_2 work as the common-source amplifier; while M_3 and M_4 work as the source follower. Accordingly, all amplified differential signals are added in the in-phase at output node as shown in Fig. 5. For common-mode input signals, however, all amplified signals by M_1, M_2, M_3, and M_4 are added in out-of-phase at output node, so that the in-phase input signals are cancelled out. The simulated cancellation ratio of the proposed amplifier shows about 15 dB at 3 GHz, 12 dB at 4 GHz, and 10 dB at 5 GHz. This topology also provides a sufficient wideband characteristics. The common-drain amplifier(M_3 and M_4) inherently shows inherently very wideband characteristics[11] and the common-source amplifier(M_1 and M_2) has low values of resistive loads, $1/g_{m3}$ and $1/g_{m4}$, respectively. The simulated -3 dB cut-off frequency is up to 6 GHz.

The method to convert differential signal into single-ended signal is also a design issue in the wideband applications. The D2S circuit shown in Fig. 6 is used to convert the differential signal from the output node of the RF amplifier in Fig. 2 to the single-ended signal for direct connection to the off-chip single-ended power amplifier. To completely sum the differential input signal at output node in the in-phase, several bonding wires are in parallel connected to the source node of NMOS transistor M_1 in Fig. 6. The output of the D2S is matched to 50 ohm over 3~5 GHz with a small value of output impedance $1/g_{m2}$.

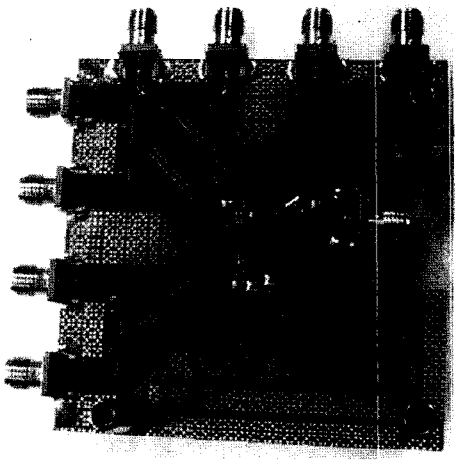


Fig. 7. Photograph of test board.

III. Measurements and Summary

Fig. 7 shows the test board for the proposed *I/Q* up-mixer block, which is fabricated in 0.18 μm CMOS technology. The fabricated core chip size without pads is 1.2 mm^2. The chip is packaged(MLF RF package) and mounted on the FR4 PCB for measurements. LO and IF signals are externally provided from signal generators. All measurements are performed in the *I*-path circuits.

Fig. 8 shows the measured output return loss(S_{11}) of the fabricated chip, which shows lower than -8.8 dB over 3~5 GHz.

In this work, it's very difficult in externally providing reliable *I/Q* banseband signal with a bandwidth of dc to 264 MHz and three LO tones(3,432 MHz, 3,960 MHz, and 4,488 MHz) into the fabricated chip respectively. Accordingly, only in-phase baseband 100 MHz signal of -20 dBm and three LO tones of -3 dBm are externally provided to the chip in this work. Fig. 9 shows the measured output power level for three channels is -28 dBm,

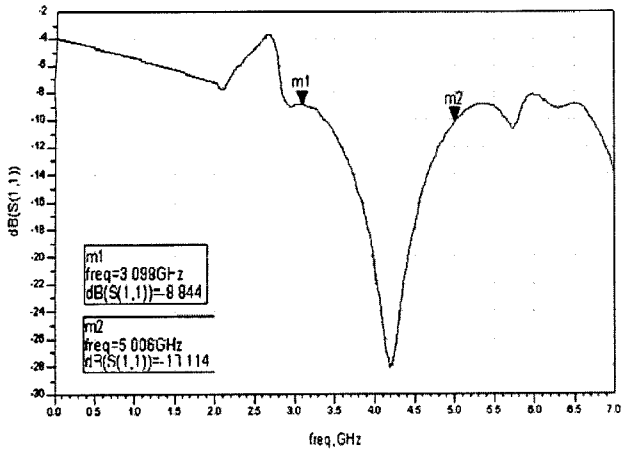
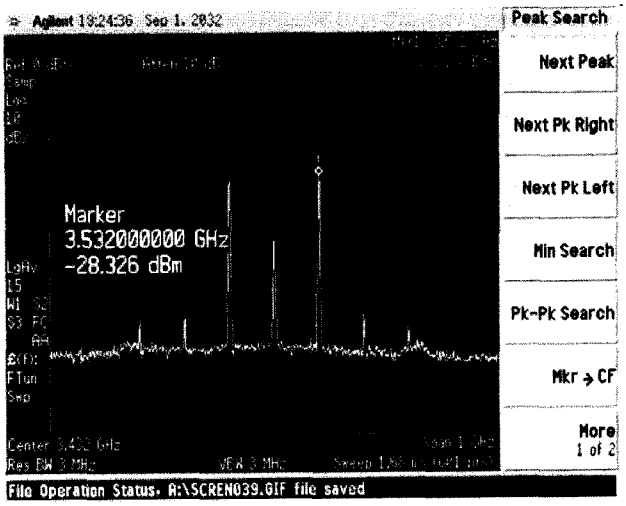


Fig. 8. Measured output return loss (S_{11}).

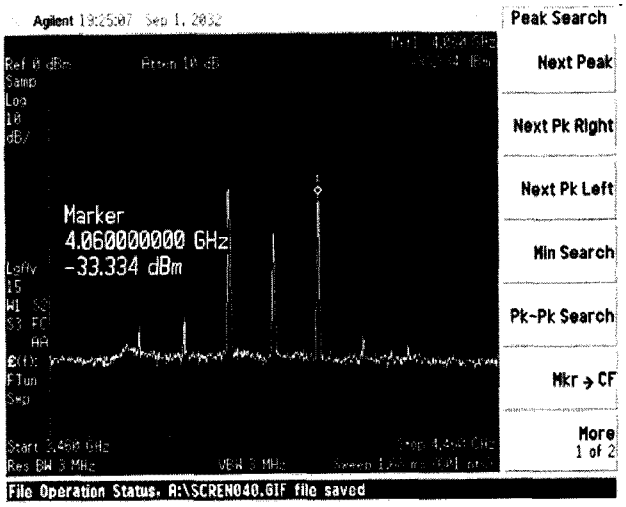
Table 1. Comparison between the simulation and measurement results.

	Simulation		Measurements	
Power gain (Channel 1)	−1.6 dB		−2 dB	
Power gain (Channel 2)	−1.5 dB		−7 dB	
Power gain (Channel 3)	−1.3 dB		−9 dB	
Output reutrn loss	>−14 dB		−8.8 dB	
Max. output power (dBm)	−4.3 dBm		−7/−12.3/ −14.5 dBm	
OIP_3(dBm)	+4.9 dBm		+2.1/−2.8/ −4.0 dBm	
Sideband rejection	>60 dBc			
DC power consumption	27 mA@ 1.8V		25.2 mA@ 1.8V	
	VI	2 mA	VI	1.7 mA
	MIXER	14 mA	MIXER	13 mA
	RF AMP	6 mA	RF AMP	6 mA
	D2S	5 mA	D2S	4.5 mA

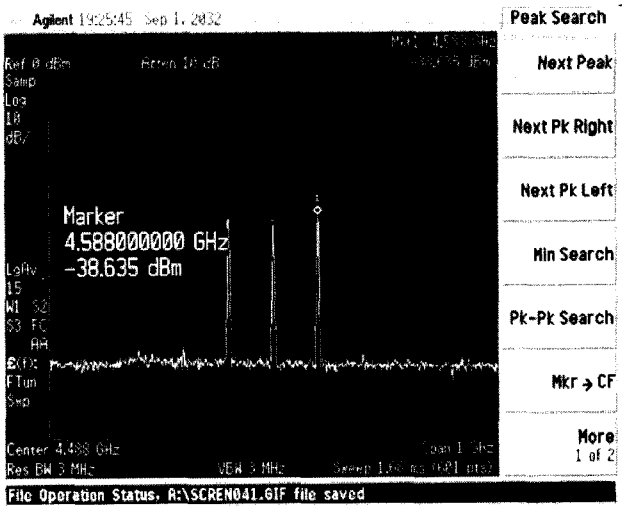
−33 dBm, and −38 dBm, respectively. If these applied baseband signal and LO signal are all quadrature signals, additional power gain of 3 dB should be added to the measured output power in Fig. 9. Finally, after calibrations for cable loss, PCB loss, and so on, the estimated power gain for each channel is −2 dB, −7 dB, and −9 dB, respectively. Especially, the measured power gain of channel 2 and 3 is very lower than that of the channel 1. These gain degradation in the channel 2 and 3 is mainly due to the unexpected reduction of the bandwidth of the shunt-peaking load in the up-mixer. In



(a) Channel 1



(b) Channel 2



(c) Channel 3

Fig. 9. Measured output spectrum.

the future revision design step, to improve the power gain in the channel 2 and 3, the shunt-peaking load of the up-mixer is more carefully designed, or can be replaced by a switchable LC resonant load. From Fig. 9,

the maximum LO leakage is less than −40 dBm when the external LO power level is −3 dBm. The simulation and measured results of this work are summarized in Table 1. The current consumption of this work is 25.2 mA from a 1.8 V power supply.

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References

[1] Ramesh Harjani, Jackson Harvey, and Robert Sainati, "Analog/RF physical layer issues for UWB systems", *VLSI Design, Proceeding 17th International Conference on*, pp. 941-948, 2004.

[2] Standard ECMA-368, *High Rate Ultra Wideband PHY and MAC Standard*, 2nd Edition, Dec. 2007.

[3] Behzad Razavi *et al.*, "UWB CMOS transceiver", *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2555-2562, Dec. 2005.

[4] LO Steve *et al.*, "A dual-antenna phased-array UWB transceiver in 0.18 μm CMOS", *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2776-2786, Dec. 2006.

[5] Christoph Sandner *et al.*, "A WiMedia/MBOA-compliant CMOS RF transceiver for UWB", *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2787-2792, Dec. 2006.

[6] Chang-Wan Kim, Sang-Sung Choi, and Sang-Gug Lee, "A CMOS frequency synthesizer block for MB-OFDM UWB systems", *ETRI Journal*, vol. 29, no. 4, pp. 437-444, Aug. 2007.

[7] Chang-Wan Kim *et al.*, "A 0.13-um CMOS UWB RF transmitter with an On-Chip T/R switch", *ETRI Journal*, vol. 30, no. 4, pp. 526-534, Aug. 2008.

[8] Bonghyuk Park, Kyungai Lee, Songcheol Hong, and Sangsung Choi, "A 3.1 to 5 GHz CMOS transceiver for DS-UWB systems", *ETRI Journal*, vol. 29, no. 4, pp. 421-429, Aug. 2007.

[9] David A. Johns, Ken Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc., 1997.

[10] Thomas H. Lee, *The Design of CMOS Radio-frequency Integrated Circuits*, Cambridge University Press, Second edition, 2004.

[11] Paul R. Gray *et al.*, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, Inc, 2001.

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