Multi-bit Sigma-Delta Modulator for Low Distortion and High-Speed Operation

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ABSTRACT—A multi-bit sigma-delta modulator architecture is described for low-distortion performance and a high-speed operation. The proposed architecture uses both a delayed code and a delayed differential code of analog-to-digital converter in the feedback path, thereby suppressing signal components in the integrators and relaxing the timing requirement of the analog-to-digital converter and the scrambler logic. Implemented by a 0.13 μm CMOS process, the sigma-delta modulator achieves high linearity. The measured spurious-free dynamic range is 89.1 dB for −6 dBFS input signal.

Keywords—Multi-bit sigma-delta modulator, feed-forward topology, low distortion, low voltage.

I. Introduction

Multi-bit architecture is a possible means to achieve high resolution and wide bandwidth using low-voltage technology in a sigma-delta modulator. However, improvement of the dynamic range cannot be easily achieved due to digital-to-analog converter (DAC) nonlinearity. Consequently, the multi-bit architecture should employ the noise shaping technique of DAC nonlinearity. For this function, scrambler logic is required; however, it can induce a timing constraint in some topologies, such as full feed-forward architecture. Furthermore, analog blocks for wideband applications require both high-speed and low-distortion properties, thus posing a significant challenge.

In this letter, we describe a multi-bit sigma-delta modulator which relaxes the distortion requirement of analog blocks, the timing requirement of the analog-to-digital converter (ADC) and the scrambler logic for high speed operation. In addition,

the proposed approach is thought to be suitable for low supply voltage operations because the signal component in the loop filter is suppressed.

II. Previous Work

Figure 1(a) shows the architecture of a traditional second-order sigma-delta modulator. This architecture requires low-distortion analog blocks to satisfy the system distortion requirement in case of low oversampling ratio (OSR) operation. The outputs of the first and second integrator include the input signal component with full amplitude. Because of opamp nonlinearity, harmonic components are generated at the outputs of the integrators in $x1$ and $x2$. These components appear at the output of the modulator in y, shaped by first- and second-order highpass transfer functions, respectively [1]. Due to the highpass transfer function, low OSR results in low distortion
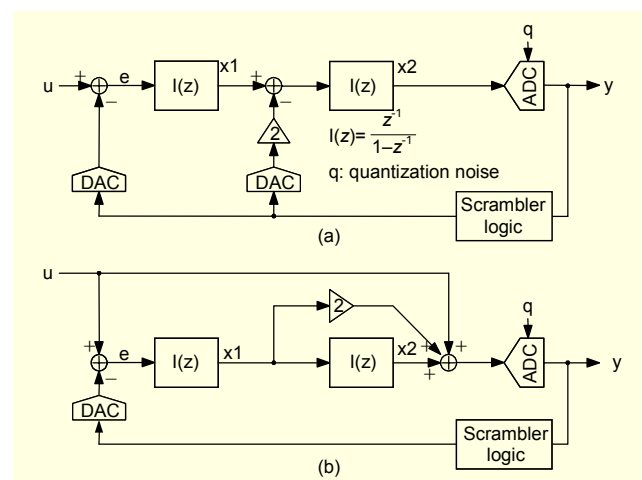

Fig. 1. Previous sigma-delta modulator architecture: (a) traditional and (b) full feed-forward architecture.

attenuation from $x1$ and $x2$ to y. Analog blocks for wideband applications require both high-speed and low-distortion properties, thus, posing a significant challenge.

Figure 1(b) shows a full feed-forward sigma-delta modulator architecture [2]. This architecture has a direct feed-forward path from the input of the sigma-delta modulator to the ADC input, which results in suppression of the input signal component in the loop-filter. Therefore, the integrators process only the quantization noise, thereby improving the distortion performance. However, this architecture requires a delay-free ADC and scrambler logic to cancel out the input signal component at the input subtractor before the first integrator. In a normal two-phase clocking scheme, the time required for the ADC and scrambler logic to operate reduces the time available for the integration phase of the first integrator. Therefore, this architecture is not appropriate for a high-speed modulator in the case of multi-bit architecture.

III. Proposed Architecture

The proposed architecture is shown in second order for simplicity in Fig. 2. It has a unity-gain signal transfer function (STF) and a second-order noise transfer function (NTF). The input of the DAC before the first integrator is the sum of delayed y and delayed differential y, from which the first integrator's input ($E(z)$) and output ($X1(z)$) can be derived:

$$E(z) = -Q(z) \cdot (1 - z^{-1})^2 + Y(z) \cdot (1 - z^{-1})^2 ,$$

$$X1(z) = Q(z) \cdot z^{-1} \cdot (1 - z^{-1}) + Y(z) \cdot z^{-1} \cdot (1 - z^{-1}) .$$

At the input of the second integrator and the multiplying DAC (MDAC), the differential y term in $x1$ is cancelled out by subtracting differential y. The first integrator processes the second-order highpass filtered version of the input signal, reducing the amplitude of the input signal component. The second integrator and MDAC process only the quantization noise. Therefore, the distortion requirement of the analog blocks can be relaxed.

The use of delay elements in the feedback path relaxes the allowable time for the ADC and scrambler logic to operate, thus making it possible for this architecture to operate with a multi-bit ADC/DAC at high speed.

In practice, cancellation of the input signal component in $x1$ at the second integrator and the MDAC will not be perfect. However, the distortion effects of these residual signal components will be negligible because the mismatch of the signal component in $x1$ and DAC_DIFF is small, and these error signals will appear at the output of the modulator in y, shaped by the first- and second-order highpass transfer functions.
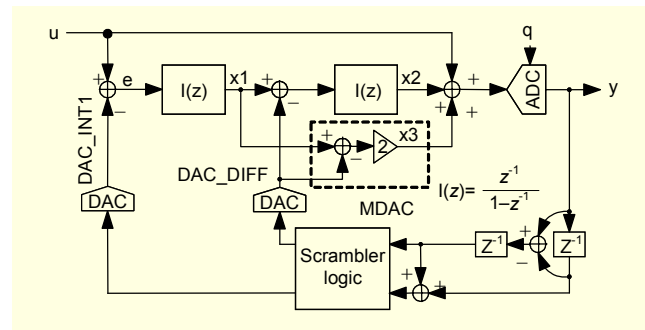
The MDAC requires an additional opamp, but the opamp

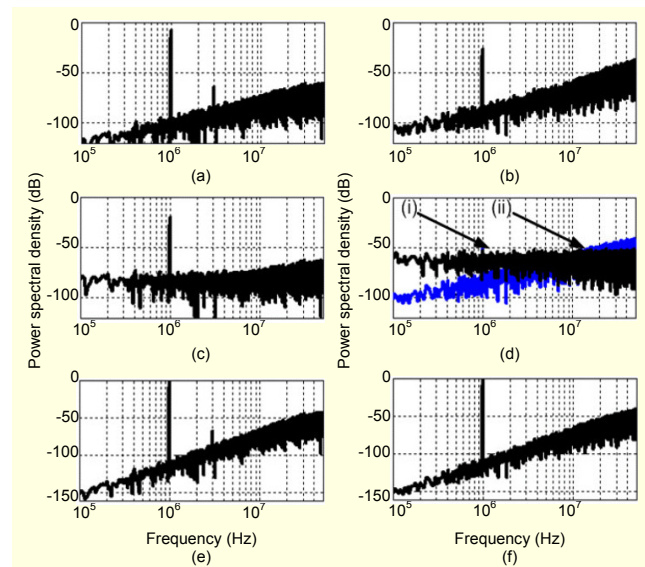Fig. 2. Proposed sigma-delta modulator.

Fig. 3. Comparison of simulation results: spectra in traditional architecture of (a) x1, (c) x2, and (e) y; and spectra in proposed architecture of (b) x1, (d)-(i) x2, (d)-(ii) x3, and (f) y.

performance will be relaxed. As previously described, the MDAC cancels the signal component in $x1$ and processes only the quantization noise. In addition, the MDAC output distortion will be shaped by the second-order highpass transfer function. These attributes alleviate the opamp performance requirement.

To verify the low-distortion performance, the traditional and proposed architectures, as shown in Figs. 1(a) and 2, are simulated with MATLAB. The nonlinearity incorporated into the integrators and the MDAC generated –40 dB harmonics in the case of a full scale signal. Both architectures used 4-bit ADC. The sampling frequency was 100 MHz and the sine-wave input signal, u, had an amplitude of 0.8 V (for a reference of 1 V) and a frequency of 1 MHz. Scaling factors were adjusted in each structure to ensure that the integrator output voltages were comparable.

Figure 3 shows the fast Fourier transforms (FFTs) of signals $x1$, $x2$, $x3$, and y for the two topologies. The traditional architecture shows that the output of the integrator includes the input signal

together with harmonics created due to the non-linear function. The modulator output y shows a third harmonic with an amplitude of –67 dBc. The proposed architecture shows that the output of the first integrator has a suppressed input signal component with –27 dBFS, and the second integrator and MDAC output contain only shaped quantization noise, which reduces the generation of harmonics. As a result, the modulator output y shows negligible harmonic distortion despite the poor distortion performance of the integrators and the MDAC.

IV. Implementation and Measurement

The proposed sigma-delta modulator architecture was expanded to a third-order 4-bit system, as shown in Fig. 4, and implemented using a switched capacitor circuit [3] in a 0.13-μm CMOS process with an active area of 1.0 mm × 1.1 mm, as shown in Fig. 5. The power consumption was 20 mW at 40M sample/sec from a 1.2 V supply. Figure 6 shows a 32768-point FFT spectrum of a 30 kHz –6 dB signal at a 40 MHz sampling frequency. Figure 7 shows the signal-to-noise ratio (SNR) and the signal-to-noise-plus-distortion ratio (SNDR) versus input amplitude for a 30 kHz input signal at a 1 MHz bandwidth with an OSR of 20. The amplitude of 0 dB corresponds to 1.2 Vpp differential. The spurious-free dynamic range (SFDR) shown in Fig. 6, the peak SNR, and the peak SNDR shown in Fig. 7 are 89.1 dB, 77.9 dB, and 74.6 dB, respectively.

The distortion performance of the proposed sigma-delta modulator is better than that of the published result which uses only the feedback path and a multi-bit ADC [4] despite its relatively low supply voltage. While [4] shows a third harmonic with an amplitude of –88 dBc for a –7 dBFS input signal, the measured results of the proposed architecture show a third harmonic with an amplitude of −89.1 dBc for a –6 dBFS input signal.
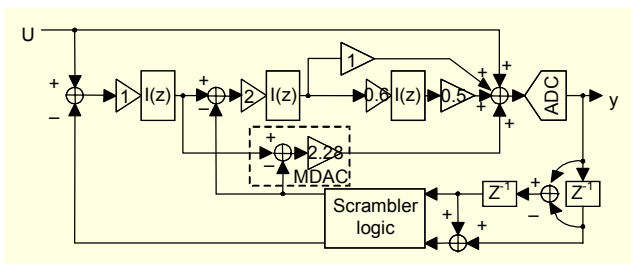

Fig. 4. Proposed third-order sigma-delta modulator.

V. Conclusion

We proposed a multi-bit sigma-delta modulator architecture which suppresses signal components in the loop filter and has delay elements in the feedback path to achieve low-distortion
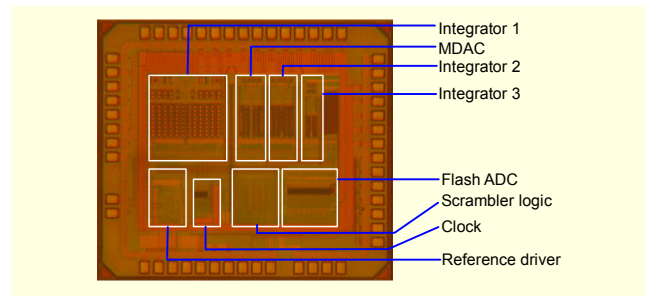

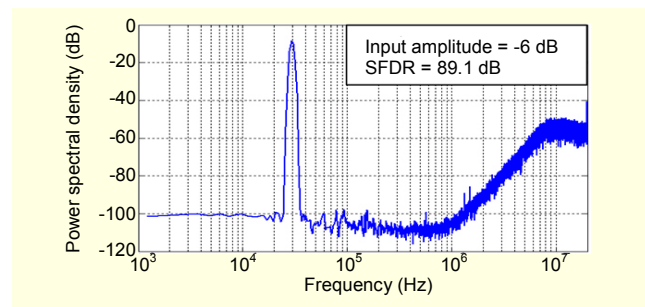Fig. 5. Die photo of the proposed sigma-delta modulator.

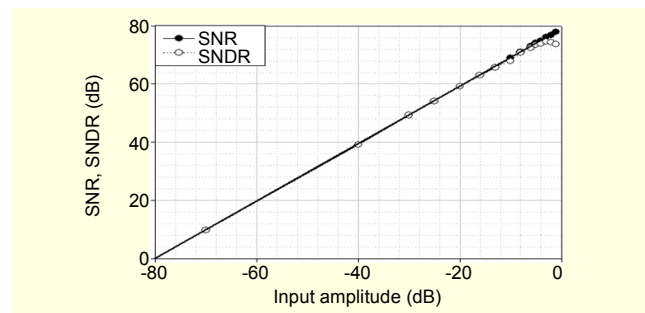Fig. 6. Measured output spectrum of -6 dB sinusoidal input.

Fig. 7. Measured SNR and SNDR versus input amplitude.

performance and relax the timing requirement of the ADC and the scrambler logic. The simulated and measured results showed that the proposed architecture has good distortion performance.

References

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