Integrated Rail-to-Rail Low-Voltage Low-Power Enhanced DC-Gain Fully Differential Operational Transconductance Amplifier

Giuseppe Ferri, Vincenzo Stornelli, and Angelo Celeste

In this paper, we present an integrated rail-to-rail fully differential operational transconductance amplifier (OTA) working at low-supply voltages (1.5 V) with reduced power consumption and showing high DC gain. An embedded adaptive biasing circuit makes it possible to obtain low stand-by power dissipation (lower than 0.17 mW in the rail-to-rail version), while the high DC gain (over 78 dB) is ensured by positive feedback. The circuit, fabricated in a standard CMOS integrated technology (AMS 0.35 μm), presents a 37 V/μs slew-rate for a capacitive load of 15 pF. Experimental results and high values of two quality factors, or figures of merit, show the validity of the proposed OTA, when compared with other OTA configurations.

Keywords: Fully differential amplifier, adaptive biasing, enhanced DC-gain, low-power, low-voltage.

I. Introduction

In analog integrated circuits, the recent trend toward miniaturized circuits has given a decisive boost towards low-voltage low-power design, widely used in portable system applications [1]-[4]. The most efficient way to reduce power consumption is to decrease both the supply voltage and the stand-by current. Reducing the supply voltage makes it difficult to implement efficient analog circuits, so novel circuit architectures have to be developed. The values of the current sources inside the amplifiers are the main cause of quiescent power dissipation. Adaptive biasing techniques boost the bias current of the input differential pair when large signals are applied, thus, increasing circuit dynamic characteristics without affecting stand-by dissipation [5]-[14].

In this paper, we present a novel rail-to-rail fully differential OTA, showing low-voltage low-power characteristics, where DC gain has been enhanced by a suitable technique which increases the output impedance of the operational transconductance amplifier (OTA) input stage through positive feedback [15], [16]. The proposed OTA has been developed using standard CMOS technology (AMS 0.35 μm) in NMOS, PMOS, and rail-to-rail versions and has shown very good characteristics in terms of two figures of merit (FOM), introduced in [12]. The paper is organized as follows. In section II, the OTA design technique is described in all its steps. Section III shows the amplifier structure and reports some considerations on stability. In section IV the main simulated and measured results are reported, in section V we present our conclusions.

Manuscript received May 31, 2007; revised July 16, 2007.

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II. Design Techniques

In the development of the proposed fully differential OTA (in NMOS, PMOS, and rail-to-rail versions, according to the type of input transistors), we have considered the following design steps: choice and design of the symmetrical OTA topology, application of the adaptive biasing technique, implementation of a fully differential adaptive biased OTA, and DC enhancement through negative load impedance compensation.

1. Symmetrical OTA

Figure 1 shows the basic topology of an NMOS symmetrical OTA [17]. Its voltage gain is given as

$$A_V = B\frac{g_{m1}}{g_{ds5}+g_{ds6}}, \tag{1}$$

where

$$B = \frac{(W/L)_8}{(W/L)_3} = \frac{(W/L)_5}{(W/L)_4}. \tag{2}$$

The GBW value is given by

$$GBW = B\frac{g_{m1}}{2\pi C_L}, \tag{3}$$

where C_L is the load capacitance, while the the slew rate (SR) is

$$SR = B\frac{I_B}{C_L}, \tag{4}$$

where I_B is the biasing current. In the weak inversion (WI) region, we have the maximum values of GBW and SR for a fixed current, as given in [8], as

$$SR = 4\pi\, nV_T \cdot GBW \cong 600\ \text{mV} \cdot GBW, \tag{5}$$

where n is the slope factor in WI, whose value is between 1 and 2, and V_T=KT/q is the thermal voltage, K is the Boltzmann constant, T is the absolute temperature in K degrees, and q is the electron charge. From (3) and (4), we can also deduce that

$$\frac{SR}{GBW} \propto \frac{I_B}{g_m}. \tag{6}$$

From (6), in order to enhance SR without changing GBW, the biasing current must be increased with consequent power consumption enhancement. In this sense, the use of the adaptive biasing technique helps to reduce stand-by power dissipation without degrading the circuit dynamic performances.

2. Adaptive Biasing

The adaptive biasing technique adds current at the input stage only if a differential input is applied. Many adaptive biasing circuits have been proposed [5]-[14]. One of the first and most diffused of them was presented in [8]. It is based on the current subtractor shown in Fig. 2. In this work, it has been applied to a symmetrical OTA (see Fig. 3). The current given by the subtractor is equal to

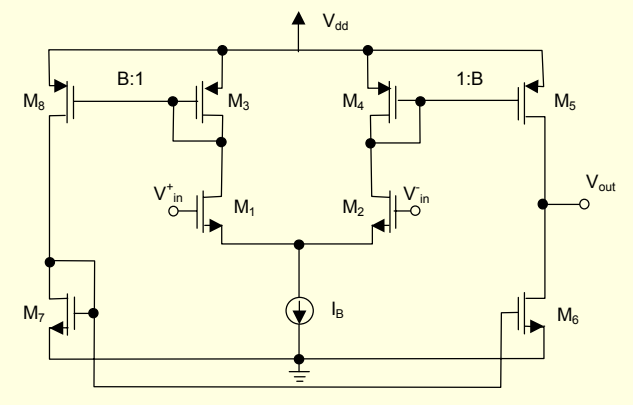


Fig. 1. NMOS symmetrical OTA.

$$I_B + A\left|I_2 - I_1\right|, \tag{7}$$

where, considering Fig. 2, the gain current A is given as

$$A = \frac{(W/L)_4}{(W/L)_{1,2,3}}. \tag{8}$$

The output current I_{out} and the bias current I_B are related according to the following equation (see Fig. 3):

$$I_{out} = B\left(I_1 - I_2\right) = \frac{BI_B(e^{V_{in}/nV_T}-1)}{(1+A)-(A-1)e^{V_{in}/nV_T}}, \tag{9}$$

which is valid in the weak inversion region, and, in the case of unitary gain B between output mirrors, for A typically in the range between 0 and 0.9, the output maximum current is I_B/(1–A). If A=0.9, the output current and, consequently, SR increase by a factor of 10.

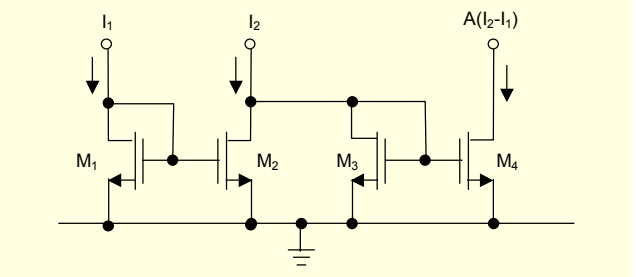


Fig. 2. Current subtractor.

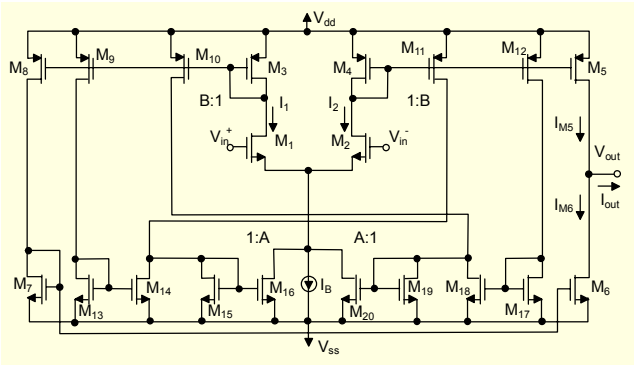


Fig. 3. Symmetrical OTA with adaptive biasing.

3. Fully Differential Solution

A fully differential version of the proposed OTA has been developed through the elimination of the diode connection in the M_7 transistor. A common mode feedback (CMFB) error amplifier has been added (R_1, R_2, M_9-M_{12}, I_{bias}, V_{ref}). Figure 4 shows the fully differential adaptive biased OTA with CMFB. In the circuit, I_B represents an adaptive biased current.

4. DC Gain Enhancement Techniques

To increase the DC gain, the negative conductance technique has been utilized [15]. It is illustrated in the circuit diagram given in Fig. 5. Placing a negative resistance R_n in parallel with the output resistance of the amplifier, the voltage gain is given as

$$A_V = \frac{V_0}{V_{in}} = \frac{-g_{m1}}{g_{ds1} + 1/R + 1/R_n}. \quad (10)$$

The voltage gain is ideally infinite if the following relation is satisfied:

$$\frac{1}{R_n} = -\left[\left(\frac{1}{R}\right) + g_{ds1}\right]. \quad (11)$$

This technique is better than others, such as cascode, because it is possible to obtain a DC gain enhancement also for

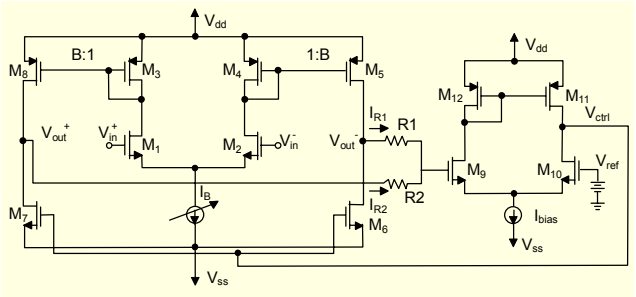


Fig. 4. Fully differential OTA with CMFB. I_B represents an adaptive biased current.

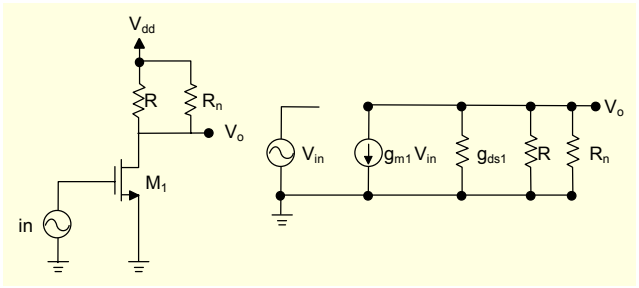


Fig. 5. Gain enhancement through NIC (left: considered architecture; right: small-signal equivalent circuit).

low-voltage applications. It can be applied to symmetrical OTA according to the topology shown in Fig. 6, where the gates of M_{23} and M_{24} are connected to the drains of M_3 and M_4. In this manner, at A and B nodes, a parallel resistance ($1/g_{m23,24}$) has been added. Transistors M_1, M_2 and M_{23}, M_{24} constitute a positive feedback loop, where the direct path is characterized by A_d voltage gain and the feedback loop, formed by M_{23}, M_1, and M_3 (M_{24}, M_2, and M_4), has a gain equal to β. The overall gain is given by

$$A = \frac{A_d}{1 - A_d\beta} = \frac{A_d}{1 - G_{loop}}, \quad (12)$$

where G_{loop} is the loop gain equal to $A_d\beta$. The gain A_d is given as

$$A_d = \frac{g_{m1}}{g_{m3} + g_{ds23} + g_{ds3} + g_{ds1}}. \quad (13)$$

To calculate the loop gain G_{loop}, the input voltage has to be grounded, and a signal has to be forced in an arbitrary node inside the same loop. The G_{loop} is the ratio between the signal processed by the loop and the forced signal. Figure 7 shows the feedback branch structure. From the small-signal analysis we can write

$$G_{loop} = \frac{V_{out}}{V_{in}} = \frac{g_{m23}}{g_{m3} + g_{ds23} + g_{ds3} + g_{ds1}}. \quad (14)$$

Stability is ensured if G_{loop} is lower than 1. From (14), this is easily obtained if g_{m3} is close to g_{m23}. In this case, since the overall gain A can be expressed as

$$A = \frac{g_{m1}}{g_{m3} - g_{m23} + g_{ds23} + g_{ds3} + g_{ds1}} \approx \frac{g_{m1}}{g_{m3} - g_{m23}}, \quad (15)$$

a condition on g_{m3} and g_{m23} values can be deduced. In particular, to avoid gain A becoming infinite or changing its sign, the value of g_{m3} has been set to be lower than 94% of the g_{m23} value.

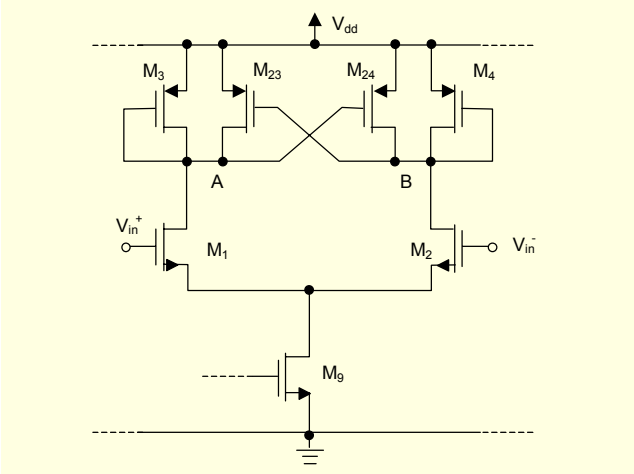


Fig. 6. Negative compensated OTA.

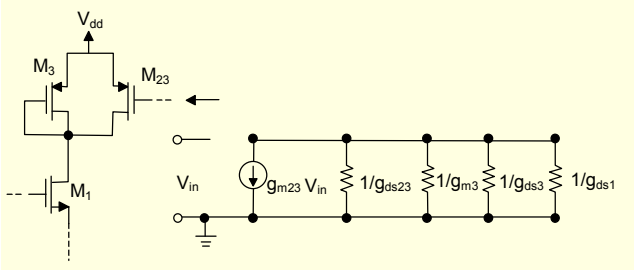


Fig. 7. Feedback branch structure (left: considered architecture; right: small-signal equivalent circuit).

III. The Proposed Amplifier

In this section, we report the complete architecture of the proposed amplifier. In particular, we have implemented the NMOS, PMOS, and rail-to-rail versions, according to the type of the input transistors.

1. NMOS OTA Architecture

Figure 8 shows the topology of the designed NMOS adaptive-biased DC-enhanced fully differential symmetrical OTA. The transistor of the original symmetrical OTA comprises M_1 to M_8, while adaptive biasing is formed by M_{13} to M_{16} and $_{M17}$ to M_{20} current subtractors and by M_3 to M_9, M_3 to M_{10}, M_4 to M_{11}, and M_4 to M_{12} current mirrors. Transistors M_{23} and M_{24} allow the performance of DC enhancement, while R_1, R_2, M_{21}, M_{22}, M_{25}, M_{26}, I_{p1}, and V_{ref} form the CMFB circuit.

2. NMOS OTA Stability

The designed amplifier is a two-stage OTA. In this case, we have not applied a classical Miller compensation because the right half plane zero has not been nullified; rather, it has been designed at a frequency close to that related to the non-dominant pole to benefit from the lead effect. The choice of C_M=3 pF and R_M= 40 kΩ allows us to have a zero with a negative real part, and this partially compensates the non-dominant pole effects on the module and phase response. The dominant pole is at frequency

$$f_{p1} = \frac{1}{2\pi g_{m5} R_i R_u C_m}, \tag{16}$$

where R_i is the output resistance of the differential stage and R_u is that at the amplifier output:

$$R_i = \frac{1}{g_{m3} - g_{m23} + g_{ds3} + g_{ds23} + g_{ds1}}, \tag{17}$$

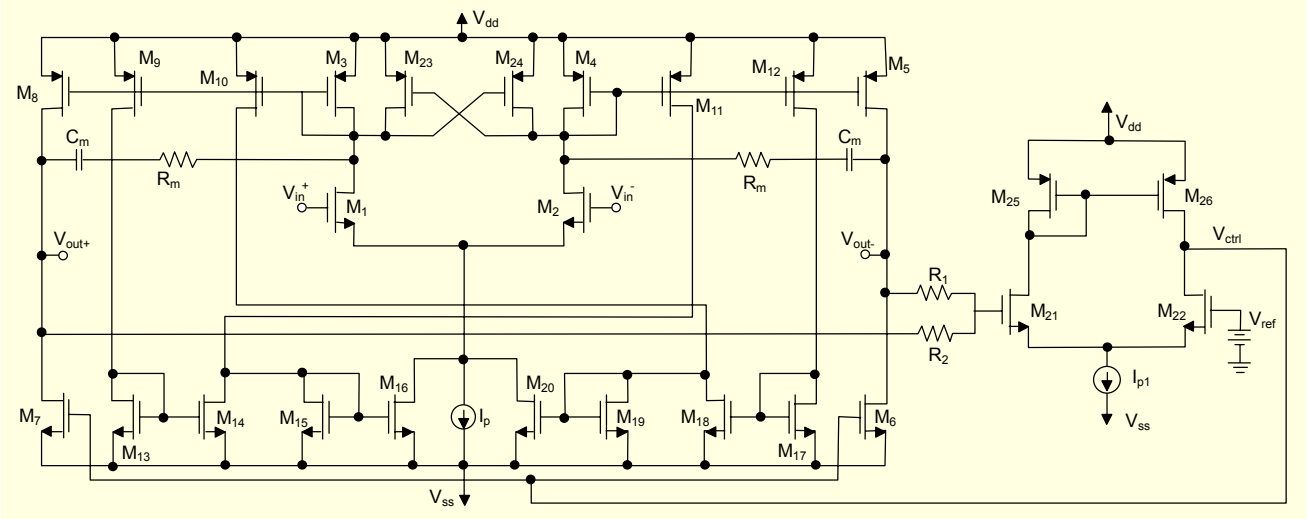


Fig. 8. Fully differential amplifier with adaptive biasing and enhanced DC-gain topology (NMOS version).

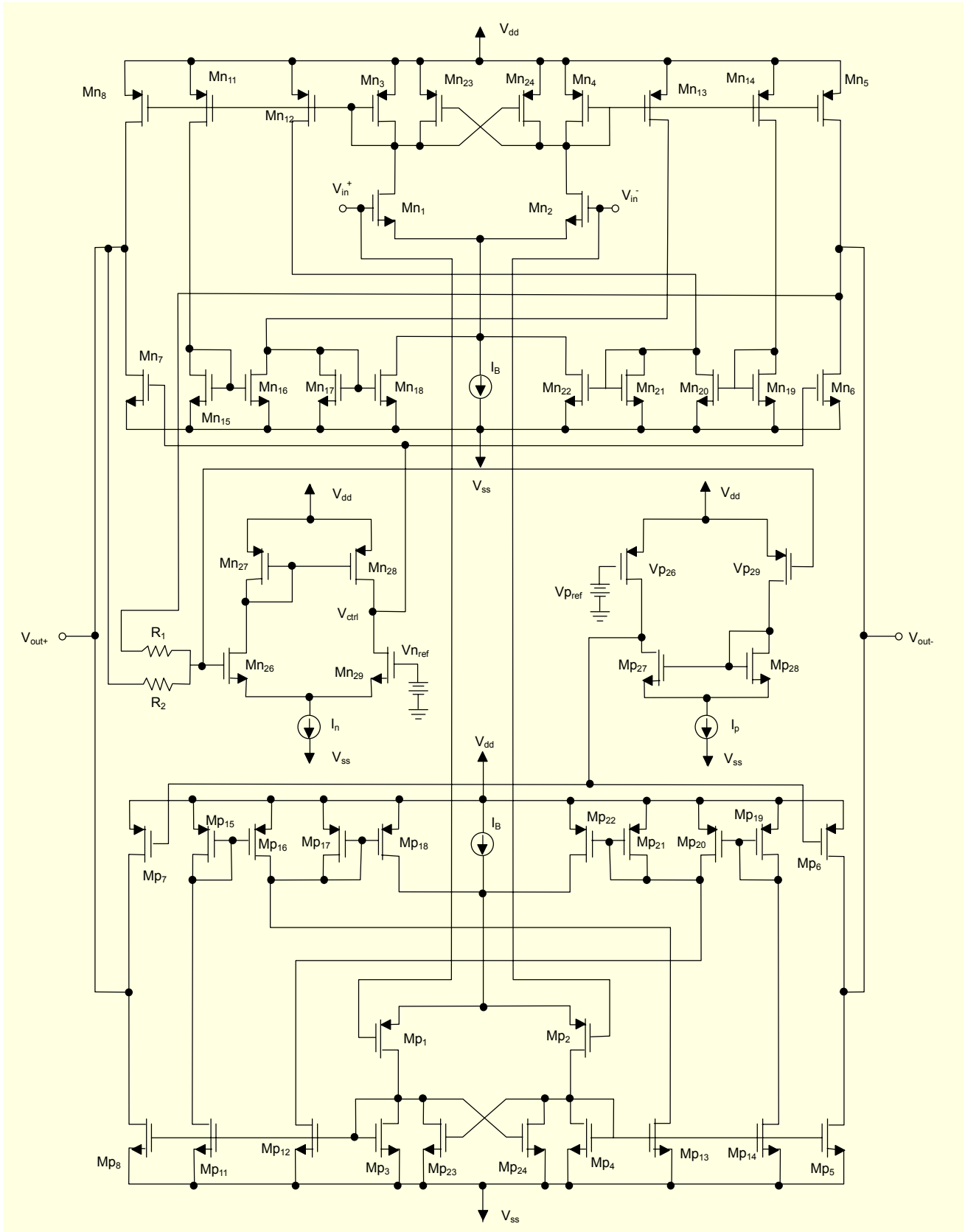


Fig. 9. Rail-to-rail configuration of the designed amplifier.

$$R_u = \frac{1}{g_{ds5} + g_{ds6} + 1/R}. \quad (18)$$

First, the non-dominant pole is given by

$$f_{p2} = \frac{g_{m5}C_m}{2\pi\left[C_iC_u + (C_i + C_u)C_m\right]} \approx \frac{g_{m5}}{2\pi C_u}, \quad (19)$$

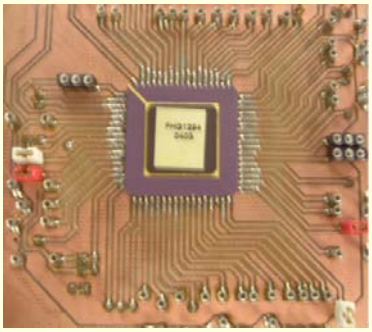
where C_i and C_u are the first- and second-stage output capacitances. Zero occurs at the following frequency:

$$f_z = \frac{g_{m5}}{2\pi C_m\left(R_m - \frac{1}{g_{m5}}\right)}. \quad (20)$$

Table 1 shows the operative values of output conductances and transconductances of the main transistors, from which R_i=3.03 MΩ and R_u=188 kΩ. Consequently, we have f_{p1} =940 Hz and f_{p2}=1.05 MHz. Choosing R_m=40 kΩ, we obtain f_z=1.77 MHz. The phase margin is 74°, but stability (PM>45°) is always ensured by also considering temperature and technological parameter variations, as indicated by Monte Carlo analysis and confirmed by experimental results.

Table 1. Main transistor transconductances and output conductances (simulated results).

Transistor	Transconductances (S)	Output conductances (S)
M_1	1.49×10^{-4}	1.89×10^{-6}
M_3	3.9×10^{-5}	1.02×10^{-6}
M_{23}	4.27×10^{-5}	1.12×10^{-6}
M_5	9.9×10^{-5}	2.6×10^{-6}
M_6	1.52×10^{-4}	1.72×10^{-6}



(a)

(b)

Fig. 10. a) PCB used for the measurements and b) micrograph of the chip area occupied by the amplifier.

3. Rail-to-Rail Configuration

We have designed the PMOS version of the amplifier (through the implementation of the complementary circuit of the NMOS OTA) and the rail-to-rail configuration placing the NMOS and PMOS solutions in parallel (see Fig. 9). This latter circuit has complete common-mode control, a higher SR, and a better output dynamic range, even if stand-by power dissipation is increased. The OTA transconductance and GBW values, influenced by the adaptive biasing current, are about 50 mS and 820 Hz, respectively.

IV. Experimental Results

The three designed OTA topologies were first simulated using standard CMOS technology (AMS 0.35 μm). The rail-

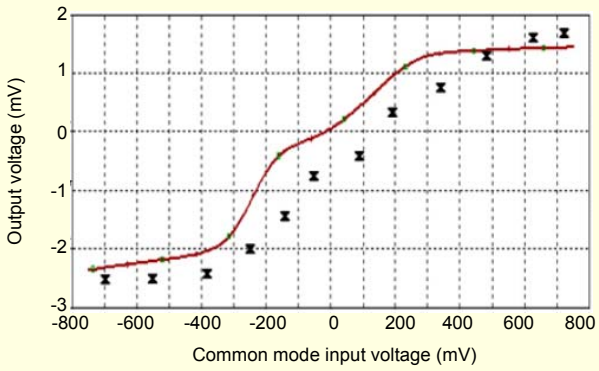


Fig. 11. Simulated (continuous line) vs. measured differential output response to a common mode input for the rail-to-rail solution.

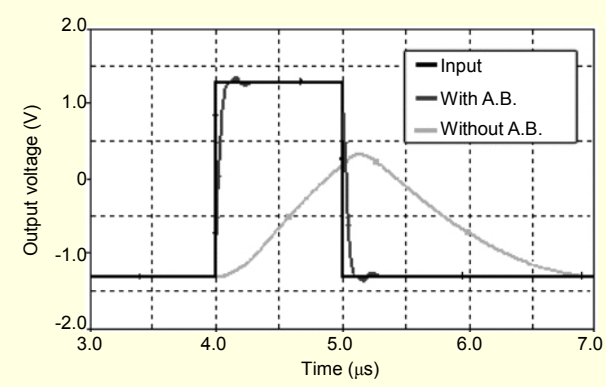


Fig. 12. SR behaviour with and without the adaptive biasing for the rail-to-rail solution.

to-rail version was fabricated using the same technology. Figure 10 shows the PCB used for measurements and the amplifier chip microphotograph (silicon area of the amplifier: about 0.15 mm^2). The circuits were supplied at ±0.75 V while an external load capacitance was chosen at 15 pF even if the circuit was able to drive capacitive loads up to 100 pF. In Fig. 11, the measured output response when a common mode signal is applied is reported and compared with the simulation results. Figure 12 reports the simulated transient response to a square wave input, showing the SR performance with and without the adaptive biasing circuitry for the rail-to-rail version. The adaptive biasing operation allows an increase in the SR value by a factor of about 30. In Fig. 13, the same measured response (using a Yokogawa DL 1520 8-bit, 200 MS/s, 150 MHz oscilloscope) is shown, considering the presence of adaptive biasing. In Fig. 14, the OTA response, in its integrator configuration (Fig. 14(a)), to an 8 kHz frequency input square-wave signal is shown (Fig. 14(b)). Both results are in excellent agreement with post layout simulations. Table 2 shows the main simulated and measured results for the rail-to-rail version only. In Table 3, two significant quality factors, named FOM and introduced in [12], for both small (FOM_S) and large (FOM_L) signals, are reported. These two parameters are defined as follows:

$$FOM_L = \frac{SR \cdot C_{LOAD}}{\text{Power}} \quad [(\text{V}/\mu\text{s} \cdot \text{pF})/\text{mW}] \qquad (21)$$

$$FOM_S = \frac{GBW \cdot C_{LOAD}}{\text{Power}} \quad [(\text{MHz} \cdot \text{pF})/\text{mW}] \qquad (22)$$

All the obtained results are compared with other topologies presented in the literature, both simulated and measured, confirming the validity of the proposed solution.

V. Conclusion

We designed an adaptive-biased fully differential low-voltage low-power OTA topology with enhanced DC-gain. By experiment and simulation, the proposed circuit, fabricated in its rail-to-rail version, was confirmed to show good performance results. Therefore, it can be utilized, for example, in biomedical and sensor interfaces, where power dissipation is a fundamental requirement to maintain the life of batteries. Moreover, due to high SR and low settling time values, this solution is also suitable for those applications that require high speed and precision.

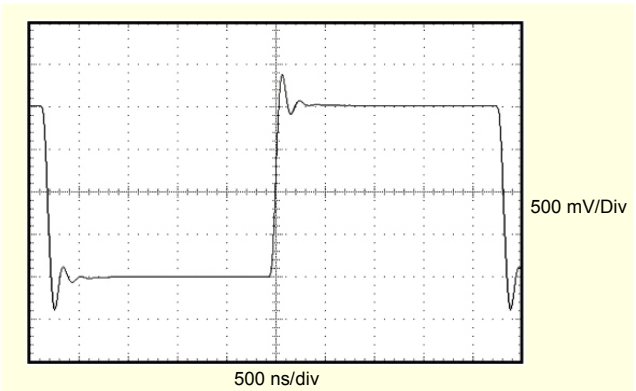


Fig. 13. Measured step response for the rail-to-rail solution.

Table 2. Main simulated and experimental results, for single-ended (s) and differential (d) outputs.

Parameter	NMOS simulated	PMOS simulated	Rail-to-rail simulated	Rail-to-rail measured
Static power dissipation	85 µW	84 µW	166 µW	169 µW
DC-gain	79 dB	82 dB	81 dB	78 dB
GBW	4.7 MHz	6.8 MHz	9.2 MHz	8.9 MHz
Input offset	65 µV	69 µV	71 µV	< 200 µV
Phase-margin	74°	81°	89°	-
SR	17 (V/µs)	25 (V/µs)	40 (V/µs)	37 (V/µs)
CMRR	142 dB	136 dB	132 dB	126 dB
PSRR+	107 dB	114 dB	147 dB	-
PSRR–	114 dB	109 dB	150 dB	-
Settling time (0.25%)	390 ns	410 ns	310 ns	390 ns

Table 3. Comparison of FOM parameters.

	FOM_L in (21)	FOM_S in (22)
This work, NMOS (simulated)	829	3,000
This work, PMOS (simulated)	1,214	4,464
This work, rail-to-rail (simulated)	831	3,614
This work, rail-to-rail (measured)	789	3,284
[5]	800	2,400
[6]	3,636	263
[7]	50	135
[12]	271	500
[13]	652	4,000
[18]	272	400
[19]	1,350	447

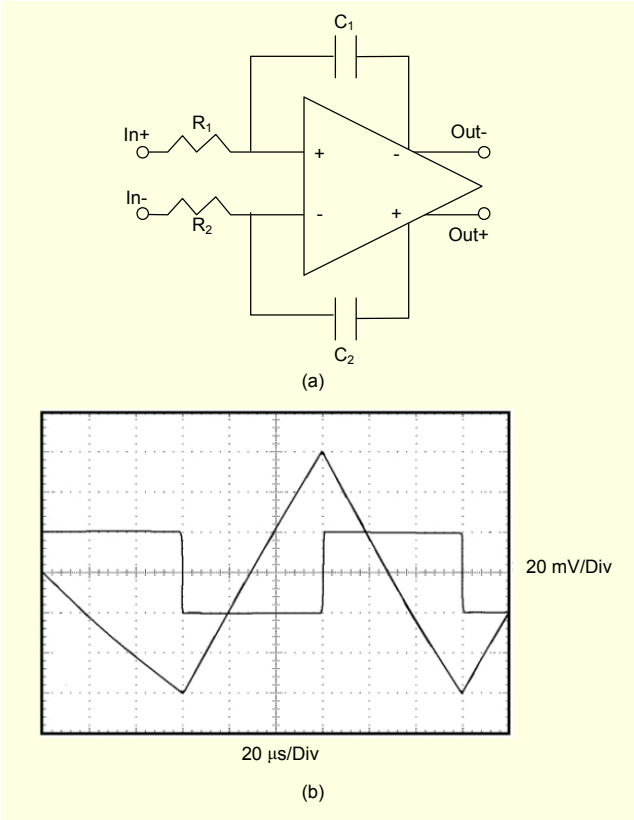


Fig. 14. (a) Differential integrator configuration and (b) measured integrator response for the rail-to-rail solution (C_1=C_2=100 pF; R_1=R_2=100 kΩ).

References

[1] W. Serdijn, A.C. van der Woerd, and J.C. Kuenen, *Low Voltage Low Power Analog Integrated Circuits*, Kluwer Ac. Publ., Boston, 1995.

[2] M.A.T. Sanduleanu and E.A.J.R. van Tuijl, *Power Trade-Offs And Low-Power In Analog CMOS ICs*, Kluwer Ac. Publ., Boston, 2002.

[3] G. Ferri and N. Guerrini, *Low Voltage Low Power CMOS Current Conveyors*, Kluwer Ac. Publ., Boston, 2003.

[4] R. Hogervorst, *Design CMOS Operational Amplifier Cells*, Delft Univ. Publ., Delft, 1996.

[5] A. J. López-Martín, S. Baswa, and J. Ramirez-Angulo, "Low-Voltage Power-Efficient Adaptive Biasing for CMOS Amplifiers and Buffers," *Electronics Letters*, vol. 40, no. 4, Feb. 2004, pp. 217-219.

[6] J. A. Galan, A. Lòpez-Martin, R. Carvajal, J. Ramirez-Angulo, and C. Rubia-Marcos, "Super Class AB OTAs with Adaptive Biasing and Dynamic Output Current Scaling," *IEEE Trans. on Circuits and Systems-I,* vol. 54, Mar. 2007, pp. 449-457.

[7] R. Klinke, B.J. Hosticka, and H.J. Pfleiderer, "A Very High Slew Rate CMOS Operational Amplifier," *IEEE J. of Solid State Circuits,* vol. 24, June 1989, pp. 744-746.

[8] M.G. Degrauwe, J. Rijmenants, E.A. Vittoz, and H. DeMan, "Adaptive Biasing CMOS Amplifiers," *IEEE J. of Solid State Circuits,* vol. 17, June 1982, pp. 522-528.

[9] H. Parzhuber and W. Steinhagen, "An Adaptive Biasing One-Stage CMOS Operational Amplifier for Driving High Capacitive Loads," *IEEE J. of Solid State Circuits,* vol. 1, May 1991, pp. 1457-1460.

[10] G. Ferri and G.C. Cardarilli, "A 1.6 V 80 μW Rail-to-Rail Constant-Gm Bipolar Adaptive Biased Op-Amp Input Stage," *Proc. ISCAS*, vol. 1, May 1998, pp. 452-455.

[11] G. Giustolisi, G. Palmisano, G. Palumbo, and T. Segreto, "1.2-V CMOS Op-Amp with a Dynamically Biased Input Stage," *IEEE J. of Solid State Circuits,* vo1. 35, no. 4, Apr. 2000, pp. 632-636.

[12] C. Lin and M. Ismail, "A Low-Voltage CMOS Rail-to-Rail Class AB Input-Output Op-Amp with Slew Rate and Settling Enhancement," *Proc. ISCAS*, vol. 1, May 1998, pp. 448-450.

[13] G. Cardarilli, G. Ferri, and F. Bordoni, "A Low-Voltage Low-Power Rail-To-Rail Constant-Gm Adaptive Biased CMOS Operational Amplifier," *Proc. ICM Conference,* vol. 1, Dec. 1998, pp. 13-16.

[14] S. Sengupta, "Adaptively Biased Linear Transconductor," *IEEE Trans. on Circuits and Systems-I,* vol. 52, Nov. 2005, pp. 2369-2375.

[15] J. Yan and R.L. Geiger, "A Negative Conductance Voltage Gain Enhancement Technique for Low Voltage High Speed CMOS Op Amp Design," *Proc. of 2000 Midwest Symposium on Circuits and Systems*, vol. 1, Aug. 2000, pp. 502-505.

[16] J. Yan and R.L. Geiger, "A High Gain CMOS Operational Amplifier With Negative Conductance Gain Enhancement," *Proc. Custom Integrated Circuits Conference*, vol. 1, May 2002, pp. 337-340.

[17] R. Laker and W.M. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw Hill Publ., NY, 1994.

[18] H.T. Ng, R.M. Ziazadeh, and D.J. Allstot, "A Multistage Amplifier Technique with Embedded Frequency Compensation," *IEEE J. of Solid-State Circuits,* vol. 34, Mar. 1999, pp. 339-347.

[19] H. Lee and P.K.T. Mok, "Active-Feedback Frequency Compensation Technique for Low-Power Multistage Amplifiers," *IEEE J. of Solid-State Circuits,* vol. 38, Mar. 2003, pp. 511-520.

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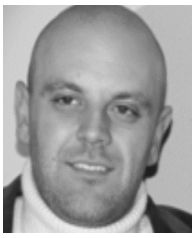

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