Improved Delay-Locked Loop in a UWB Impulse Radio Time-Hopping Spread-Spectrum System

Weihua Zhang, Hanbing Shen, and Kyung Sup Kwak

As ultra-wideband impulse radio (UWB-IR) uses short-duration impulse signals of nanoseconds, even a small number of timing errors can cause a detrimental effect on system performance. A delay-locked loop (DLL) is proposed to synchronize and reduce timing errors. The design of the DLL is vital for UWB systems. In this paper, an improved DLL is introduced to a UWB-IR time-hopping spread-spectrum system. Instead of using only two central correlator branches as in a conventional DLL, the proposed system uses two additional correlator branches with different delay parameters and different weight parameters. The performance of the proposed schemes with the optimal parameters is compared with that of traditional schemes through simulation: the proposed four-branch DLLs achieves less tracking jitter or a longer mean time to lose lock (MTLL) than the conventional two-branch DLLs if proper parameters are chosen.

Keywords: Ultra-wide band (UWB), delay-locked loop (DLL), tracking jitter, mean time to lose lock (MTLL).

I. Introduction

Recently, communication systems that employ ultra-wideband (UWB) technology have drawn considerable attention from academic institutions and commercial endeavors working on their development. UWB technology was originally adopted in military applications and short-range radar for locating and tracking items. Since the clearance of UWB for commercial usage, it has been considered as the physical layer for a new indoor wireless personal area network (WPAN) standard [1]. This radio technology is based on the radiation of waveforms formed by a sequence of very short (in or below the nanosecond range) baseband pulses, thereby spreading the energy of the radio signal from near zero to several gigahertz [2].

According to FCC reports, the bandwidth of UWB is relatively large and offers the ability to transfer data at rates as high as several hundred megabits per second. Short pulse waves coupled with a wide bandwidth also enable the accurate measurement of the relative distance between UWB terminals. Due to the extremely short time duration of pulse waveforms, a timing shift from the correct time to the achieved time by the delay-locked loop (DLL) degrades system performance. For this reason, the design of the DLL is vital in UWB systems.

A number of papers have investigated the performance of DLLs in UWB impulse radio (IR) systems, and several new DLL schemes have been proposed to achieve better performance. For example, it was found that a well-known DLL [3], [4] can be used in a UWB direct-sequence spread-spectrum (DS-SS) system to reduce timing jitter. Additionally, a novel DLL has been developed [5] for a time-hopping spread-spectrum (TH-SS) system and its performance has been evaluated [6]. An adaptive DLL algorithm for UWB-IR

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transmissions in multipath scenarios was proposed in [7]. Finally, the performance of a conventional DLL in a UWB distance measurement system was evaluated in [8]. System performance can be improved further by other DLL schemes.

In this paper, an improved DLL design method is proposed to achieve better performance in UWB-IR TH-SS systems. New correlator branch arrays with different delay parameters and different weight parameters are applied. Analysis and simulation results certify that, with carefully chosen parameters, the proposed DLLs are superior to conventional DLLs.

II. UWB-IR TH-SS System Model

1. TH-SS Format Signal Model

A UWB-IR TH-SS system with pulse position modulation (PPM) uses nanosecond pulses of the baseband to modulate the information bits.

A typical output signal $s(t)$, which is a random process describing the transmitted signal, is given by

$$s(t)=\sum_{i=-\infty}^{\infty}\sum_{j=0}^{N_s-1} w_{tr}\left(t-iT_b-jT_f-c_jT_c-\delta d_i\right), \quad (1)$$

where $w_{tr}(t)$ is the transmitted monocycle waveform; t is the transmitter clock time; T_f is the frame length which equals the nominal interval between two pulses; N_s is the number of frames per data symbol and T_b is the symbol duration (thus, $T_b = N_sT_f$); T_c is the chip duration and N_f is the number of chips per frame (thus, $T_f = N_f T_c$); c_j is a pseudorandom code assigned to a certain user, determining the position of the j-th pulse with $0 \le c_j \le N_f - 1$; $d_i \in \{0, 1\}$ is the i-th data; and δ is the modulation index representing the delay time in transmission of data d_i.

The corresponding received signal $r(t)$ is given by

$$r(t)=\sum_{i=-\infty}^{\infty}\sum_{j=0}^{N_s-1} w_{rec}\left(t-iT_b-jT_f-c_jT_c-\delta d_i-\tau_s\right)+n(t), \quad (2)$$

where $w_{rec}(t)$ represents the received monocycle waveform corresponding to the transmitted monocycle waveform $w_{tr}(t)$; τ_s is the delay time brought out from the transmission distance between the transmitter and receiver; and $n(t)$ is additive noise (AWGN). As the DLL makes its focus on the receiver side, we define $w_{rec}(t)$ as given in [9] as

$$w_{rec}(t)=\left(1-4\pi\left(\frac{t}{t_m}\right)^2\right)e^{-2\pi\left(\frac{t}{t_m}\right)^2}, \quad (3)$$

where t_m is the pulse width parameter. In the analysis and simulation of this study, the useful parameter T_p is employed as a reference time duration. It is the time duration of the main lobe of the received pulse waveform $w_{rec}(t)$. The waveform

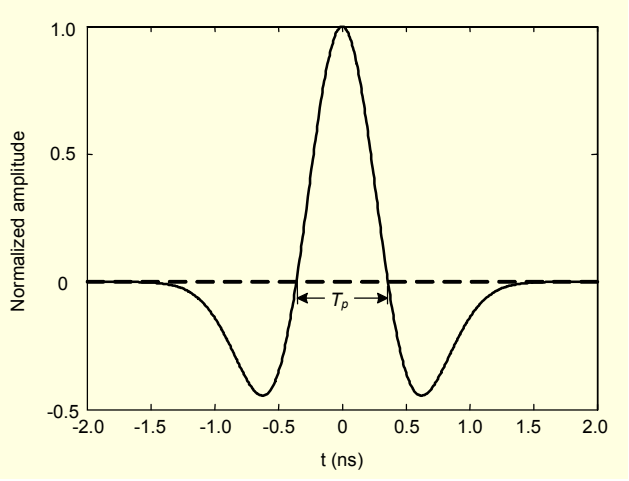

Fig. 1. Pulse waveform of $w_{rec}(t)$.

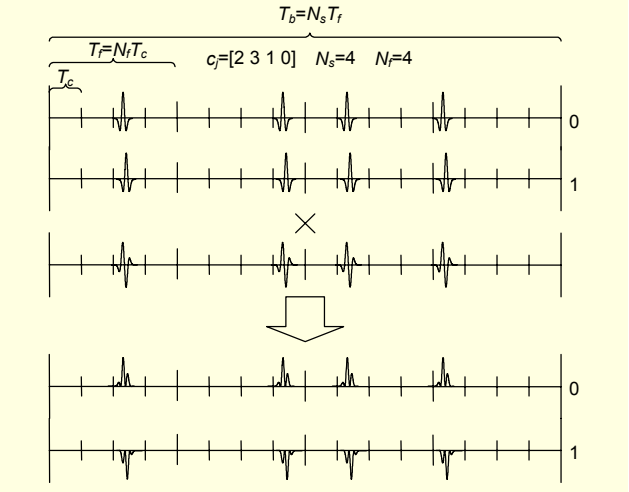

Fig. 2. Demodulation of a conventional TH PPM UWB.

$w_{rec}(t)$ and the parameter T_p are illustrated in Fig. 1.

A template is required in the receiver. The template waveform $v(t)$ at the receiver is given by

$$v(t)=w_{rec}(t)-w_{rec}(t-\delta). \quad (4)$$

Demodulation is achieved by correlating the received signals to the template waveform. Figure 2 is an example of a conventional UWB TH-SS system in which the correlation values are changed between +1 and −1 by 0 and 1 data. This scheme works well in a TH-SS system for modulation and demodulation. In terms of the DLL, however, this unbalanced data (all 1s or all 0s) creates difficulties with the synchronization. The discriminator output of one bit is an unbalanced result. It is necessary to collect an adequate number of randomized bits that include nearly the same number of 1 bits and 0 bits to achieve correct discriminator output. However, a longer discrimination duration leads to a longer

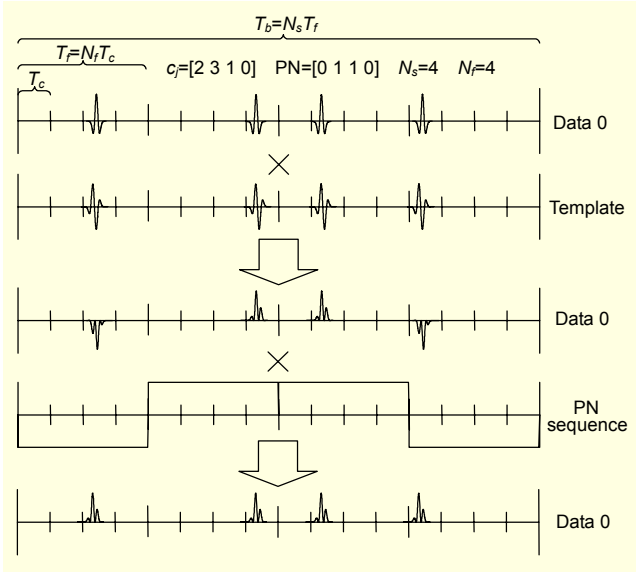

Fig. 3. Demodulation of TH PPM UWB with the PN sequence.

tracking duration, and increases the tracking delay. If the discrimination duration is not sufficiently long, a delay discrimination error will occur.

A balanced pseudorandom noise (PN) sequence (including half 1s and half 0s) is introduced to the TH PPM UWB to resolve this problem [5]. An example of this system with the PN sequence is given in Fig. 3. The transmitter output $s(t)$ is given by

$$s(t)=\sum_{i=-\infty}^{\infty}\sum_{j=0}^{N_s-1} w_{tr}\left(t-iT_b-jT_f-c_jT_c-\delta\left(PN_j\oplus d_i\right)\right), \quad (5)$$

where $PN_j \in \{0, 1\}$ represents the j-th weight coefficient of the PN sequence and $\oplus$ is the modulo 2 addition function. The corresponding received signal is represented as

$$r(t)=\sum_{i=-\infty}^{\infty}\sum_{j=0}^{N_s-1} w_{rec}\left(t-iT_b-jT_f-c_jT_c-\delta\left(PN_j\oplus d_i\right)-\tau_s\right)+n(t). \quad (6)$$

The PN_j is represented as $\{0, 1\}$ in the modulation; however, it will be converted to $\{-1, +1\}$ when it is multiplied with correlated signals in the demodulation. It must be emphasized that the numbers of 0s and 1s should be equal in the design of the PN sequence

With this balanced PN sequence, one bit signal is expressed as the equal number (N_s/2) of 0s and 1s. A correct discriminator output can then be achieved after only one bit duration. This method can reduce the discrimination duration and increase the discrimination accuracy.

2. DLL in TH PPM UWB

A conventional DLL in a UWB system is performed as in Fig. 4, in which the pulse generator gives out local pulses based on the clocks from a clock generator. The received signal $r(t)$ is multiplied by the αT_p-early and αT_p-late replicas of the local pulse, and the outputs of the integrators are inverted and added to produce discriminator characteristics. The discriminator characteristics are sent to a loop filter and to a voltage controlled delay line (VCDL), where a new clock time is evaluated. The difference between the evaluated clock time $\hat{\tau}_s$ and the real delay time τ_s from the transmitter to the receiver is the delay error τ_e which is given as

$$\tau_e = \tau_s - \hat{\tau}_s. \quad (7)$$

A well-designed DLL should make the absolute value of the delay error τ_e as small as possible.

Figure 5 shows the DLL adopting the balanced PN sequence for the TH-SS UWB, which has two correlation branches. Here, α is a variable that can adjust the quantity of time shift of the branches. As the numbers of 0s and 1s are equal in the PN sequence, the correlator outputs are given by

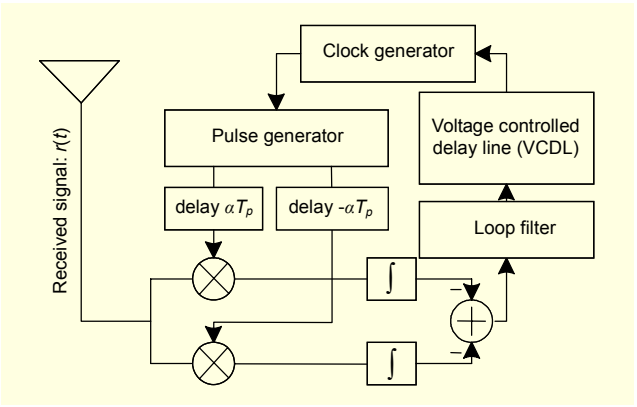

Fig. 4. Block diagram of a conventional DLL in UWB.

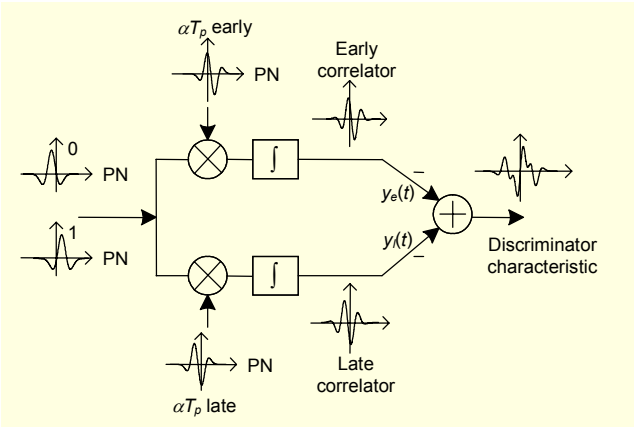

Fig. 5. Discriminator characteristics for a DLL with two branches.

$$y_e(\tau_e)=\sum_{j=0}^{N_s-1}\int_{\hat{\tau}_s+iT_b+jT_f+c_jT_c}^{\hat{\tau}_s+iT_b+(j+1)T_f+c_jT_c} w_{rec}\left(t-iT_b-jT_f-c_jT_c-\delta(PN_j\oplus d)-\tau_s\right)$$
$$\cdot v\left(t-iT_b-jT_f-c_jT_c-\hat{\tau}_s+\alpha T_p\right)dt$$
$$=\frac{N_s}{2}\left[R\left(\tau_e+\delta+\alpha T_p\right)-R\left(\tau_e-\delta+\alpha T_p\right)\right],$$
$$y_l(\tau_e)=\frac{N_s}{2}\left[R\left(\tau_e+\delta-\alpha T_p\right)-R\left(\tau_e-\delta-\alpha T_p\right)\right], \quad (8)$$

where $R(t)$ is the autocorrelation function of $w_{rec}(t)$. If $w_{rec}(t)$ is the waveform expressed in (3), the normalized $R(t)$ can be given by

$$R(t)=\left(1-4\pi\frac{t^2}{t_m^2}+\frac{4}{3}\pi^2\frac{t^4}{t_m^4}\right)\exp\left(-\frac{\pi t^2}{t_m^2}\right). \quad (9)$$

The discriminator characteristic is the sum of $-y_e(\tau_e)$ and $-y_l(\tau_e)$, which is given by

$$DD(\tau_e)=\frac{N_s}{2}\left[R\left(\tau_e-\delta-\alpha T_p\right)-R\left(\tau_e+\delta-\alpha T_p\right)\right.$$
$$\left.+R\left(\tau_e-\delta+\alpha T_p\right)-R\left(\tau_e+\delta+\alpha T_p\right)\right]. \quad (10)$$

3. Evaluation Figures of Merit

Two figures of merit are introduced in this subsection: tracking jitter variance and mean time to lose lock (MTLL).

After establishing the behavior of the DLL in UWB TH-SS PPM systems, the equivalent timing model of a DLL becomes known and is shown in Fig. 6, where $D(z)$ is Z-transform of the digital loop filter and $I(z)$ is the Z-transform of the VCDL. The result as given in [10] is

$$\frac{Z(\tau_e)}{Z(n)}=\frac{-D(z)I(z)}{1+DD(\tau_e)D(z)I(z)}. \quad (11)$$

For a high E_b/N_0, the tracking error τ_e fluctuates about the stable equilibrium point at $\tau_e=0$. The discriminator characteristic performs as a linear function in this duration as

$$DD(\tau_e)=\tau_e DD'(0), \quad (12)$$

where $DD'(t)=dDD(t)/dt$ is the gradient of the discriminator characteristic. After closing the loop, the tracking jitter variance is proportional to

$$\sigma_{\tau_e}^2=E\left\{\tau_e^2\right\}\propto\frac{1}{\left[\tau_e DD'(0)\right]^2}. \quad (13)$$

This implies that the tracking jitter variance is inversely proportional to the square of the gradient of discriminator characteristic $DD(\tau_e)$ at $\tau_e=0$.

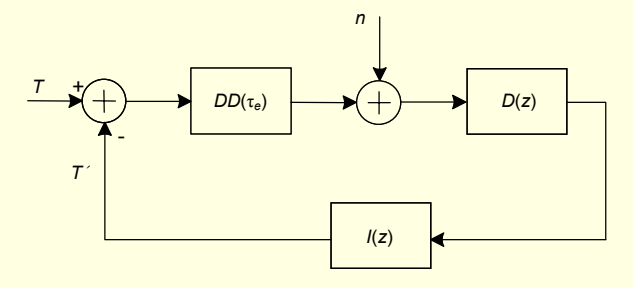

Fig. 6. Equivalent timing model for a DLL in UWB systems.

In addition, MTLL is an important figure of merit in the evaluation of a DLL. A DLL should be suitably robust to maintain a lock when there is a high level of interference or noise. Therefore, a measurement to quantify the loop robustness to maintain the lock must be evaluated in terms of a low E_b/N_0. In this case, the linear analysis cannot hold any more. It is necessary to consider the entire lock range of the DLL. As is known, the DLL will lose the lock when the tracking error exceeds the ability of the DLL. The explicit expression of MTLL cannot be deduced according to the waveform of (3) and the $DD(.)$ of (12), but it is feasible to compare the MTLL performance based on the lock range of the discriminator characteristics, which is the distance between the two nearest zero-crossing points located on the left and right sides of $\tau_e=0$. The longer the lock range is, the longer the MTLL that can be achieved by the DLL.

4. Bit Error Rate (BER) and Timing Errors

UWB uses baseband pulses with nanosecond duration ranges to transmit information. This renders the system BER very sensitive to timing errors. Any small timing error will bring performance degradation to the system. The relationship between the BER in a 2PPM system and a tracking error in an AWGN environment is given in [11] as

$$P_e\left(\frac{E_b}{N_0},\tau_e\right)=Q\left(\sqrt{\frac{E_b}{N_0}}R_{PPM}(\tau_e)\right), \quad (14)$$

where $R_{PPM}(\tau_e)=\dfrac{R(\tau_e)-R(\delta-\tau_e)}{\sqrt{R(0)-R(\delta)}}$.

The BER performance vs. timing error at different E_b/N_0 values (5 dB, 7 dB, and 10 dB) is given in Fig. 7, where the delay error is normalized by T_p. A large degradation of BER occurs when the error is more than approximately $0.3T_p$. This implies that a small timing error causes serious system performance degradation. It also indicates that the performance of the DLL greatly affects the performance of the entire system.

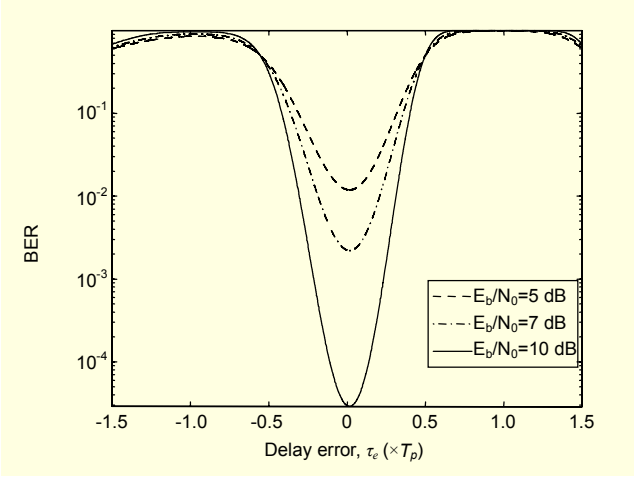

Fig. 7. BER vs. the delay error τ_e.

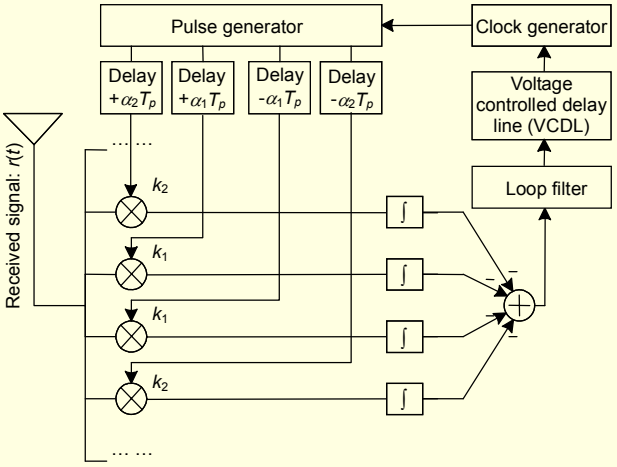

Fig. 8. Block diagram of the proposed DLL in a UWB.

III. The Proposed DLL for UWB-IR TH-SS System

We propose adding two more branches to the conventional DLL for a UWB-IR TH-SS system, which results in four branches in the DLL.

Figure 8 shows a block diagram of the proposed DLL. Four branches with delay parameters $\pm\alpha_1$ and $\pm\alpha_2$, and weight parameters k_1 and k_2 are correlated with the received signal $r(t)$. As the basic principle of this four-branch DLL is identical to that of a two-branch DLL, the discriminator characteristic $DD(\tau_e)$ can be deduced simply by

$$\begin{aligned} DD(\tau_e) = \frac{k_1 N_s}{2}\Big[& R(\tau_e - \delta - \alpha_1 T_p) - R(\tau_e + \delta - \alpha_1 T_p) \\ & + R(\tau_e - \delta + \alpha_1 T_p) - R(\tau_e + \delta + \alpha_1 T_p)\Big] \\ + \frac{k_1 N_s}{2}\Big[& R(\tau_e - \delta - \alpha_2 T_p) - R(\tau_e + \delta - \alpha_2 T_p) \\ & + R(\tau_e - \delta + \alpha_2 T_p) - R(\tau_e + \delta + \alpha_2 T_p)\Big]. \end{aligned} \quad (15)$$

The tracking jitter variance and MTLL of the DLLs are analyzed based on their gradients at τ_e=0 and the lock range of the discriminator characteristics curves. To reduce the computation complexity, the weight parameters k_1 and k_2 are set to 1. As in section II. 3, the tracking jitter variance is inversely proportional to the square of the gradient of the discriminator characteristic at τ_e=0, and the MTLL increases as the lock range increases. The tracking jitter variance and MTLL of different DLL schemes can be compared by the gradients at τ_e=0 and the lock range of the discriminator characteristics.

As the explicit closed form expressions of the gradients at τ_e=0 and the lock range of the discriminator characteristics cannot be deduced easily, a numerical enumeration method is used to evaluate the performance of these two figures of merit. The scale of the shift parameter α is limited to a range from 0 to 1.5T_p.

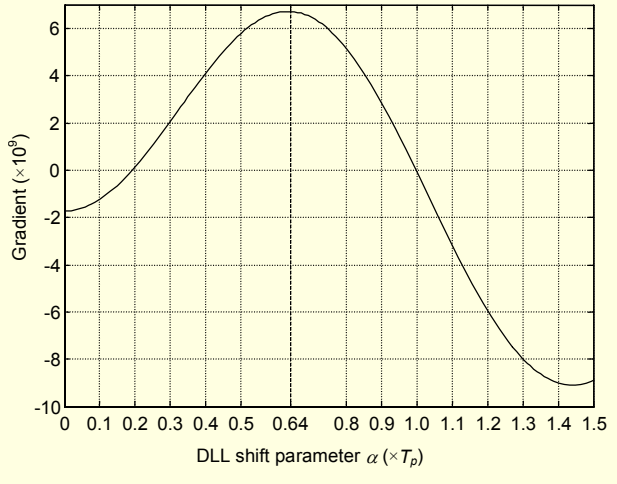

Fig. 9. Comparison of the gradient vs. different α's in two-branch DLLs.

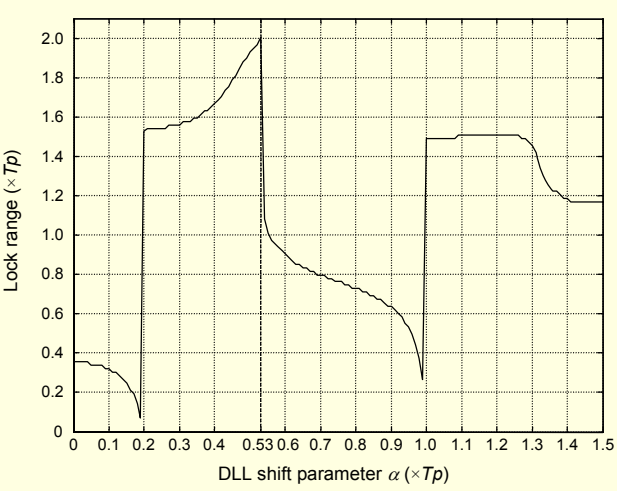

Fig. 10. Comparison of the lock range vs. different α's in two-branch DLLs.

First, the gradient at τ_e=0 of two-branch DLLs with the different shift parameter α is evaluated. The results are shown in Fig. 9. The highest gradient value can be achieved when α is approximately $0.64T_p$ and the corresponding gradient is approximately 6.7×10^9. Secondly, the lock range of the two-branch DLLs with the different shift parameter α is evaluated. The result is shown in Fig. 10. It is found that the longest lock range can be achieved when α is approximately $0.53T_p$ and the corresponding lock range is approximately $2.00T_p$.

The gradients at τ_e=0 and lock ranges of four-branch DLLs with different shift parameter sets (α_1, α_2) are also evaluated. As there are two variables α_1 and α_2, two dimension contour figures are adopted. The evaluation results are shown in Fig. 11 and Fig. 12, respectively. Given that α_1 and α_2 are interchangeable, the figures are in diagonal symmetry. The highest gradient value can be achieved at (α_1, α_2)= (0.64, 0.64)$\times T_p$ and the highest gradient is approximately 13.4×10^9. In addition, the longest lock range is achieved at

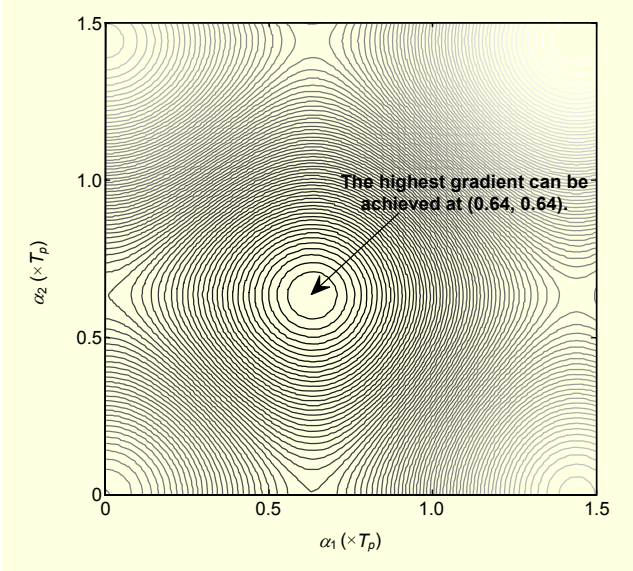

Fig. 11. Contour figure of the gradient vs. (α_1, α_2) in four-branch DLLs.

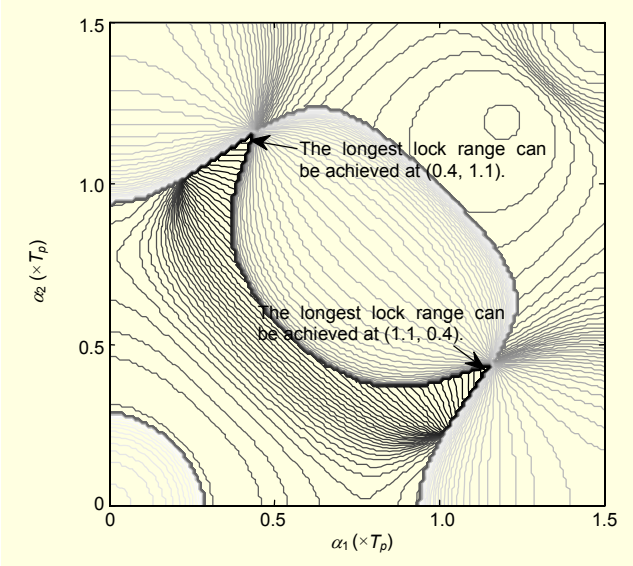

Fig. 12. Contour figure of the lock range vs. (α_1, α_2) in four-branch DLLs.

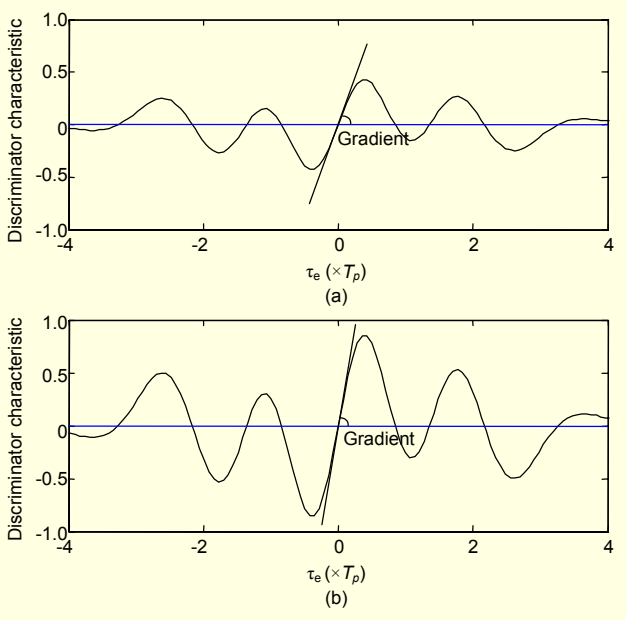

Fig. 13. Discriminator characteristics of (a) a two-branch DLL with $\alpha=0.64T_p$ and (b) a four-branch DLL with (α_1, α_2) = (0.64, 0.64)$\times T_p$.

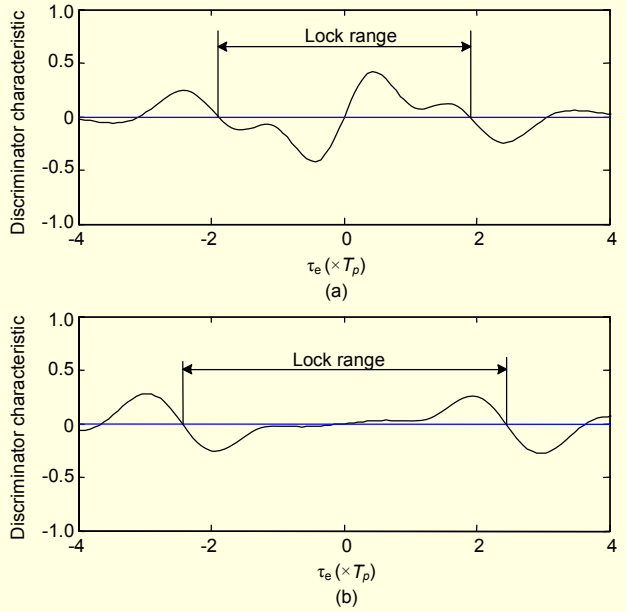

Fig. 14. Discriminator characteristics of (a) a two-branch DLL with $\alpha=0.53T_p$ and (b) a four-branch DLL with (α_1, α_2)= (1.1, 0.4)$\times T_p$.

$(\alpha_1, \alpha_2)=(1.1, 0.4)\times T_p$ and the longest lock range is approximately 2.45 T_p.

The discriminator characteristics of the two-branch schemes with $\alpha=0.53\ T_p$ and $0.64\ T_p$ are compared with that of the four-branch schemes with $(\alpha_1, \alpha_2)=(1.1, 0.4)\times T_p$ and $(\alpha_1, \alpha_2)=(0.64, 0.64)\times T_p$ in Fig. 13 and 14, respectively.

From the evaluation results, we draw the following conclusions.

1) In the traditional two-branch DLLs, the minimum tracking jitter variance can be achieved by setting $\alpha=0.53T_p$, and the longest MTLL can be achieved by setting $\alpha=0.64T_p$.
2) In the proposed four-branch DLLs, the minimum tracking jitter variance can be obtained by setting $(\alpha_1, \alpha_2)=(0.64, 0.64)\times T_p$. Compared with the maximum gradient (6.7×10^9) at $\tau_e=0$ of the two-branch schemes, a higher gradient (13.4×10^9) at $\tau_e=0$ can be achieved.
3) In the proposed four-branch DLLs, the longest MTLL can be achieved by setting $(\alpha_1, \alpha_2)=(1.1,0.4)\times T_p$. Compared with the longest lock range of the two-branch schemes $(2.00T_p)$, a longer lock range $(2.45T_p)$ can be achieved.
4) According to different application environments, four-branch DLLs can achieve smaller tracking jitter variance or higher MTLL than traditional two-branch DLLs by adjusting the shift parameters α_1 and α_2.
5) Even better performance can be achieved by the proposed four-branch DLLs or DLLs with more than four branches. The additional branches, however, also lead to higher implementation complexity in the system as more integration units and ADC units are required.

IV. Performance Comparison

The performance of the proposed four-branch schemes is compared with that of traditional two-branch DLLs via computer simulation in this section. As in the analysis previously discussed, the performance is evaluated here by two figures of merit: tracking jitter variance and MTLL. All simulations are based on the coherent DLL structures given in the previous sections. The pulse waveform $w_{rec}(t)$ is identical to that in (3), which is shown in Fig. 1. The time duration of one pulse is 4 ns. The pulse width parameter t_m=1 ns, and the reference time duration $T_p=t_m/\sqrt{\pi}$ is the main lobe of $w_{rec}(t)$. In the simulations, N_s is 16, and N_f is 4 for simplicity. The PPM modulation index δ is identical to T_p.

1. Comparison of Tracking Jitter Variance

Tracking jitter is an important figure of merit to evaluate a DLL when the delay error is small, that is, when the E_b/N_0 is high. In a well-designed DLL, the tracking jitter should be as small as possible. For high E_b/N_0 levels, tracking error τ_e fluctuates about the stable equilibrium point at $\tau_e=0$. The discriminator characteristic performs as a linear function in this duration.

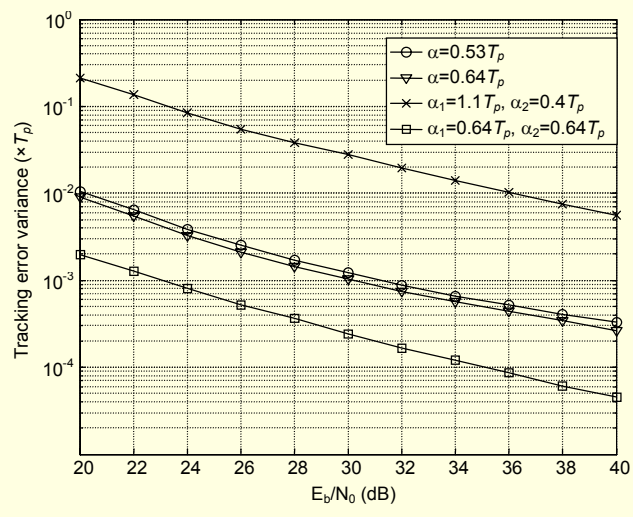

Fig. 15. Tracking jitter variance of different DLLs.

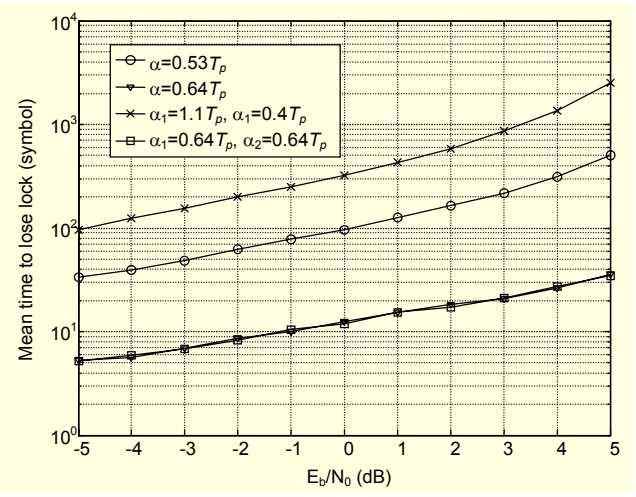

Fig. 16. MTLL of different DLLs.

The simulation results of the tracking jitter variance of the four schemes are shown in Fig. 15. As the tracking jitter variance reflects the anti-jitter abilities of the DLLs when the E_b/N_0 is high, this figure of merit is evaluated for a high E_b/N_0 (20 to 40 dB). As in section II. 3, the tracking jitter variance is inversely proportional to the square of the gradient of the discriminator characteristic $DD(.)$ at $\tau_e=0$. The simulation results strongly verify this conclusion.

The tracking jitter variance of the four-branch scheme of $(\alpha_1, \alpha_2)=(0.64, 0.64)\times T_p$ is the lowest from among the four evaluated schemes. In the two traditional two-branch DLLs with $\alpha=0.53T_p$ and $0.64T_p$, the DLL with $\alpha=0.64T_p$ outperforms the other scheme. However, it was unfortunately observed that the

tracking jitter variance of the four-branch scheme of $(\alpha_1, \alpha_2)=(1.1, 0.4)\times T_p$ is the highest, due to the lowest gradient of this scheme from among the four evaluated schemes.

2. Comparison of MTLL

As previously discussed, for a low E_b/N_0, the DLL should be sufficiently robust to maintain a lock. Therefore, it is a critical criterion in evaluation of a DLL. It is possible to compare the MTLL performance based on the lock range of the discriminator characteristics. The longer the lock range, the longer the MTLL that can be achieved.

The simulation results for the MTLL are shown in Fig. 16. All simulations are evaluated in low E_b/N_0 from −5 to 5 dB. As in the previous analysis, the four-branch scheme with $(\alpha_1, \alpha_2)=(1.1, 0.4)\times T_p$ has the longest lock range from among the four evaluated schemes. The simulation results also verify that this scheme has the longest MTLL of the four schemes. As the two-branch DLL with $\alpha=0.53T_p$ has the longest lock range of all two-branch DLLs, the longest MTLL in the two-branch schemes can be achieved by setting $\alpha=0.53T_p$. However, the proposed four-branch DLL with $(\alpha_1, \alpha_2)=(1.1, 0.4)\times T_p$ has a longer MTLL than all of the two-branch DLLs.

When the discriminator characteristic curves of the two-branch scheme are compared with $\alpha=0.64T_p$ and the four-branch scheme with $(\alpha_1, \alpha_2)=(1.1, 0.4)\times T_p$, the lock range of these two schemes are equal. Therefore, the MTLL performance of these two schemes should be similar. The simulation results verify this conclusion, even when the MTLL performance of each of these two schemes is very poor.

V. Conclusion

In this paper, an improved DLL with four branches in a UWB-IR TH-SS system was proposed and evaluated. By adjusting the delay parameters of the four branches, reduced tracking jitter variance and extended MTLL were achieved. Through analyses and simulations, the optimal design parameters for the proposed schemes were obtained. For a moderate or high E_b/N_0, low tracking jitter variance is the main design object of the DLL. By setting $(\alpha_1, \alpha_2)=(0.64, 0.64)\times T_p$, the lowest tracking jitter variance can be obtained. In contrast, for a low E_b/N_0, a long MTLL is the main design object of the DLL. By setting $(\alpha_1, \alpha_2)=(1.1, 0.4)\times T_p$, the longest MTLL can be obtained. In conclusion, by adding two additional branches with proper parameters, better performance compared to two-branch DLLs is achieved by the proposed four-branch DLLs.

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