A Versatile Universal Capacitor-Grounded Voltage-Mode Filter Using DVCCs

Hua-Pin Chen and Sung-Shiou Shen

In this paper, a versatile three-input five-output universal capacitor-grounded voltage-mode filter is proposed. The circuit employs two differential voltage current conveyors as active elements together with two grounded capacitors and four resistors as passive elements. The proposed configuration can be used as either a single-input five-output or three-input two-output. Unlike the previously reported works, it can simultaneously realize five different generic filtering signals: lowpass, bandpass, highpass, bandreject, and allpass. It still maintains the following advantages: (i) the employment of all grounded capacitors, (ii) no need to employ inverting-type input signals, (iii) no need to impose component choice, (iv) orthogonal control of the resonance angular frequency ω_o and the quality factor Q, and (v) low active and passive sensitivity performances.

Keywords: Analog electronics, active filters, current conveyors.

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I. Introduction

As a current-mode active device, the differential voltage current conveyor (DVCC) has the advantages of both the second-generation current conveyor (CCII) (such as large signal bandwidth, great linearity, and wide dynamic range) and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability) [1]. This element is a versatile building block whose applications appear in the literature [1]-[7]. Many voltage-mode multifunction filters using current conveyors have been proposed [8]-[12]. However, these configurations require at least four active components.

In 2003, Chang and others proposed a voltage-mode multifunction filter with a single input and four outputs [13]. In 2004, Horng and others proposed another multifunction filter with a single input and three outputs [14]. However, with these two proposed configurations only three standard filter signals can be simultaneously obtained. In 2006, Horng and others. proposed four voltage-mode universal biquadratic filters with a single input and five outputs [15]. The proposed circuits can realize highpass (HP), bandpass (BP), lowpass (LP), bandreject (BR), and allpass (AP) simultaneously, but need a component-matching condition to realize the AP filter response. Also, each of the proposed circuit employs many more passive components.

In 2007, Chen [16] proposed another voltage-mode universal biquadratic filter with a single input and five outputs using two differential difference current conveyors (DDCCs), two grounded capacitors, and three resistors. The circuit uses one Z+ output device, whereas the proposed circuit uses two Z outputs. The circuit uses three Y inputs, whereas the proposed circuit uses only two Y inputs. The two capacitors in each of the two DVCCs are similarly positioned at the Z output

terminals. The circuit in [16] can realize the AP filter without any component-matching condition. However, it needs to make capacitor C_1 float and insert another voltage input signal V_{in} into the floating terminal of capacitor C_1. In this paper, the proposed circuit also can realize the AP filter without any component-matching condition and still employ the grounded capacitor, unlike the biquad reported in [16].

On the other hand, some universal voltage-mode biquads with multiple inputs and one output have been proposed [17]-[24]. However, these configurations cannot be realized by using only grounded capacitors. Also, they suffer from either inverting-type input signals or component-matching conditions. In 2003, Chang and Chen [25] proposed a universal voltage-mode filter with three inputs and a single output. The circuit has additional advantages, such as the employment of only grounded capacitors, no need for inverting-type input signals, and no need for component-matching conditions. However, it still suffers from orthogonal control of ω_o and Q. In this paper, the proposed circuit has the same advantages reported by Chang and Chen [25] in addition to one more important advantage—orthogonal control of ω_o and Q. The proposed new circuit offers the following features: (i) simultaneous realization of LP, BP, HP, BR, and AP responses with the single-input five-output or three-input two-output in the same configuration; (ii) the employment of all grounded capacitors; (iii) no need to employ inverting-type input signals; (iv) no need to impose component choice; (v) orthogonal control of the ω_o and Q; and (vi) low active and passive sensitivity performance. In Table 1, the main features of the proposed new circuit are compared with those of previous works.

Table 1. Summary of recent filters specifications.

Criteria / Circuits	(i)	(ii)	(iii)	(iv)	(v)	(vi)
The new circuit	yes	yes	yes	yes	yes	yes
Ref. [16] in 2007	no	yes	yes	no	yes	no
Ref. [15] in 2006	no	yes	yes	no	yes	yes
Ref. [14] in 2004	no	yes	yes	yes	no	yes
Ref. [13] in 2003	no	yes	yes	yes	no	yes
Ref. [25] in 2003	no	yes	yes	yes	no	yes
Ref. [24] in 2005	no	no	no	yes	yes	no
Ref. [23] in 2004	no	no	no	no	no	no

II. The Proposed Circuit

The block diagram of the DVCC is shown in Fig. 1 and its terminal relations are given by

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix}. \quad (1)$$

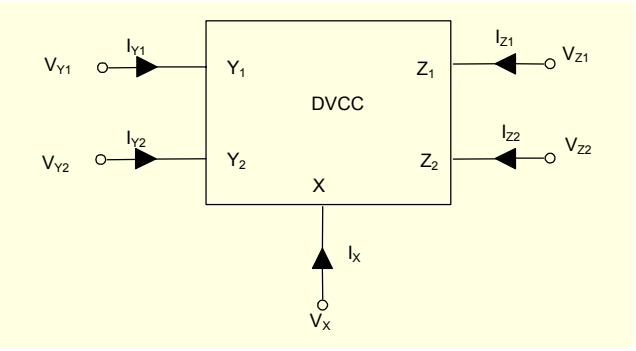

Fig. 1. Block diagram of the DVCC.

The proposed versatile universal voltage-mode circuit comprises two DVCCs, two grounded capacitors and four resistors, as shown in Fig. 2. The use of grounded capacitors is particularly attractive for integrated circuit implementation [25]. Derived by each nodal equation of the proposed circuit, the input-output relationship matrix form of Fig. 2 can be expressed as

$$\begin{bmatrix} sC_1 & G_1 & -G_1 & 0 & 0 \\ -G_2 & sC_2 & 0 & 0 & 0 \\ G_2 & 0 & G_3 & 0 & 0 \\ 0 & -1 & 1 & 1 & 0 \\ 0 & -G_1 & G_1 & 0 & G_4 \end{bmatrix} \begin{bmatrix} V_{o1} \\ V_{o2} \\ V_{o3} \\ V_{o4} \\ V_{o5} \end{bmatrix} = \begin{bmatrix} G_1 V_{i2} \\ -G_2 V_{i3} \\ G_3 V_{i1} + G_2 V_{i3} \\ 0 \\ -G_1 V_{i2} \end{bmatrix}, \quad (2)$$

where

$$G_1 = \frac{1}{R_1},\ G_2 = \frac{1}{R_2},\ G_3 = \frac{1}{R_3}, \text{ and } G_4 = \frac{1}{R_4}.$$

From the above matrix form, the following five output voltages can be derived:

$$V_{o1} = \frac{1}{\Delta}[(sC_2G_1G_3)V_{i1} + (sC_2G_1G_3)V_{i2} + (sC_2G_1G_2 + G_1G_2G_3)V_{i3}], \quad (3)$$

$$V_{o2} = \frac{1}{\Delta}[(G_1G_2G_3)V_{i1} + (G_1G_2G_3)V_{i2} - (sC_1G_2G_3)V_{i3}], \quad (4)$$

$$V_{o3} = \frac{1}{\Delta}[(s^2C_1C_2G_3 + G_1G_2G_3)V_{i1} - (sC_2G_1G_2)V_{i2} + (s^2C_1C_2G_2)V_{i3}], \quad (5)$$

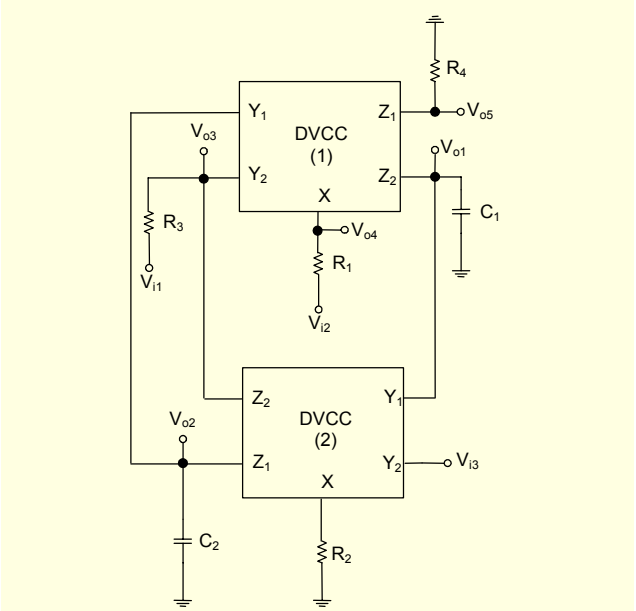

Fig. 2. Block diagram of the proposed versatile voltage-mode biquad based on DVCCs.

$$V_{o4} = \frac{1}{\Delta}[-(s^2C_1C_2G_3)V_{i1} + (sC_2G_1G_2 + G_1G_2G_3)V_{i2} - (s^2C_1C_2G_2 + sC_1G_2G_3)V_{i3}], \quad (6)$$

$$V_{o5} = \frac{1}{\Delta}(\frac{G_1}{G_4})[-(s^2C_1C_2G_3)V_{i1} - (s^2C_1C_2G_3)V_{i2} - (s^2C_1C_2G_2 + sC_1G_2G_3)V_{i3}], \quad (7)$$

where

$$\Delta = s^2C_1C_2G_3 + sC_2G_1G_2 + G_1G_2G_3 . \quad (8)$$

Depending on the status of the three biquad input voltages, V_{i1}, V_{i2}, and V_{i3}, numerous filter functions are obtained. There are two cases shown as follows.

Case 1. If $V_{i2} = V_{i3} = 0$ and $V_{i1} = V_{in}$, then

$$\frac{V_{o1}}{V_{in}} = \frac{1}{\Delta}(sC_2G_1G_3) , \quad (9)$$

$$\frac{V_{o2}}{V_{in}} = \frac{1}{\Delta}(G_1G_2G_3) , \quad (10)$$

$$\frac{V_{o3}}{V_{in}} = \frac{1}{\Delta}(s^2C_1C_2G_3 + G_1G_2G_3) , \quad (11)$$

$$\frac{V_{o4}}{V_{in}} = \frac{1}{\Delta}(-s^2C_1C_2G_3) , \quad (12)$$

$$\frac{V_{o5}}{V_{in}} = \frac{1}{\Delta}[-(\frac{G_1}{G_4})(s^2C_1C_2G_3)] , \quad (13)$$

where

$$\Delta = s^2C_1C_2G_3 + sC_2G_1G_2 + G_1G_2G_3 . \quad (14)$$

It can be seen from (9) to (13) that a BP filter response is obtained from V_{o1}, an LP filter response is obtained from V_{o2}, a BR filter response is obtained from V_{o3}, and two HP filter responses are obtained from V_{o4} and V_{o5}, respectively. If $V_{i3} = 0$ and $V_{i1} = V_{i2} = V_{in}$, then the AP transfer function is easily obtained from the node of V_{o3} as

$$\frac{V_{o3}}{V_{in}} = \frac{s^2C_1C_2G_3 - sC_2G_1G_2 + G_1G_2G_3}{s^2C_1C_2G_3 + sC_2G_1G_2 + G_1G_2G_3} . \quad (15)$$

Obviously, from (9) to (15), it can be seen that the proposed circuit is a universal voltage-mode filter, too. Also, (9) to (15) demonstrate that the BP gain constant H_{BP}, the LP gain constant H_{LP}, the BR gain constant H_{BP}, the first HP gain constant H_{HPI}, the second HP gain constant H_{HP2}, and the AP gain constant H_{AP} are given by

$$H_{BP} = \frac{G_3}{G_2} , H_{LP} = H_{BR} = 1 , H_{HP1} = -1 , H_{HP2} = -\frac{G_1}{G_4} ,$$

$$\text{and} \quad H_{AP} = 1 . \quad (16)$$

Case 2. The specialization of the numerators in (4) and (5) result in the five generic filter functions:

(i) lowpass: $V_{i3} = 0$, $V_{i1} = V_{in}$ or $V_{i2} = V_{in}$, and $V_{out} = V_{o2}$;
(ii) bandpass: $V_{i1} = V_{i3} = 0$, $V_{i2} = V_{in}$, and $V_{out} = V_{o3}$;
(iii) highpass: $V_{i1} = V_{i2} = 0$, $V_{i3} = V_{in}$, and $V_{out} = V_{o3}$;
(iv) bandreject: $V_{i2} = V_{i3} = 0$, $V_{i1} = V_{in}$, and $V_{out} = V_{o3}$;
(v) allpass: $V_{i3} = 0$, $V_{i1} = V_{i2} = V_{in}$, and $V_{out} = V_{o3}$.

Note that there are not any component-matching conditions and inverting-type voltage input signals to realize all of the filter responses. In all cases the resonance angular frequency ω_o and quality factor Q are given by

$$\omega_o = \sqrt{\frac{G_1G_2}{C_1C_2}} \quad \text{and} \quad Q = G_3\sqrt{\frac{C_1}{C_2G_1G_2}} . \quad (17)$$

The ω_o and Q can be properly controlled by G_1 and/or G_2 and G_3, in that order.

From cases 1 and 2, we can note that the proposed circuit can act as a universal voltage-mode with single input and five outputs and can realize voltage-mode BR, LP, BP, and two HP filter signals from the five output terminals, without any component-matching conditions. When another input signal is inserted into the circuit, the AP filter response can be easily

realized without any component-matching condition. On the other hand, it also can act as a universal voltage-mode filter with three inputs and two outputs and can realize five generic voltage-mode filter signals from the same configuration without any component-matching conditions and inverting-type voltage input signals to realize all of the filter responses. Obviously, the filter configuration with multiple inputs and multiple outputs seems to be more suitable than a single input and multiple outputs configuration or the multiple inputs and a single output configuration.

III. Effect of Non-idealities

Equations (3) to (17) have been obtained by considering the ideal description of the DVCC. Ports Y_1 and Y_2 exhibit an infinite input resistance. Port X exhibits zero input resistance and the output ports Z_1 and Z_2 show an infinite output resistance. Practically, when implementing the active element using transistors, these resistances assume some finite value depending upon the device parameters. Similarly, the high frequency effects also need to be accounted for by assuming capacitances at these ports. The non-ideal DVCC symbol with various parasitic elements is shown in Fig. 3. It is shown that port X exhibits low-value parasitic serial resistance Rx, and ports Y_1 and Y_2 exhibit high-value parasitic resistance R_{Y1} and R_{Y2}, respectively. The ports Z_1 and Z_2 exhibit high-value parasitic resistance R_{Z1} and R_{Z2} in parallel with low-value capacitors C_{Z1} and C_{Z2}. It is to be noted that the proposed circuit employs resistors at the X terminals of the DVCCs; therefore, most of the parasitic R_x can be easily merged.

Taking the non-idealities of the DVCC into account, the relationships of the terminal voltages and currents can be rewritten as $V_X = \beta_{1k}(s)V_{Y1} - \beta_{2k}(s)V_{Y2} + R_X I_X$, $I_{Y1} = I_{Y2} = 0$, $I_{Z1} = +\alpha_{1k}(s)I_X$, $I_{Z2} = -\alpha_{2k}(s)I_X$, where $\beta_{1k}(s)$ represents the voltage transfers from the V_{Y1} terminal to the V_X terminal of the k-th DVCC, $\beta_{2k}(s)$ represents the voltage transfers from V_{Y2} terminal to V_X terminal of the k-th DVCC, $\alpha_{1k}(s)$ represents the current transfers from I_X terminal to I_{Z1} terminal of the k-th DVCC, and $\alpha_{2k}(s)$ represents the current transfers from I_X terminal to I_{Z2} terminal of the k-th DVCC. Thus, $\alpha_{1k}(s)$, $\alpha_{2k}(s)$, $\beta_{1k}(s)$, and $\beta_{2k}(s)$ can be approximated by LP functions, which can be considered to have a unity value for frequencies much lower than their corner frequencies [3]-[7]. By assuming the circuit is working at frequencies much lower than the corner frequencies of $\alpha_{1k}(s)$, $\alpha_{2k}(s)$, $\beta_{1k}(s)$, and $\beta_{2k}(s)$, namely, $\beta_{1k}(s) = \beta_{1k} = 1 - \varepsilon_{1kv}$ and ε_{1kv} ($|\varepsilon_{1kv}| \ll 1$) which denotes the voltage tracking error from the V_{Y1} terminal to the V_X terminal of the k-th DVCC, $\beta_{2k}(s) = \beta_{2k} = 1 - \varepsilon_{2kv}$ and ε_{2kv} ($|\varepsilon_{2kv}| \ll 1$) which denotes the voltage tracking error from the V_{Y2} terminal to the V_X terminal of the k-th DVCC, $\alpha_{1k}(s) = \alpha_{1k} = 1 - \varepsilon_{1ki}$, and ε_{1ki} ($|\varepsilon_{1ki}| \ll 1$) which denotes the current tracking error from the I_X terminal to the I_{Z1} of the k-th DVCC, and $\alpha_{2k}(s) = \alpha_{21k} = 1 - \varepsilon_{2ki}$ and ε_{2ki} ($|\varepsilon_{2ki}| \ll 1$) which denote the current tracking error from I_X terminal to I_{Z2} of the k-th DVCC, the denominator of the transfer functions becomes

$$D(s) = s^2 C_1 C_2 G_3 + \alpha_{21}\alpha_{22}\beta_{12}\beta_{21} s C_2 G_1' G_2' + \alpha_{12}\alpha_{21}\beta_{11}\beta_{12} G_1' G_2' G_3, \quad (18)$$

where

$$G_1' = \frac{1}{R_{X1} + R_1}, \quad G_2' = \frac{1}{R_{X2} + R_2}, \quad \text{and} \quad G_3 = \frac{1}{R_3}.$$

The resonance angular frequency ω_o and quality factor Q are obtained by

$$\omega_o = \sqrt{\frac{\alpha_{12}\alpha_{21}\beta_{11}\beta_{12} G_1' G_2'}{C_1 C_2}}, \quad (19)$$

$$Q = \frac{G_3}{\alpha_{22}\beta_{21}} \sqrt{\frac{\alpha_{12}\beta_{11} C_1}{\alpha_{21}\beta_{12} C_2 G_1' G_2'}}. \quad (20)$$

The low active and passive sensitivities of ω_o and Q are shown as

$$S_{\alpha_{12}}^{\omega_o} = S_{\alpha_{21}}^{\omega_o} = S_{\beta_{11}}^{\omega_o} = S_{\beta_{12}}^{\omega_o} = S_{G_1'}^{\omega_o} = S_{G_2'}^{\omega_o} = \frac{1}{2}, \quad (21)$$

$$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2}, \quad (22)$$

$$S_{\alpha_{12}}^{Q} = S_{\beta_{11}}^{Q} = S_{C_1}^{Q} = \frac{1}{2}, \quad (23)$$

$$S_{\alpha_{21}}^{Q} = S_{\beta_{12}}^{Q} = S_{C_2}^{Q} = S_{G_1'}^{Q} = S_{G_2'}^{Q} = -\frac{1}{2}, \quad (24)$$

$$S_{G_3}^{Q} = 1, \quad (25)$$

$$S_{\alpha_{22}}^{Q} = S_{\beta_{21}}^{Q} = -1. \quad (26)$$

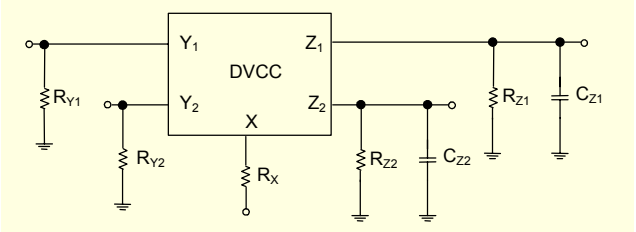

Fig. 3. Blick diagram of the DVCC with its parasitic elements.

IV. Simulation Results

Finally, to verify the theoretical prediction of the proposed biquad circuit, a simulation using H-Spice with a TSMC 0.25 μm process [26] was performed. The symmetrical cascaded CMOS implementation of the DVCC is shown in Fig. 4 [4] with the NMOS and PMOS transistor aspect ratios $(W/L = 5\mu/1\mu)$ and $(W/L = 10\mu/1\mu)$, respectively. The supply voltages were V_{DD}=-V_{SS}=1.25 V, and the biasing voltages were V_{B1}=-0.2 V and V_{B2}=-0.45 V. The proposed circuit was designed for f_o=1 MHz and Q=3.16 by choosing R_1=R_3=5 kΩ, R_2=R_4=50 kΩ, and C_1=C_2=10 pF. Figure 5 shows the simulated amplitude responses for the BR, LP, BP, and two HP filters of Fig. 2 with V_{i2}=V_{i3}=0, and V_{i1}=V_{in}. Figure 6 shows the simulated amplitude and phase responses for the AP filter at the output V_{o3} of Fig. 2 with V_{i3}=0, and V_{i1}=V_{i2}=V_{in}. Figure 7 shows the simulated amplitude responses for the BR, LP, BP, and HP filters in case 2 of Fig. 2. As can be seen, there is a close agreement between theory and simulation.

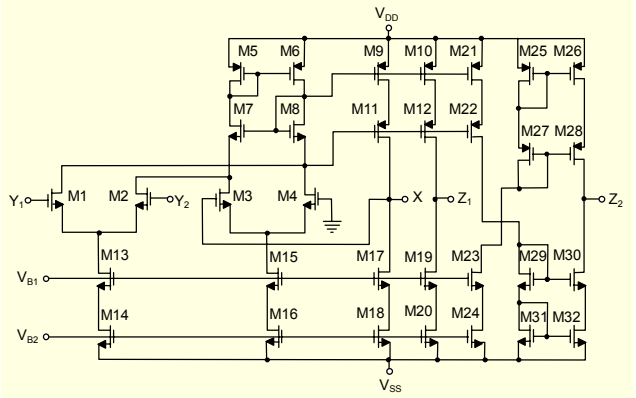

Fig. 4. CMOS implementation of DVCC.

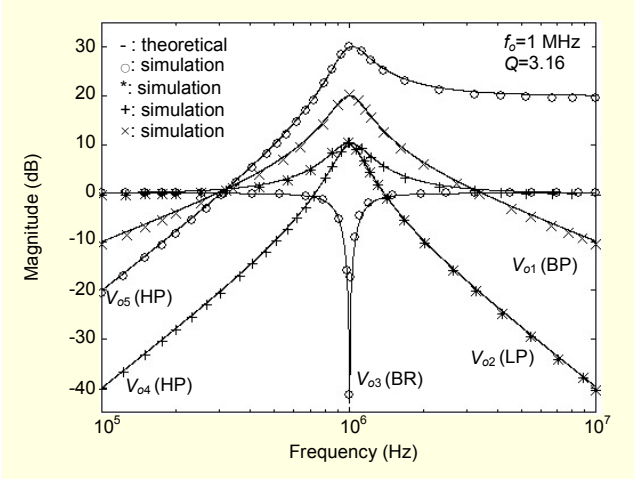

Fig. 5. Amplitude–frequency responses in case 1 of Fig. 2.

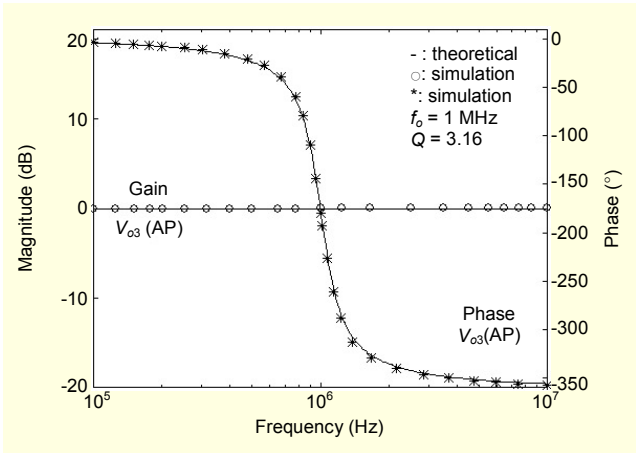

Fig. 6. Amplitude–frequency response and phase–frequency response of Fig. 2 with V_{i3}= 0 and V_{i1} = V_{i2} = V_{in}.

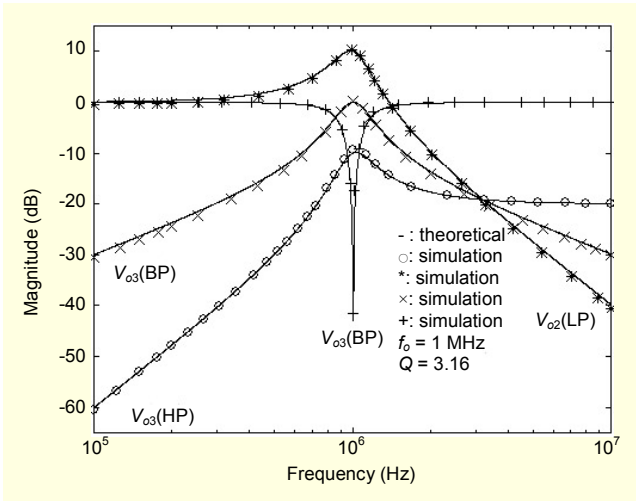

Fig. 7. Amplitude–frequency responses in case 2 of Fig. 2.

V. Conclusion

In this paper, a new universal voltage-mode filter was proposed. The proposed circuit can be used as either a three-input two-output universal filter or single-input five-output multifunction filter with the same topology. It is more versatile than the universal one with a single input and multiple outputs or the universal one with multiple inputs and one or two outputs. Moreover, the proposed circuit still offers the following advantages: (i) the employment of two grounded capacitors, (ii) no need to employ inverting-type input signals, (iii) no need to impose component choice, (iv) orthogonal control of ω_o and Q, and (v) low active and passive sensitivity performance. H-Spice simulations with TSMC 0.25 μm process and ±1.25 V supply voltages confirm the theoretical predictions.

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