A Phase-Locked Loop with Embedded Analog-to-Digital Converter for Digital Control

Sooho Cha, Chunseok Jeong, and Changsik Yoo

A phase-locked loop (PLL) is described which is operable from 0.4 GHz to 1.2 GHz. The PLL has basically the same architecture as the conventional analog PLL except the locking information is stored as digital code. An analog-to-digital converter is embedded in the PLL, converting the analog loop filter output to digital code. Because the locking information is stored as digital code, the PLL can be turned off during power-down mode while avoiding long wake-up time. The PLL implemented in a 0.18 μm CMOS process occupies 0.35 mm^2 active area. From a 1.8 V supply, it consumes 59 mW and 984 μW during the normal and power-down modes, respectively. The measured rms jitter of the output clock is 16.8 ps at 1.2 GHz.

Keywords: Phase-locked loop, digital control, CMOS.

I. Introduction

Phase-locked loops (PLLs) are widely used for various purposes such as frequency multiplication, clock synchronization, and zero-delay buffering [1]-[4]. Among several types of PLL, the charge pump (CP) PLL shown in Fig. 1 is most widely used due to its simple architecture and superior performance. In a CP PLL, the oscillation frequency of the voltage controlled oscillator (VCO) is stored as analog voltage on loop filter output. Therefore, during the power-down mode, that is, while the output clock of the PLL is not necessary, it is very difficult to turn the PLL off because it would take a long time for the PLL to be re-locked due to the loss of locking information stored as analog voltage. If the PLL remains running during the power-down mode, the power consumption would be substantial.

In order to alleviate this problem of the analog CP PLL, an all-digital PLL might be used where the VCO is substituted by a digitally controlled oscillator (DCO) and phase error is detected by a time-to-digital converter (TDC) as shown in Fig. 2 [4]. A digital PLL can be turned off without any

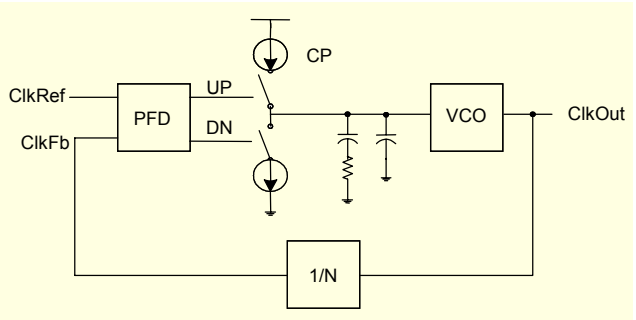


Fig. 1. Conventional analog charge-pump PLL.

Manuscript received Aug. 10, 2006; revised Mar. 02, 2007.

This work was supported by Hynix Semiconductor. The CAD tools were provided by IDEC.

Sooho Cha (phone: + 82 31 208 7593, email: sooho.cha@samsung.com) was with the Department of Electronics and Computer Engineering, Hanyang University, Seoul, S. Korea, and is now with Advanced Technology Development Team, Memory Division, Samsung Electronics, Hwaseong, Gyeonggi-do, S. Korea.

Chunseok Jeong (email: chunseok.jeong@hynix.com) was with the Department of Electronics and Computer Engineering, Hanyang University, Seoul, S. Korea, and is now with DRAM Design Team 4, Hynix Semiconductor Inc., Incheon, S. Korea.

Changsik Yoo (phone: +82 2 2297 3361, email: csyoo@hanyang.ac.kr) is with the Department of Electronics and Computer Engineering, Hanyang University, Seoul, S. Korea.

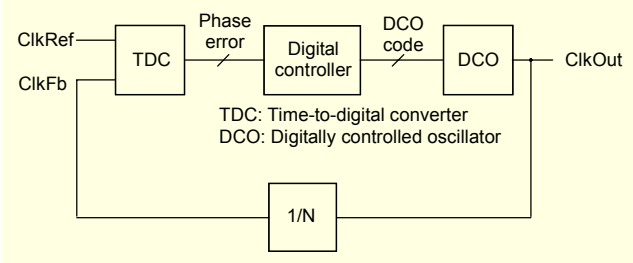


Fig. 2. Conventional all-digital PLL.

concern about the wake-up time because all the locking information is stored as digital code. The jitter and locking accuracy (static phase error) of the digital PLL are determined by the minimum time step provided by the TDC and DCO. To minimize jitter and static phase error, the delay of the delay cells must be minimized. However, for a given clock period, the smaller delay of the delay cells means a larger number of delay cells because the total delay (sum of delays of all delay cells) must be equal to the clock period. Therefore, for a smaller step with a given clock period, a larger silicon area and higher power consumption are required because a larger number of delay cells with smaller delay is required.

In this paper, an alternative technique is proposed which allows an analog PLL to be turned off during power-down mode without increasing wake-up time [5]. Neither DCO nor TDC is used. Instead, a tracking analog-to-digital converter (ADC) is embedded in the feedback loop of the analog CP PLL. The operation principle of the PLL is described in the next section, and the experimental results on a 0.4 GHz to 1.2 GHz PLL implemented in a 0.18 μm CMOS process follow in section III. Finally, the conclusion is given in section IV.

II. Analog PLL with Embedded ADC in Feedback Loop for Digital Control

The proposed analog PLL has basically the same architecture as the conventional analog CP PLL as shown in Fig. 3. The difference is that the tracking ADC is embedded in the feedback loop to convert the analog VCO control voltage to digital code.

Because the PLL is digitally controlled, there is bang-bang jitter. The ADC has 10-bit resolution to provide sufficient locking accuracy and jitter performance. With higher resolution of the ADC, better jitter performance can be achieved but the area and power consumption will be larger. The resolution of the ADC is determined so the bang-bang jitter due to the ADC quantization is smaller than 20 ps. The ADC comprises a comparator, counter, and digital-to-analog converter (DAC).

The loop filter output is compared with the output of the 10-bit DAC, and the counter counts up or down accordingly. The

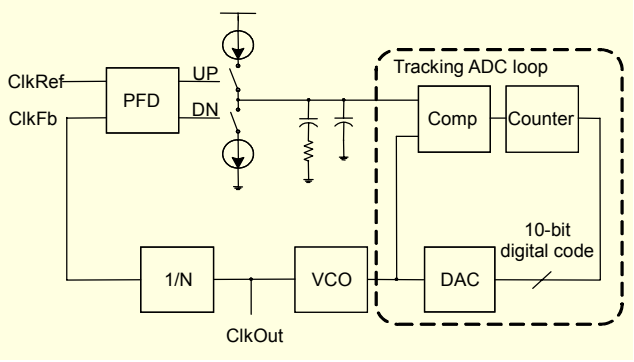


Fig. 3. Proposed PLL with embedded ADC for digital control.

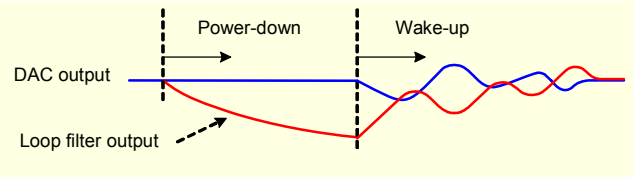


Fig. 4. Effect of floating loop filter output during power-down mode.

ADC itself is a feedback system; thus, there are two feedback loops in the PLL. To prevent the ADC from affecting the stability of the global feedback of the PLL, the loop bandwidth of the ADC is designed to be much wider than that of the global feedback loop of the PLL.

While the PLL is turned off (power-down mode), the phase frequency detector (PFD) and CP are turned off, which means the loop filter output is floating. Therefore, the loop filter output can deviate from its originally locked value determined during normal operation. Of course, the 10-bit digital code of the DAC does not change even during the power-down mode, which means the outputs of the DAC and the loop filter are not equal during the power-down mode. When the PLL wakes up from the power-down mode, the ADC loop tries to equalize the DAC output to the loop filter output, although the DAC output already has the correct value. Then, the PLL must be re-locked, resulting in a long wake-up time as shown in Fig. 4. To avoid this, a switch is inserted between the DAC and the loop filter as shown in Fig. 5. The switch is turned on during the power-down mode to prevent the loop filter output from floating and to ensure that the loop filter output is the same as the DAC output. The clock inputs of the 10-bit counter and DAC are delayed in relation to that of the comparator to provide a sufficient timing margin for each block.

Because the output of the DAC controls the VCO, the glitch of the DAC which occurs when the control code changes must be minimized (For example, with binary weighted architecture, a large glitch occurs when the code changes from 0111111111 to 1000000000). Therefore, the 10-bit DAC is thermometer

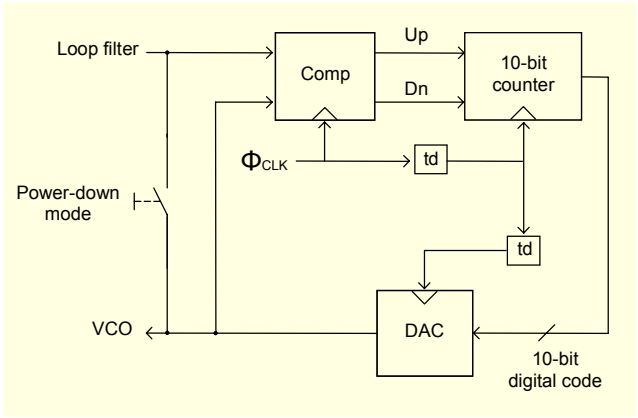


Fig. 5. Tracking ADC loop with switch between the DAC and loop filter outputs to prevent the loop filter output from floating during power-down mode.

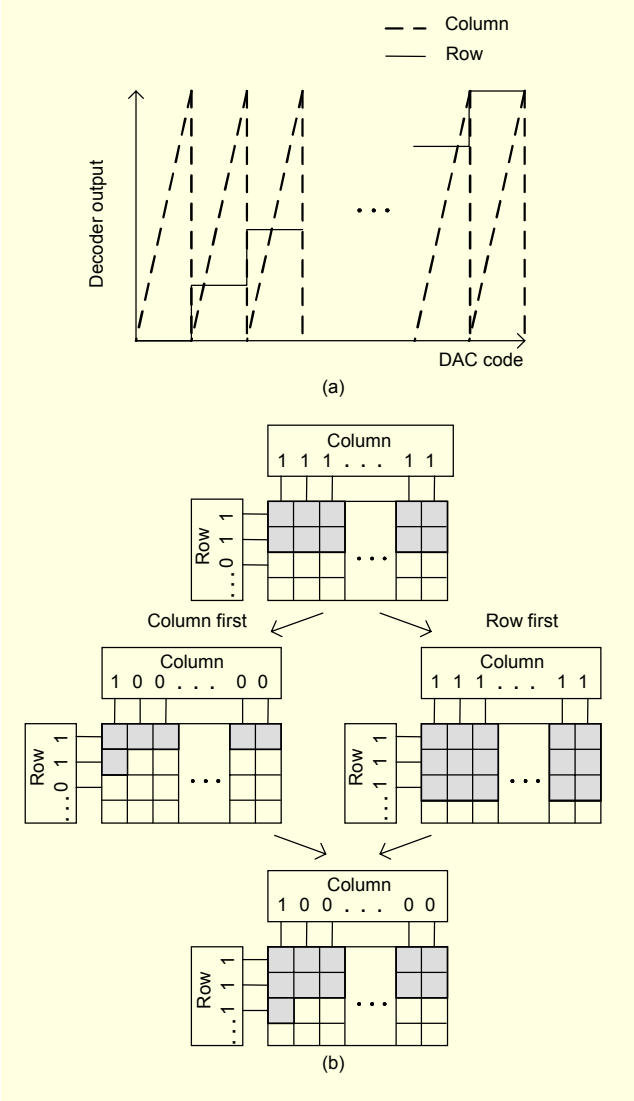


Fig. 6. (a) Conventional decoding scheme of thermometer-coded DAC and (b) the mechanism of large glitch generation.

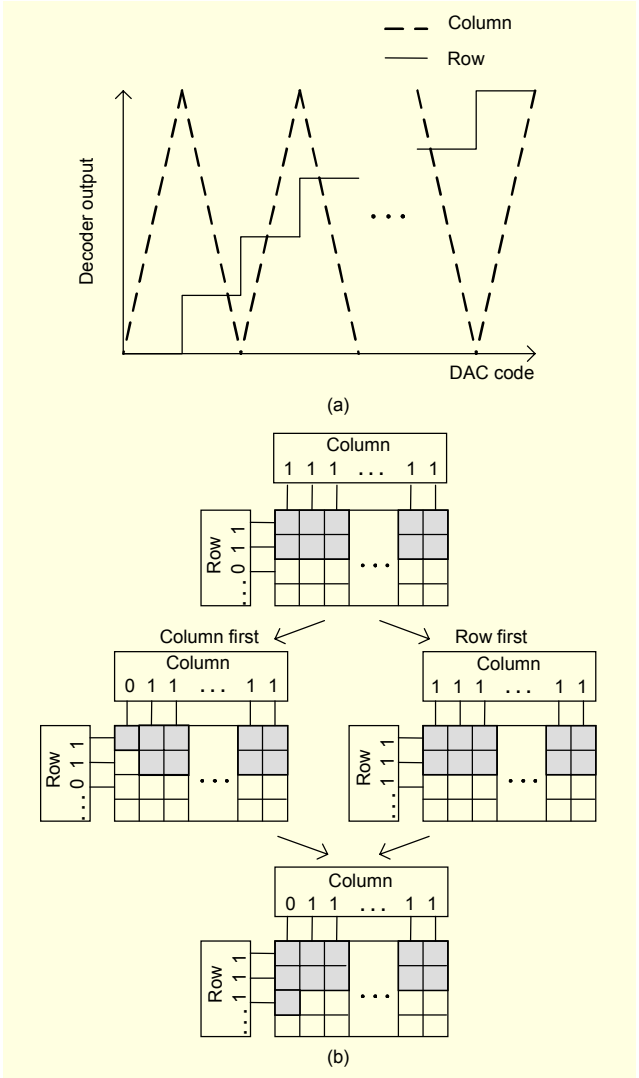


Fig. 7. (a) Decoding scheme for glitch minimization and (b) the principle of glitch minimization.

coded and built with a segmented structure of 9 bits with unit current cells and 1 bit with a binary scaled current cell [6]. The array of the current cells is configured as a four by five matrix.

With a conventional decoding scheme, rows are selected first, and then an appropriate number of columns is selected as shown in Fig. 6(a). If mismatch exists between the delays of the control signal paths for the row and column switch, the thermometer-coded DAC still exhibits a large glitch when another row is selected as shown in Fig. 6(b) [4], [5]. If the column (row) control path is faster, one less (more) row is temporarily selected, creating a large glitch. To avoid this problem, the improved decoding scheme shown in Fig. 7(a) proposed in [4] is adopted. This scheme uses different control logics for even and odd rows and limits the glitch to less than 2-LSB even with delay mismatch between column and row control signals as shown in Fig. 7(b).

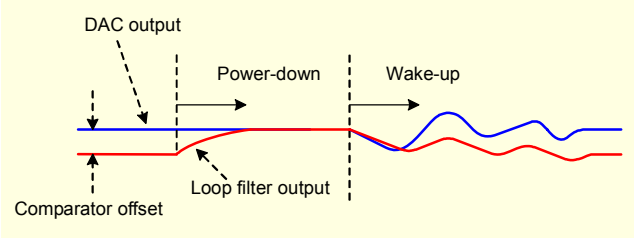


Fig. 8. Offset of comparator results in long wake-up time.

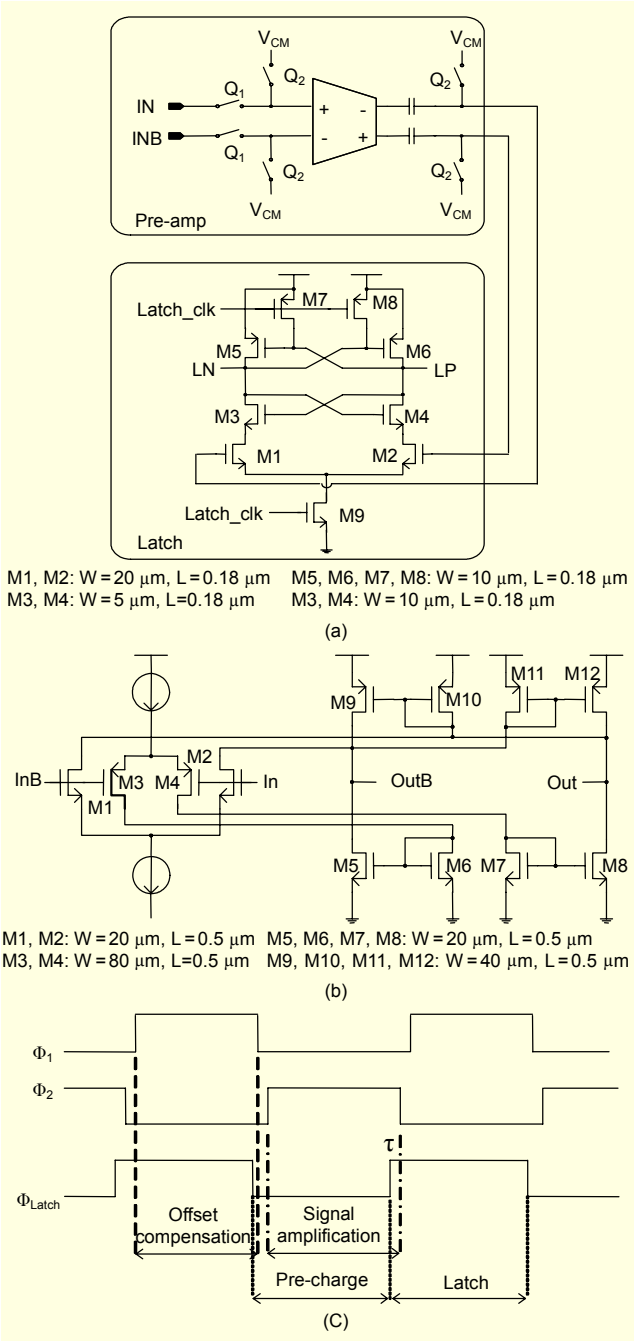


Fig. 9. (a) Offset compensated comparator, (b) pre-amplifier with rail-to-rail input common-mode range and (W/L) of the transistors (all in μm), and (c) timing diagram.

Even with the input offset of the comparator, the PLL can be locked with some difference between the outputs of the loop filter and DAC at the completion of locking. However, the offset of the comparator must still be compensated. During the power-down mode, the loop filter output is forced to be the same as the DAC output to prevent the loop filter output floating and to enable fast wake-up as explained above. If the locked value of the loop filter output is different from the DAC output due to the input offset of the comparator, the PLL should be re-locked when the system exits from the power-down mode as illustrated in Fig. 8.

As shown in Fig. 9(a), the comparator is composed of a pre-amplifier and a sense-amplifier type latch where the input offset is compensated at the pre-amplifier output [7]. Because the control voltage of the VCO can vary within a wide range, the pre-amplifier of the comparator employs a rail-to-rail input stage as shown in Fig. 9(b). The timing of the comparator is

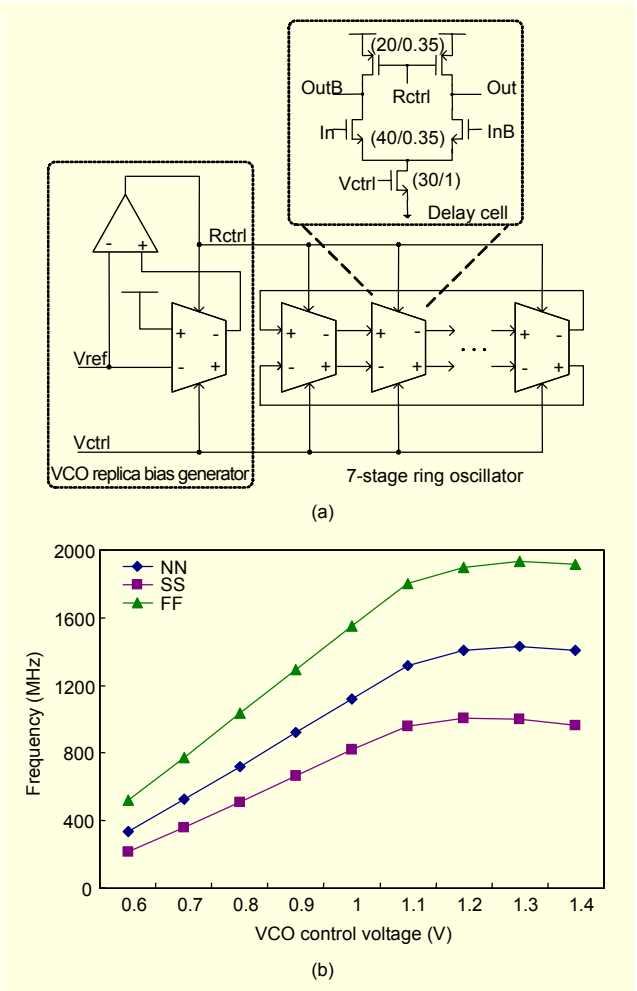


Fig. 10. (a) Voltage-controlled oscillator and (b) its voltage-to-frequency characteristics (NN: V_{DD}=1.8 V, 25°C, normal process corner; SS: V_{DD}=1.6 V, 100°C, slow process corner; and FF: V_{DD}=2.0 V, 0°C, fast process corner).

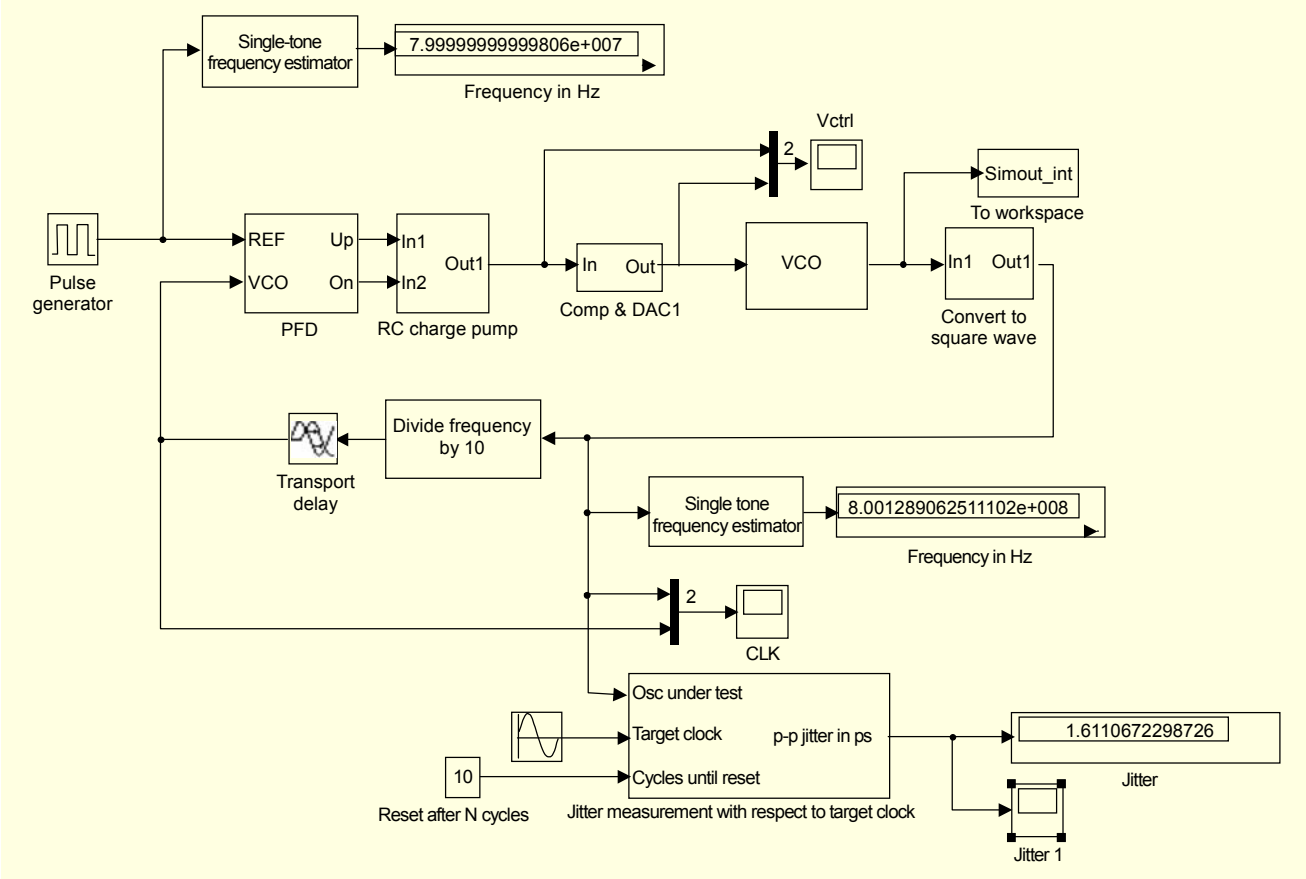


Fig. 11. Simulation setup for behavioral simulation of PLL.

shown in Fig. 9(c), where Φ_1 and Φ_2 are non-overlapping clocks. When Φ_1 is high, the input and output nodes of the pre-amplifier are connected to the reference voltage and the offset is stored on the capacitor. When Φ_2 is high, the offset voltage is cancelled, and only the input differential voltage is amplified. When Φ_{Latch} is LOW, the output nodes of the latch are pre-charged to VDD and when Φ_{Latch} goes to HIGH, the latch senses the output of the pre-amplifier.

The VCO shown in Fig. 10(a) is a fully differential ring oscillator for low sensitivity to common-mode noise. The oscillation frequency can be controlled from 350 MHz to 1.3 GHz at the nominal condition (NN) as shown in Fig. 10(b). The active VCO control voltage range is from 0.6 V to 1.1 V, which can be easily covered by the rail-to-rail input stage of the comparator in Fig. 9(b). The replica bias ensures the constant swing of the output of the VCO [2].

III. Experimental Results

Because the proposed PLL has two feedback loops, it is very difficult to check the stability and determine the loop parameters analytically. Therefore, behavioral simulation has been performed by Matlab with the simulation setup shown in Fig. 11 [8]. From the behavioral simulation results, the bandwidth of the global feedback loop is set to 500 kHz, while the DAC is clocked at a much faster rate of 40 MHz to let the tracking ADC loop have a wider bandwidth. The locking behavior of the PLL is simulated by HSPICE, and the resultant waveforms are shown in Fig. 12. After the loop is locked, the control code of the DAC changes by 1-LSB; thus, the VCO control voltage ripples by about 2 mV, which will result in 20 ps peak-to-peak jitter. The wake-up time of the proposed PLL is smaller than 0.1 μs which is mainly determined by the start-up time for the VCO to begin oscillating while for a conventional analog PLL, the wake-up time would be in the order of several tens of μs.

The PLL has been implemented in a 0.18 μm CMOS process whose microphotograph is shown in Fig. 13, and the active area is 1.0 mm×0.35 mm. The measured rms jitter of the 1.2 GHz output clock is 16.8 ps, while the peak-to-peak jitter is 84 ps as shown in Fig. 14. The peak-to-peak jitter is larger than the value obtained from the behavioral simulation in Fig. 12 because other sources of jitter exist such as the thermal noise of transistors and power supply line noise. From a 1.8 V supply

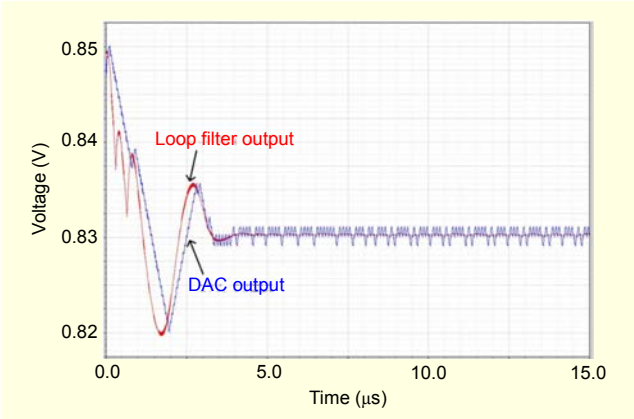


Fig. 12. Simulated locking behavior of PLL.

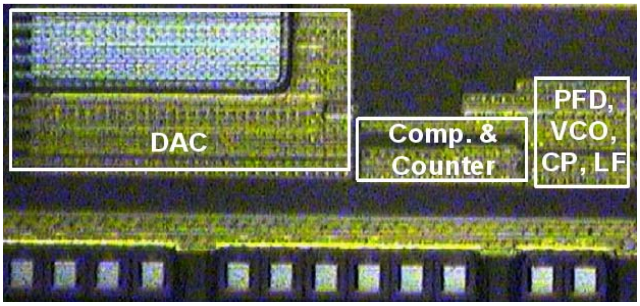


Fig. 13. Microphotograph of PLL.

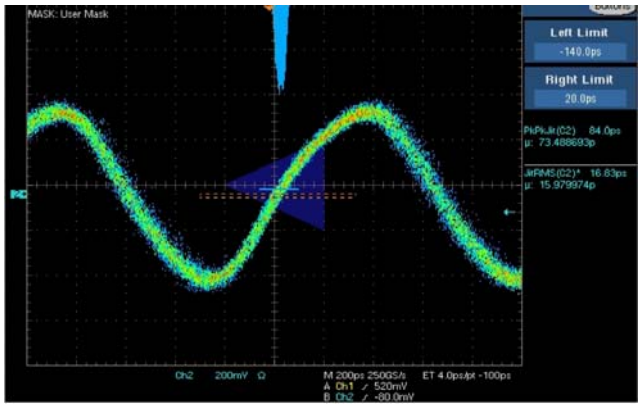


Fig. 14. Measured jitter histogram of 1.2 GHz output clock.

Table 1. Performance summary of PLL.

Technology	0.18 μm 4-metal CMOS
Die area	1.0 mm × 0.35 mm
Supply voltage	1.8 V
Power dissipation	59 mW : normal operation 984 μW : power-down state
Jitter	RMS : 16.8 ps
Locking range	400 MHz – 1.2 GHz

voltage, the PLL consumes 59 mW and 984 μW during the normal operation and power-down mode, respectively. In Table 1, the measured performance of the PLL is summarized.

IV. Conclusion

A 0.4 GHz to 1.2 GHz PLL has been developed which has embedded ADC to store the locking information as digital code. The embedded ADC has 10-bit resolution with tracking architecture, where DAC is in the feedback loop. The DAC employs a glitch minimizing decoding scheme for small jitter. Because the locking information is stored as digital code, the PLL can be turned off during power-down mode, while avoiding long wake-up time.

References

[1] T. Olsson and P. Nilsson, "A Digitally Controlled PLL for Digital SOCs," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, May 2004, pp. 751-760.

[2] S. Kim, K. Lee, Y. Moon, D.-K. Jeong, Y. Choi, and H.-K. Lim, "A 960-Mb/s/pin Interface for Skew-Tolerant Bus Using Low Jitter PLL," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, May 1997, pp. 691-700.

[3] J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, Nov. 1996, pp. 1723-1732.

[4] J. Lin, B. Haroun, T. Foo, J.-S. Wang, B. Helmick, S. Randall, T. Mayhugh, C. Barr, and J. Kirkpatrick, "A PVT Tolerant 0.18 MHz to 600 MHz Self-Calibrated Digital PLL in 90 nm CMOS Process," *Dig. Tech. Papers, Int. Solid-State Circuits Conf.*, Feb. 2004, pp. 488-489.

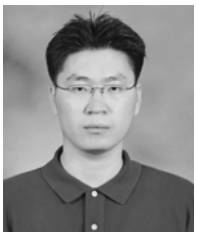
[5] S. Cha, C. Jeong, C. Yoo, and J. Kih, "Digitally Controlled Phase Locked Loop with Tracking Analog-to-Digital Converter," *Proc. IEEE Asian Solid-State Circuits Conf.*, 2005, pp. 377-380.

[6] C.-H. Lin and K. Bult, "A 10-bit, 500 Msample/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, Dec. 1998, pp. 1948-1958.

[7] B. Razavi and B.A. Wooley, "Design Techniques for High-Speed, High-Resolution Comparators," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, Dec. 1992, pp. 1916-1926.

[8] *Matlab Manual*, Mathworks Inc., 2005.

Sooho Cha received the BS and MS degrees in electronics and computer engineering from Hanyang University, Seoul, Korea. He joined the Memory Division of Samsung Electronics as a member of research staff, Hwaseong, Korea, in 2006. His main research interests include mixed-mode CMOS circuit design and high-speed interface circuit design.



Chunseok Jeong received the BS degree in electronics engineering from the University of Seoul, Korea, in 2003, and the MS degree in electronics and computer engineering from Hanyang University, Seoul, Korea, in 2005. He joined the DRAM Design Team of Hynix Semiconductor Inc., Ichon, Korea, where he is involved in the development of 1G DDR3 SDRAM. His research interests include phase-locked loop, delay-locked loop, data converters, and thermal sensors.

Changsik Yoo received the BS (with the highest honor), MS, and PhD degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1992, 1994, and 1998, respectively. From 1998 to 1999, he was with Integrated Systems Laboratory (IIS), Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, as a member of research staff working on CMOS RF circuits. From 1999 to 2002, he was with Samsung Electronics, Hwaseong, Korea. Since 2002, he has been an associate professor of Hanyang University, Seoul, Korea. He is the winner or co-winner of several technical awards including the Samsung Best Paper Bronze Award in the 2006 International SoC Design Conference, the Silver Award in 2006 IDEC Chip Design Contest, the Best Paper Award in the 2006 Silicon RF IC Workshop, and the Golden Prize for research achievement in next generation DRAM design from Samsung Electronics in 2002. His main research interests include CMOS RF transceiver design, mixed mode CMOS circuit design, and high-speed interface circuit design.