An Experimental 0.8 V 256-kbit SRAM Macro with Boosted Cell Array Scheme

Yeonbae Chung and Sang-Won Shim

This work presents a low-voltage static random access memory (SRAM) technique based on a dual-boosted cell array. For each read/write cycle, the wordline and cell power node of selected SRAM cells are boosted into two different voltage levels. This technique enhances the read static noise margin to a sufficient level without an increase in cell size. It also improves the SRAM circuit speed due to an increase in the cell read-out current. A 0.18 µm CMOS 256-kbit SRAM macro is fabricated with the proposed technique, which demonstrates 0.8 V operation with 50 MHz while consuming 65 µW/MHz. It also demonstrates an 87% bit error rate reduction while operating with a 43% higher clock frequency compared with that of conventional SRAM.

Keywords: SRAM, memory, booster, static noise margin.

I. Introduction

As mobile electronic systems become popular, power consumption is a major concern in VLSI chip design. Although various techniques to reduce power dissipation have been developed [1], lowering the supply voltage is most effective. The static random access memory (SRAM) is an important intellectual property block which occupies a large area in a system-on-chip (SoC). However, the performance of SRAM is greatly affected by the operating voltage. The static noise margin (SNM), a measure of SRAM cell stability, deteriorates with reduction of the supply voltage [2] and causes the failure bit rate of the SRAM cell array to increase. Moreover, the SRAM cell current for data detection is reduced, which degrades the operating speed of SRAM.

There have been several attempts to overcome degradation of the operating margin and speed degradation which result from the lowering of the supply voltage [3]-[7]. One conventional technique to counter speed degradation is the wordline (WL) boosting method [3]. With this technique, it is possible to increase the cell read-out current, and thus shorten the bitline delay time. Another technique uses a dual-port cell [4]. This cell separates data storage elements and data output elements. Read operations can be performed without read disturbance. However, the cell is composed of seven or eight transistors, which results in the area overhead incurred by large cell size.

Additionally, in order to improve the cell operating margin, schemes controlling the voltage level of cell power nodes have been reported [5], [6]. In [5], the power of SRAM cells is conveyed from a voltage down-converter which consumes a substantial standby current. In [6], the power of SRAM cells is conveyed from the external pins. Both schemes require multiple external power pins. This is not feasible for the

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implementation of standard SRAM using a single power supply. Furthermore, the voltage levels of cell power nodes cannot be scaled for an optimized balance of cell stability. Another proposed technique is the cell power floating method which is applied during a data write operation [7]. This technique assists the write operation in low-voltage SRAM, but the cell power voltage is effectively lowered to about 50 mV lower than the WL voltage. As the result, the improvement of the write margin is limited to a small amount.

In this work, we propose and demonstrate a dual-boosted cell-based SRAM. For each access, the WL and cell power node of selected SRAM cells are internally boosted into two different voltage levels. With optimization of boosting levels, this technique can enhance both cell stability and the cell read-out current to sufficient levels.

II. Boosted-Cell-Array-Based SRAM

Figure 1 shows a schematic diagram of a 6-T SRAM cell and the proposed bias conditions on the memory cell. Although SRAM cell stability is certainly important during standby mode, the SNM during read operations represents a more significant limitation to SRAM operation [2]. In addition, both read SNM and the cell read-out current value are in an inverse correlation [4].

During the read operation, boosting the WL voltage of selected cells above the supply voltage increases the driving capability of the NMOS access transistor. Thus it increases the cell read-out current (I_{CELL}), resulting in reduced bitline (BL) delay time [3], but the read SNM decreases. To compensate the reduced SNM, a higher voltage than the WL level is applied to the cell power line (CPL), which improves the cell read stability with enlarged SNM. In this work, the WL boosting level (V_{PPWL}) and CPL boosting level (V_{PPCPL}) are chosen to be 1.5 V_{DD} and 2 V_{DD}, respectively. Meanwhile, to achieve a good write operation in low-voltage SRAM, an access transistor with strong driving capability and a relatively weaker pull-up transistor are desired [7]. However, during the write operation, as shown in Fig. 2, only one of interleaved columns is selected for the write operation, while cells from the remaining columns on a selected row will experience a dummy read operation. To achieve the best read and write margin for the cells from a selected row, the same bias conditions are created for the memory cells as for the read operation. Boosting the CPL voltage to 2 V_{DD} increases the read SNM of cells in the dummy read operation but disturbs the write operation of cells in the selected column because the conductance of the PMOS pull-up transistor increases [5]. To resolve this, a boosting voltage of 1.5 V_{DD} is applied to the WL, which improves the driving capability of the access transistor. With the increased driving capability of the access NMOS, the cell internal node with a high data state can be driven closer to the ground through the bitline during a write operation, which makes cells flip easily from one state to another.

Figure 3 shows a memory array configuration based on the proposed dual-boosted cell technique. The WL booster

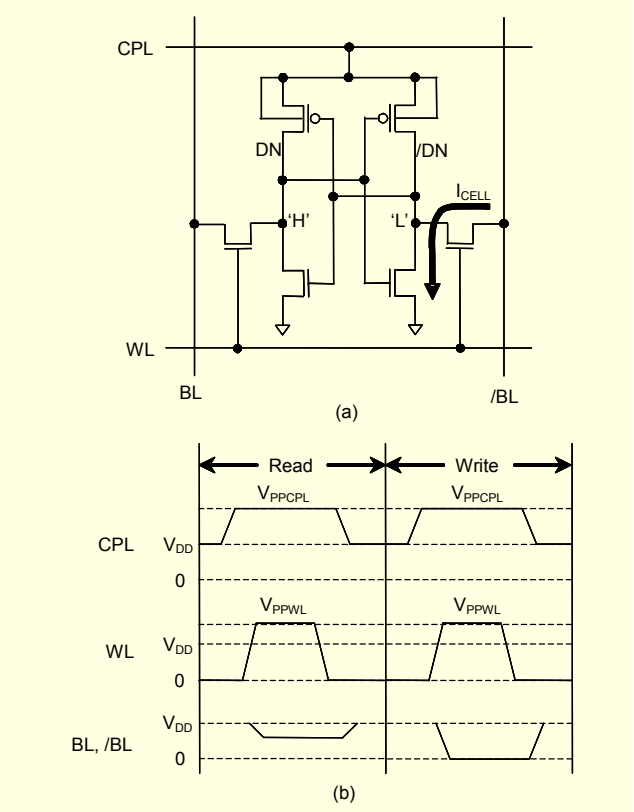

Fig. 1. 6-T SRAM cell: (a) configuration and (b) proposed bias conditions for read/write cycle (DN: data-node, /DN: /data-node).

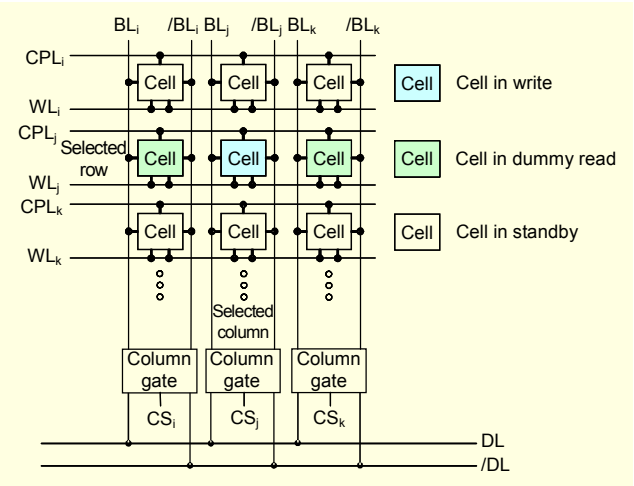

Fig. 2. Status of memory cells in array during write operation (CS: column-select, DL: dataline, /DL: /dataline).

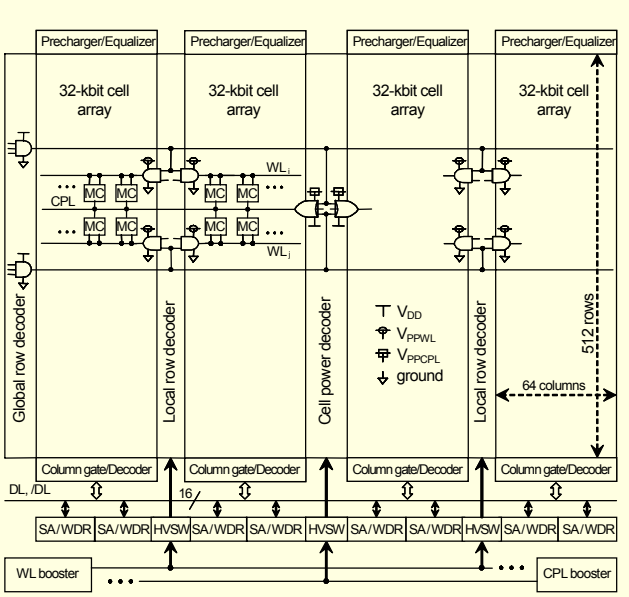

Fig. 3. Configuration of a memory block (MC: memory cell, HVSW: high-voltage switch, SA: sense amplifier, WDR: write driver).

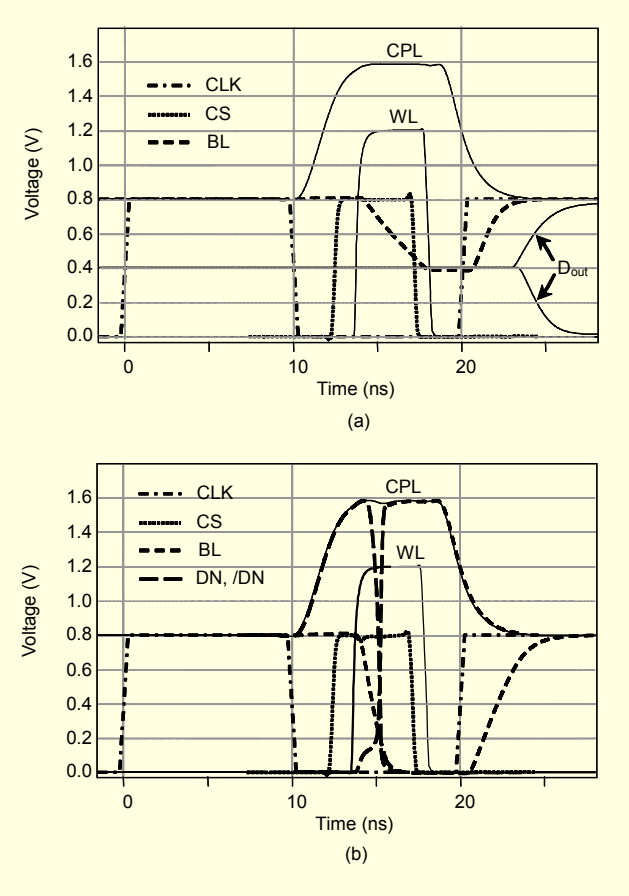

Fig. 4. Simulation waveforms at V_{DD} = 0.8 V and 20 ns cycle: (a) read cycle and (b) write cycle (CLK: clock signal).

Table 1. Features of 0.18 μm CMOS transistors.

Parameters	n-MOSFET	p-MOSFET
Gate oxide thickness (T_{OX})	38 Å	38 Å
Threshold voltage (V_{TH})	0.42 V	-0.48 V
Breakdown voltage (BV_{DSS})	3.6 V	-3.3 V

providing 1.5 V_{DD} is composed of simple circuitry with a boosting capacitor. The CPL booster providing 2 V_{DD} consists of two stages of boosting circuitry which are serially connected by a control switch. The cell array design has been optimized for both boosting performance and area efficiency. One array block has four sub-blocks, each containing 512 rows × 64 columns. Each WL couples 64 cells. Each CPL is shared among two vertical cells and runs parallel to the WL, coupling 256 cells within two adjacent sub-blocks. High-voltage switch (HVSW) decoded by block address supplies the boosting voltage to the selected sub-block. This limits the overall power consumption due to voltage boosting only to a selected sub-block level.

Circuit simulations using 0.18 μm CMOS are shown in Fig. 4. Transistor features are listed in Table 1. The memory cells use the same MOS transistors as the peripheral circuits. At 0.8 V supply, the cycle time is 20 ns for both the read and write cycles. The internally boosted levels of the CPL and WL are 1.6 V and 1.2 V, respectively. During a read operation, the data output is obtained after one clock cycle. The access time is 23 ns. Even though the voltage level of the CPL is 0.4 V higher than that of the WL during a write operation, the write operation is not disturbed by boosting the CPL. The simulation shows that the cell internal nodes (DN, /DN) flip from one state to another in 2 ns after wordline access. Moreover, the maximum voltage which can be applied to the transistors is 1.6 V in this dual-boosting SRAM. Since the level is relatively small compared to the transistor breakdown voltage, it does not affect the reliability of the transistors.

III. Experimental Results

The proposed techniques were implemented in a 256-kbit SRAM, and fabricated with 0.18 μm CMOS process technology. An image of the chip is shown in Fig. 5. The organization is 32k words × 8 bits. The chip size is 1520 μm × 1490 μm = 2.26 mm^2. The area overhead for additional cell power decoders, WL booster, and CPL booster is 5% of the total SRAM area.

Figure 6 shows the relation between V_{DD} and cycle time. The SRAM achieves a 50 MHz operating frequency at a 0.8 V

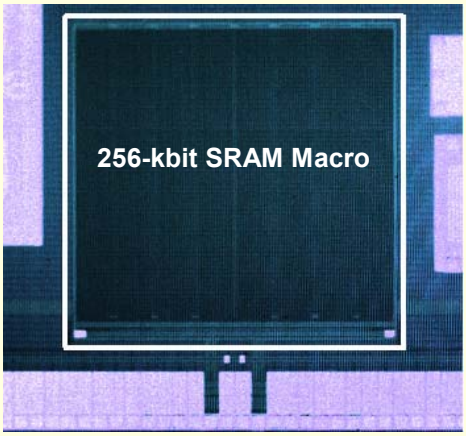

Fig. 5. Chip microphotograph.

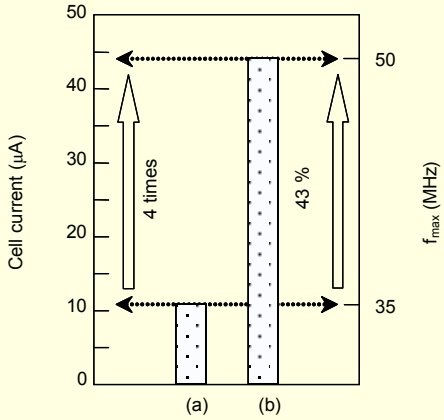

Fig. 8. Measured cell read-out current at V_{DD} = 0.8 V: (a) without cell boosting and (b) V_{PPWL} = 1.2 V and V_{PPCPL} = 1.6 V.

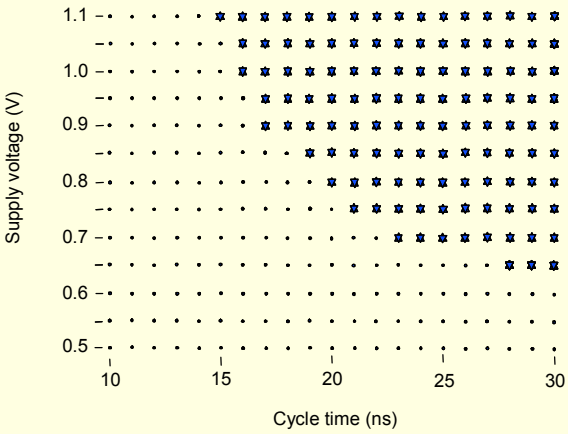

Fig. 6. Shmoo plot.

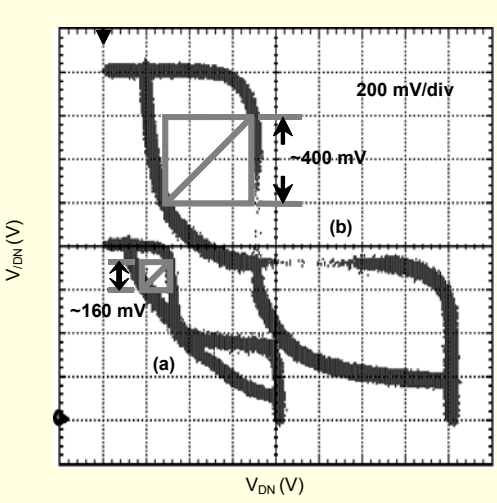

Fig. 7. Measured butterfly curves at V_{DD} = 0.8 V: (a) without cell boosting and (b) V_{PPWL} = 1.2 V and V_{PPCPL} = 1.6 V.

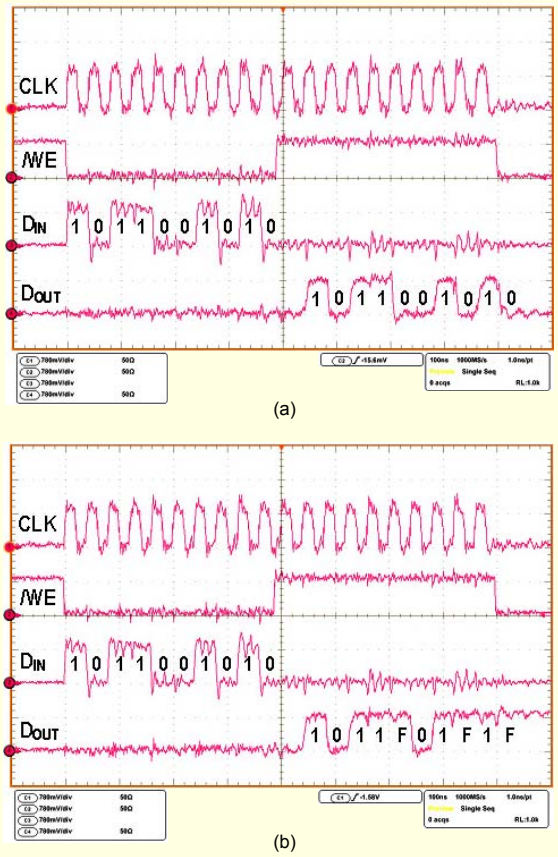

Fig. 9. Measured waveforms at V_{DD} = 0.8 V and 40 ns clock cycle: (a) with cell boosting of V_{PPWL} = 1.2 V, V_{PPCPL} = 1.6 V and (b) without cell boosting (voltage: 780 mV/div, time: 100 ns/div, F: fail-bit).

power supply. The active power dissipation is 65 μW/MHz. According to the experiment, this is 26% higher than the active power dissipation of the conventional scheme in which the SRAM cells are not boosted.

Figure 7 shows the measured butterfly curves. At a supply voltage of 0.8 V, the read SNM is found to be around 160 mV in a conventional cell without boosting. By boosting the voltage level of the WL and CPL to 1.2 V and 1.6 V, respectively, the read SNM is drastically increased to approximately 400 mV. It also increases the cell read-out current about four times as shown in Fig. 8. Improvement in the maximum operating frequency is 43% due to the increase in the read cell current. This was confirmed by circuit simulation.

The primary benefit of the proposed technique is to reduce the bit failure associated with read and write margins. Figure 9 shows the measured waveforms for both the proposed and conventional SRAMs. The chips have separated input and output pads. The input data series "1011001010" is written into the SRAM chip when the /WE signal is low. Then, the output data series "1011001010" is read when the /WE signal is high. In this test, the output data matches the input for the proposed SRAM; however, the conventional SRAM, operating without cell boosting, displays some fail bits during the read cycles. We also fully tested the functionality of the SRAM with a March sequence including write 0, read 0, write 1, and read 1. As shown in Fig. 10, a bit-failure reduction of about 87% has been achieved by dual cell boosting.

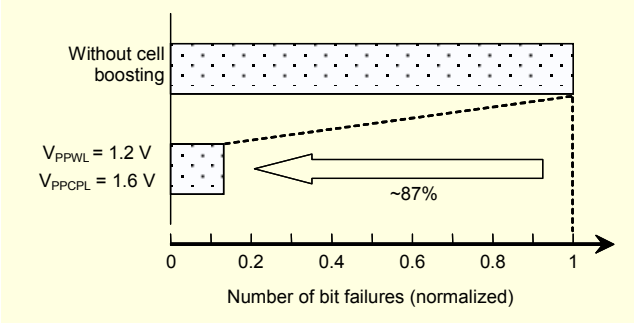

Fig. 10. Bit failure rate at V_{DD} = 0.8 V.

IV. Conclusion

In order to improve the cell stability and the SRAM circuit speed associated with low-voltage SRAM, we have proposed a dual-boosted cell-array technique which can enhance both the cell SNM and the cell read-out current. For each access at the 0.8 V supply, the wordline and cell power node of selected SRAM cells are internally boosted to 1.2 V and 1.6 V, respectively. A 256-kbit SRAM test chip designed according to the proposed scheme was fabricated in a 0.18 μm CMOS process. At a 0.8 V supply voltage, it demonstrated a 50 MHz operation while consuming a power of 65 μW/MHz, a 400 mV read SNM, and a 44 μA cell current. The bit error rate was reduced by 87% and the chip operating frequency was 43% higher compared with that of conventional SRAM. Since the memory chip yield is often determined by the failure rate of memory cells, the proposed technique will be able to provide a significant improvement in the manufacturing die yield.

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