A CMOS Frequency Synthesizer Block for MB-OFDM UWB Systems

Chang-Wan Kim, Sang-Sung Choi, and Sang-Gug Lee

A CMOS frequency synthesizer block for multi-band orthogonal frequency division multiplexing ultra-wideband systems is proposed. The proposed frequency synthesizer adopts a double-conversion architecture for simplicity and to mitigate spur suppression requirements for out-of-band interferers in 2.4 and 5 GHz bands. Moreover, the frequency synthesizer can consist of the fewest nonlinear components, such as divide-by-Ns and a mixer with the proposed frequency plan, leading to the generation of less spurs. To evaluate the feasibility of the proposed idea, the frequency synthesizer block is implemented in 0.18-μm CMOS technology. The measured sideband suppression ratio is about 32 dBc, and the phase noise is -105 dBc/Hz at an offset of 1 MHz. The fabricated chip consumes 17.6 mA from a 1.8 V supply, and the die-area including pads is 0.9 × 1.1 mm^2.

Keywords: Frequency synthesizer, UWB, ultra-wideband, mixer, divide-by N, MB-OFDM, CMOS, RFIC.

I. Introduction

Recently, interest in ultra-wideband (UWB) systems for short-range and high-data-rate wireless communications has significantly increased. The IEEE 802.15 high rate alternative PHY task group (TG3a) is considering direct-sequence code-division multiple-access (DS-CDMA) and multi-band orthogonal frequency division multiplexing (MB-OFDM) as candidates for an international standard for approach for wireless personal area networks (WPAN) [1]. The MB-OFDM approach, as can be seen in Fig. 1, divides the full 7.5 GHz UWB band (3.1 to 10.6 GHz) into 14 sub-bands with a bandwidth of 528 MHz. In particular, the lower three bands (3,432 MHz, 3,960 MHz, and 4,488 MHz) are allocated for first generation devices (mode 1, or mandatory mode) for MB-OFDM UWB systems. Mandatory devices could be more easily developed with current CMOS technology than devices which support the 7.5 GHz full-UWB band, considering the design of wideband RF/analog circuits, the high-speed analog-to-digital converter (ADC), and so on. Moreover, with this frequency plan, MB-OFDM UWB shows good flexibility for the frequency regulations of different countries and can co-exist with 802.11a/b/g wireless systems, which use frequency bands very near UWB bands. However, the frequency synthesizers for MB-OFDM UWB must provide multiple local oscillator (LO)

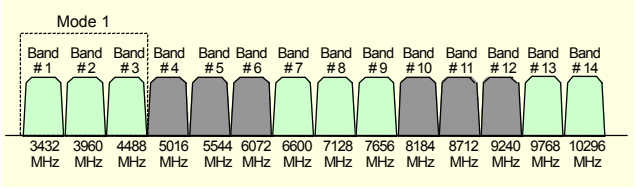

Fig. 1. Frequency plan of MB-OFDM UWB systems.

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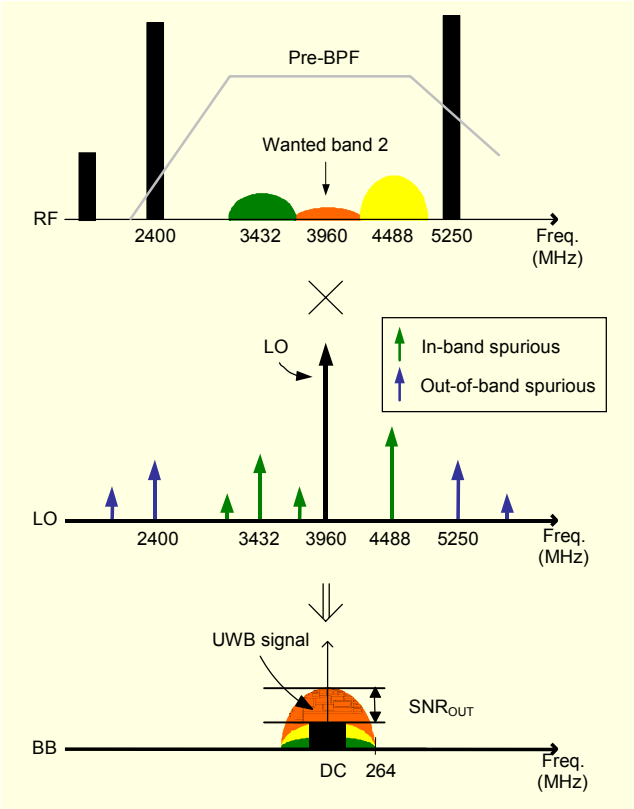


Fig. 2. Mixing mechanism between interferers and spurs in the direct-conversion MB-OFDM UWB systems.

tones for up/down-conversion of each RF sub-band with a very fast switching time of less than 9.5 ns.

Recently, many frequency synthesizers for direct-conversion UWB systems have been reported [2]-[7], which are implemented using CMOS technology. To generate multi-LO tones from one or two phase-locked loops (PLLs), single-side-band (SSB) mixers and divide-by-Ns are used in one approach [2]-[6]. One major technical issue in this scheme is unwanted spur tones generated by non-linear components, such as divide-by-Ns and SSB mixers. The approach in [7] uses three PLLs to provide three LO tones, where each voltage controlled oscillator (VCO) oscillates at three different LO frequencies, respectively. For both the above approaches [2]-[7], the sideband suppression requirement is very strict due to its wideband characteristics.

Figure 2 shows details of the mixing mechanism between spurs from the synthesizer and RF interferers (in- and out-of-band) in the direct-conversion UWB receiver. As shown in Fig. 2, while receiving weak band 2, the direct-conversion UWB receivers suffer from both in-band interferers (bands 1 and 3) transmitted by other UWB devices, and strong out-of-band RF interferers at 2.4 and 5 GHz bands, which are not sufficiently suppressed by a pre-bandpass filter (BPF). All these unwanted RF interferers can saturate the receiver chain, degrading its gain and noise characteristics. In addition, as can be seen in Fig. 2,

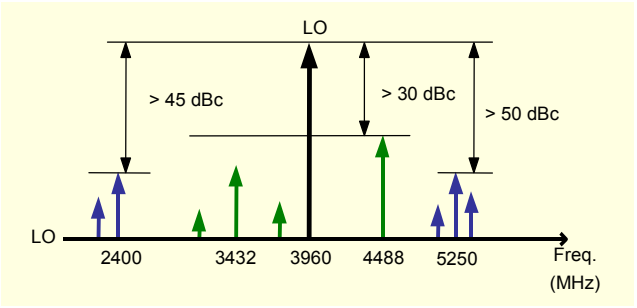


Fig. 3. Spur suppression requirements of the direct-conversion architecture.

they can corrupt the wanted baseband UWB signals by mixing operation with spurs generated from the synthesizer, degrading signal-to-noise ratio (SNR) at the output of the receiver. Here, note that this problem is very similar to the image problems [8] in the general heterodyne receivers. Accordingly, to prevent these unwanted mixing problems, all unwanted RF interferers and spur tones from the synthesizer must be sufficiently suppressed. In the case of RF interferers, they are in-band and out-of-band signals very near the UWB bands; therefore, it is hard to attenuate them due to the limitation of filtering at high frequency. Accordingly, suppressing the spurs from the frequency synthesizer can be a preferred approach. Spur suppression requirements in the direct-conversion MB-OFDM UWB frequency synthesizers are highly recommended in [9]. As can be seen in Fig. 3, the in-band sideband suppression ratio must be more than 30 dBc. For interferers in 2.4 and 5 GHz frequency bands, the spurs in 2.4 and 5 GHz frequency bands must also be 45 dB and 50 dB lower than the wanted LO tone, respectively. The above requirements are very important and strict factors, but it is not easy to achieve that suppression ratio in the silicon implementation.

To satisfy the sideband suppression requirements in [9], the proposed frequency synthesizer adopts both a double-conversion architecture and the proposed frequency plan. The proposed frequency synthesizer can consist of the fewest nonlinear components with the proposed frequency plan, leading to the generation of less spurs when multi-LO tones are synthesized. In particular, the spur suppression for out-of-band interferers in 2.4 GHz and 5 GHz bands can be considerably improved.

II. Proposed Frequency Plan

MB-OFDM UWB transceivers can be implemented as the direct-conversion [2], [4], [7] or heterodyne architecture [10]. The direct-conversion architecture for MB-OFDM UWB systems can remove off-chip IF filters due to the absence of image problems; therefore, all circuit blocks can be intensively

integrated on the silicon chip. However, the direct-conversion UWB receivers experience mixing problems between in- and out-of band RF interferers and spurs from the frequency synthesizer, as discussed in section I. In addition, inherent problems (DC offset, I/Q mismatch, and so on) in direct-conversion receivers must be solved even under the fast hopping condition in MB-OFDM UWB systems. On the other hand, the MB-OFDM UWB transceiver based on the heterodyne architecture can overcome the disadvantages of the direct-conversion architecture at the cost of the adoption of additional function blocks (the image-rejection filter and IF mixers). Moreover, the frequency synthesizer for the heterodyne architecture does not need to provide quadrature but differential multi-LO tones, showing a high possibility of simple architecture and low DC power consumption. However, to take advantage of the heterodyne architecture, a careful frequency plan is required which takes into consideration image problems and the architecture of the synthesizer.

Figure 4 shows the proposed double-conversion architecture for the MB-OFDM UWB receiver, which is focused on the mandatory mode (frequency bands: 3,432, 3,960, and 4,488 MHz). As can be seen in Fig. 4, incoming RF signals (3,432, 3,960, and 4,488 MHz) from the UWB antenna are first downconverted by the RF mixer to the fixed IF of 1,320 MHz, and then downconverted to DC. Image signals are suppressed by both a pre-BPF and image rejection filter.

Table 1 shows the proposed frequency plan for the double-conversion receiver in Fig. 4. The IF frequency of 1,320 MHz was carefully chosen in this work, considering both image problems in the receiver and the number of nonlinear components in the frequency synthesizer.

In the proposed frequency plan, all image frequency bands (from 528 to 2,112 MHz) for LO_1 (2,112, 2,640, and 3,168 MHz) can be located out-of-band and considerably suppressed only by the pre-BPF. However, because image band 3 (centered at 1,848 MHz) contains Global System for Mobile Communication (GSM) 1,800 (1,710 to 1,795 MHz) and GSM 1,900 (1,850 to 1,910 MHz) transmitter frequencies, these strong GSM signals must be further suppressed by the image rejection filter before the first down conversion. When GSM devices are far away from the double-conversion UWB

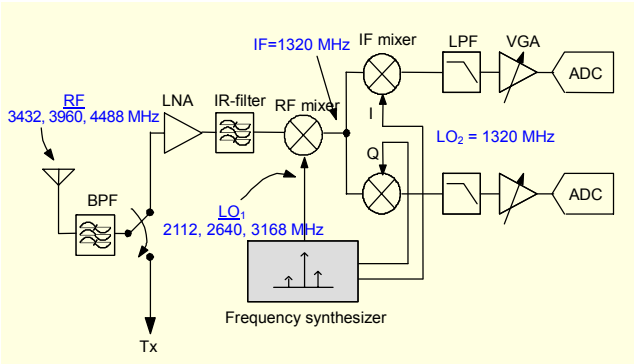


Fig. 4. Proposed double-conversion receiver for the MB-OFDM UWB radio.

Table 1. Proposed frequency plan.

(MHz)

	RF freq.		LO freq.	IF freq.	Image freq.
Band 1	Lower freq.	3,168	2,112	1,056	1,056
	Center freq.	3,432		1,320	792
	Upper freq.	3,696		1,584	528
Band 2	Lower freq.	3,696	2,640	1,056	1,584
	Center freq.	3,960		1,320	1,320
	Upper freq.	4,224		1,584	1,056
Band 3	Lower freq.	4,224	3,168	1,056	2,112
	Center freq.	4,488		1,320	1,848
	Upper freq.	4,752		1,584	1,584

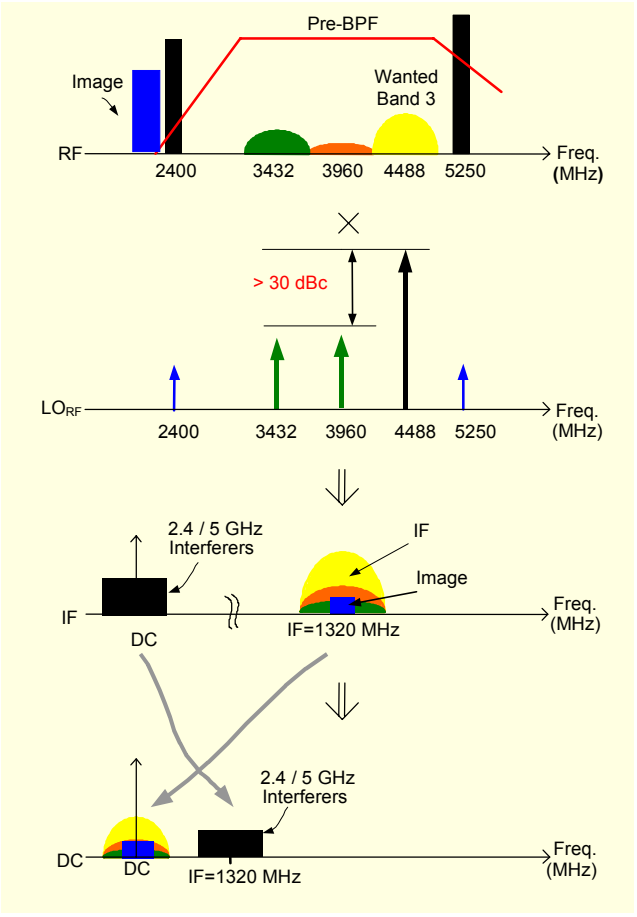


Fig. 5. Mixing mechanism between spurs and interferers in the double-conversion MB-OFDM UWB frequency synthesizers.

devices, image problems for band 3 can be further alleviated.

In terms of the architecture of the frequency synthesizer, with the IF of 1,320 MHz, multi-LO tones of LO_1 and LO_2 can be synthesized from only one VCO with the fewest nonlinear components, as can be seen in Fig. 6. The adoption of fewer nonlinear circuits in the synthesizer reduces the generation of unwanted spurs, leading to a smaller burden of sideband suppression requirements [9].

Figure 5 shows the mixing mechanism between RF interferers and spurs in the proposed double-conversion MB-OFDM UWB receiver. Note that the suppression requirements of RF interferers in 2.4 GHz and 5 GHz frequency bands are considerably mitigated in the double-conversion architecture. The RF interferers in 2.4 and 5 GHz bands are first downconverted at or near the DC and mixed with spurs at 5 and 2.4 GHz bands from the synthesizer, respectively. Then, they are finally upconverted into frequency bands over 500 MHz by the second mixing operation with an LO_2 of 1,320 MHz, not corrupting wanted UWB signals which are finally located from the DC to 264 MHz. Accordingly, only the in-band sideband suppression requirement [9] is an import factor in the proposed double-conversion frequency synthesizer.

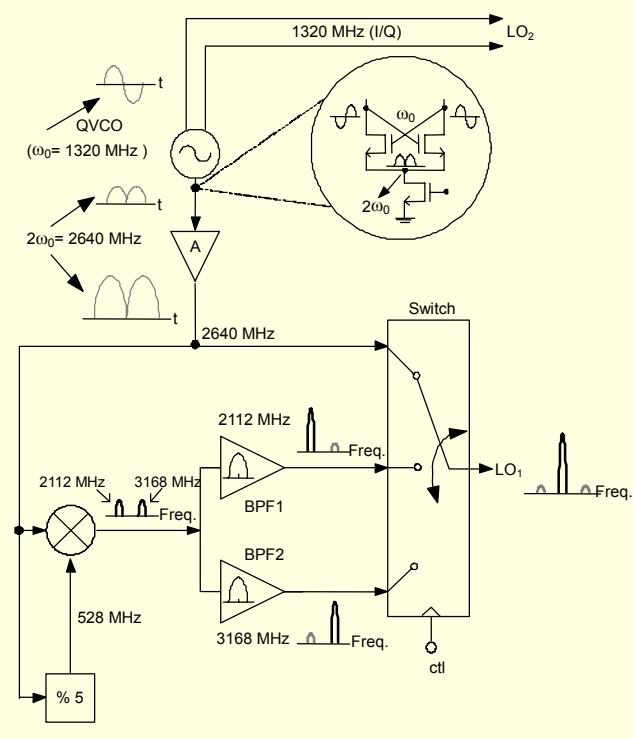


Fig. 6. Simplified block diagram of the proposed frequency synthesizer.

III. Proposed Frequency Synthesizer

The block diagram of the proposed frequency synthesizer for the double-conversion UWB receiver is shown in Fig. 6. It consists of a quadrature VCO (QVCO), an amplifier, a passive mixer, a divide-by-five, two BPFs, and a switch. Note that the block diagram in Fig. 6 is only one example of an architecture that can be generated from the frequency plan in Table 1. In Fig. 6, LO_1 signals (2,112, 2,640, and 3,168 MHz) are oriented from the second-order harmonic component (2,640 MHz) at the common-source node of the 1,320 MHz QVCO. The second-order harmonic signal of 2,640 MHz of the QVCO is amplified and directly applied to the input of the switch circuit. The 2,112 MHz and 3,168 MHz signals are synthesized by mixing 2,640 MHz with 528 MHz generated from the divide-by-five. The synthesized 2,112 and 3,168 MHz signals at the output of the passive mixer are simultaneously filtered and amplified by BPF 1 and BPF 2, respectively. BPF 1 and BPF 2 are two-stage differential pairs with LC-tank loads, and the center frequency of BPF 1(2) is 2,112 MHz (3,168 MHz). The 1 GHz distance between 2,112 and 3,168 MHz permits the adoption of LC-BPFs in this work. The sideband suppression between the 2,112 MHz and 3,168 MHz signals strongly depends on the quality factor (Q) and deviation from the center frequency of the on-chip BPFs 1 and 2, respectively. To minimize the effect of varying center frequencies of the on-chip band pass filters, high Q on-chip spiral inductors are

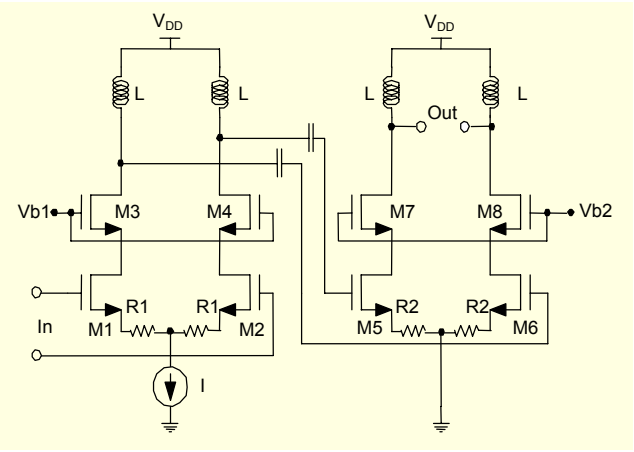


Fig. 7. Schematic of the two-stage BPF1 centered at 2,112 MHz.

carefully modeled. Moreover, to suppress inductive coupling problems between the two on-chip BPFs, they are separated and laid out in opposite directions, as shown in Fig. 11. Finally, one of the LO_1 signals is selected by the switch circuit and provided to the gate nodes of the switching transistors of the RF mixer. The quadrature LO_2 of 1,320 MHz for the quadrature IF mixer is directly provided by the output of the QVCO.

Figure 7 shows a simplified schematic of the on-chip BPF 1 centered at 2,112 MHz, which is a two-stage differential pair with LC-tank loads. With the exception of load inductance values BPF 2 is the same as BPF 1. For input signals at 2,112

and 3,168 MHz generated from a passive mixer, BPF 1 gives high impedance for 2,112 MHz but lower impedance for the 3,168 MHz input signal. As shown in Fig. 7, to provide undistorted output voltage swing for the RF mixer, differential pairs adopt the resistive degeneration technique, and the common-source node of the second-stage amplifier is directly connected to the ground. The quality factor of the on-chip spiral inductor used in BPF 1 is about 12 at 2 GHz. Cascoded transistors (M_3, M_4, M_7, and M_8) are used to improve isolation between the input and output of BPF 1.

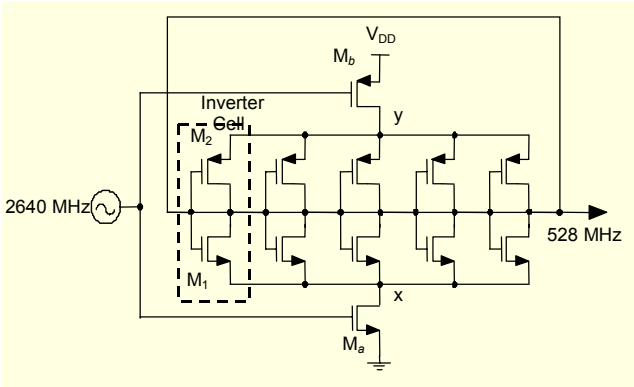


Fig. 8. Schematic of the divide-by-five circuit.

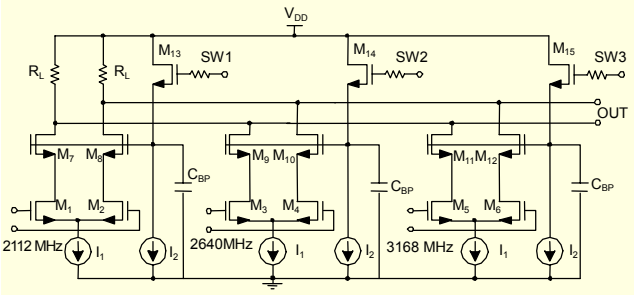


Fig. 9. Proposed switch circuit.

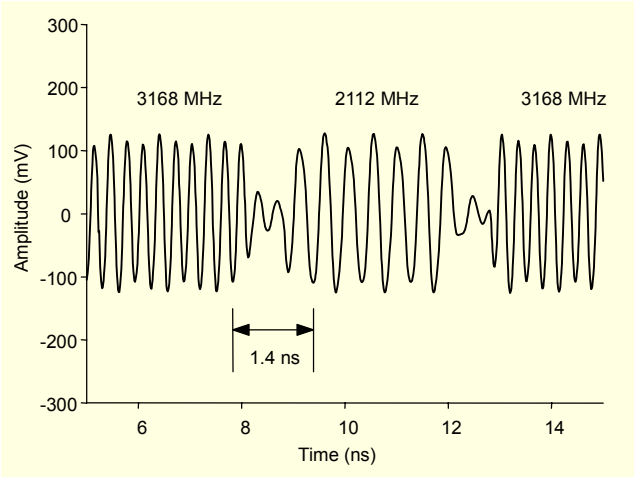


Fig. 10. Band-switching behavior.

Figure 8 shows the divide-by-five circuit, modified from [11], which is a ring-oscillator-based injection-locked frequency divider (ILFD). This ILFD, which consists of five inverter-based (M_1 and M_2) delay cells, consumes less DC power and chip area compared to other dividers using the LC- tank circuit. To increase injection efficiency, the 2,640 MHz signal from the QVCO is simultaneously injected into nodes X and Y through the current sources M_a and M_b.

Figure 9 shows a simplified schematic of the proposed switch circuit, which selects one of three LO_1 tones (2,112, 2640, and 3,168 MHz) by turning on the switch transistors M_{13}, M_{14}, and M_{15}, respectively. In Fig. 9, the three cascoded differential pairs are connected in parallel to the common resistive load, R_L, and all gate nodes of cascode transistors M_7-M_8, M_9-M_{10}, and M_{11}-M_{12} are connected to the source nodes of switch transistors M_{13}, M_{14}, and M_{15}, respectively, for the LO selection. When one of the differential pairs turns on and the others turn off, the cascode topology improves LO isolation among the three output signals. The proposed multiplexer uses resistive load R_L to save the silicon-chip area. Under 1.8 V voltage, the small cascoded transistors M_7-M_{12} (50/0.18 μm) and restive load R_L (200 ohm) provide enough voltage gain up to the frequency range of 3.3 GHz. The simulated band-switching behavior from band 3 (3,168 MHz) to band 1 (2,112 MHz) is shown in Fig. 10. The simulated settling time is less than 1.4 ns, which is below the maximum of 9.5 ns.

IV. Measurement Results

The proposed frequency synthesizer is implemented in 0.18 μm CMOS technology. It consumes 17.6 mA from a 1.8 V supply voltage. Its chip micrographic image is shown in Fig. 11. The die area with pads is 0.9×1.1 mm^2. In Fig. 6, a divide-by-five, a passive mixer, a switch circuit, and two LC-BPFs are

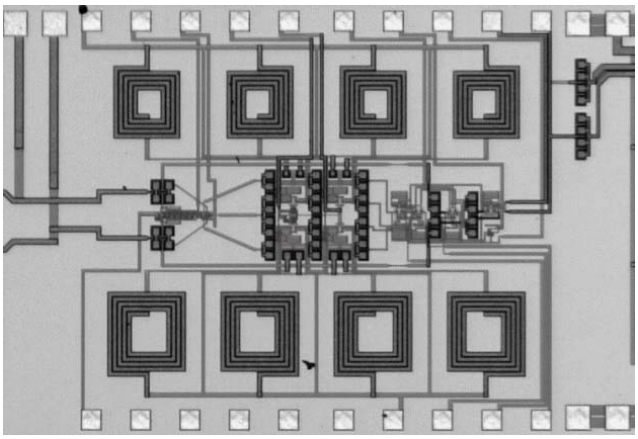
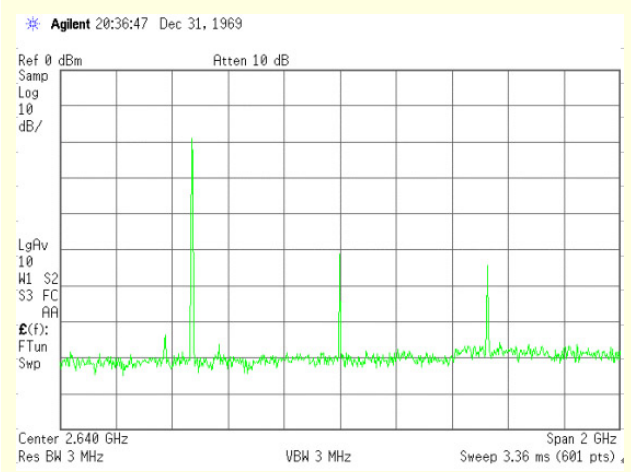
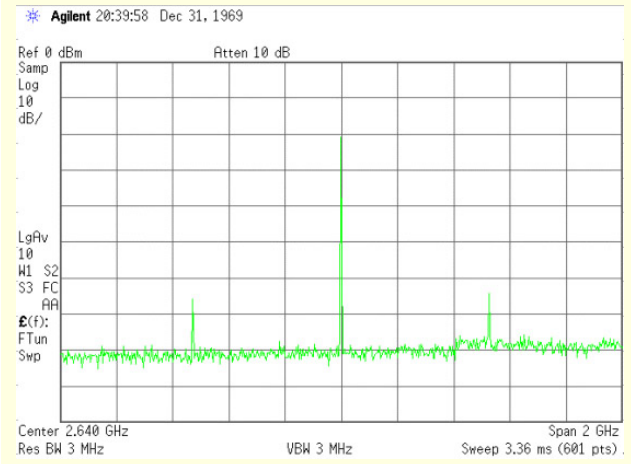


Fig. 11. Photograph of the proposed frequency synthesizer block.



(a)



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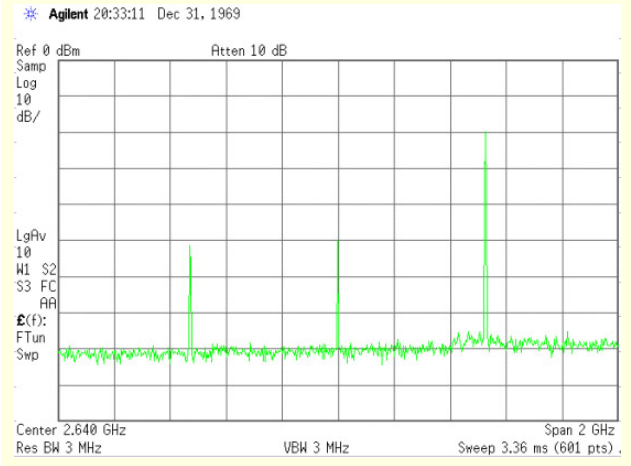

(c)

Fig. 12. Output spectrum of the frequency synthesizer: (a) band 1 (2,112 MHz), (b) band 2 (2,640 MHz), and (c) band 3 (3,168 MHz).

integrated in this work to evaluate the feasibility of the frequency synthesizer. The 1,320 MHz QVCO is separately implemented and is not included in this work. The 2,640 MHz

Fig. 13. Spectrum of band 2 (2,640 MHz) over 1.5 to 6 GHz.

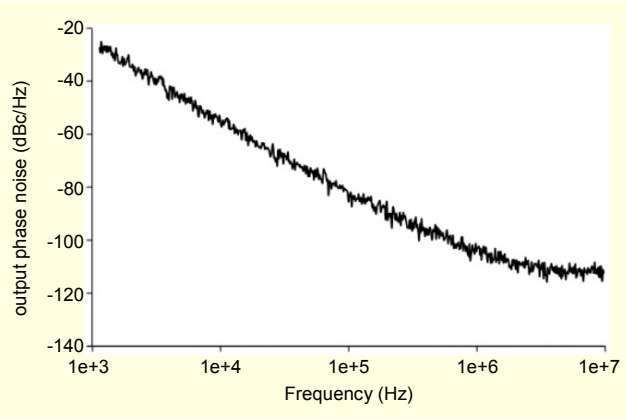

Fig. 14. Measured output phase noise of band 3.

signal is externally provided by the separate 1,320 MHz QVCO.

Figure 12 shows measured output spectra from the frequency synthesizer for LO_1 tones of 2,112, 2,640, and 3,168 MHz, respectively. The measured in-band sideband suppression ratio is 32 dBc for 2,112 and 3,168 MHz LO tones and 43 dBc for 2,640 MHz. These measured values more than satisfy the MB-OFDM UWB requirements [9]. This spur suppression ratio comes from the isolation between two on-chip BPFs, the isolation characteristics of the switch, and having few nonlinear components. However, as can be seen in Fig. 12, the measured output power level is relatively low, which is due to process variation, FR4 PCB loss, cable loss, and so on. For our future transceiver implementation, an LO buffer amplifier will be added for higher voltage swing. Figure 13 shows the spectrum of a 2,640 MHz LO tone over a 1.5 to 6 GHz frequency range. Unwanted out-of-band spurs are also below 35 dB compared to a 2,640 MHz signal and their leakages to the antenna do not affect other wireless systems like 2.4/5 GHz WLAN systems

Table 2. Performance Comparison of various frequency synthesizers.

	This work	[2]	[4]	[5]	[6]	[7]
Bands	3	3	3	7	3	3
Sideband suppression (in-band)	32 dBc	36 dBc	37 dBc	N/A	20 dBc	40 dBc[4)]
Phase noise (@ l-MHz offset)	-105 dBc/Hz	-117 dBc/Hz	1.9 deg RMS	-103 dBc/Hz	N/A	-106 dBc/Hz
Switching time	1.4 ns[1)]	5 ns	2 ns	1 ns	N/A	N/A
Chip area	0.9×1.1 mm^2	N/A	N/A	1.3×1.1 mm^2	0.8×0.85[3)]	N/A
Supply voltage	1.8 V	1.8 V	1.5 V	2.2 V	1.8 V	1.5 V
DC power	31.7 mW[2)]	N/A	186 mW	48 mW	54 mW[2)]	45 mW
Technology	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS

1) Simulated switching time, 2) Not include PLLs, 3) Core area, 4) When all PLLs are turned on

because they are more suppressed by the pre-BPFs. The measured output phase noise of band 3 (3,168 MHz) can be seen in Fig. 14, which is -105 dBc/Hz at 1 MHz offset. Table 2 summarizes the measured performance of the proposed frequency synthesizer block as compared to other previous works. As the results in Table 2 demonstrate, the proposed frequency synthesizer satisfies the MB-OFDM in-band spur suppression requirements (more than 30 dBc) with lower DC power consumption than other previous works. This is because it adopts few nonlinear components, such as divide-by-Ns and mixers in accordance with the proposed frequency plan. Finally, the proposed frequency synthesizer provides a new low-power design solution which generates less spurs for the MB-OFDM UWB transceivers.

V. Conclusion

A frequency synthesizer for MB-OFDM UWB systems was proposed, and was implemented in 0.18 μm CMOS technology. With the proposed frequency plan based on a double-conversion architecture, the low-power frequency synthesizer can be simply implemented with few nonlinear components. Its measured spur suppression ratio is more than 32 dBc and the phase noise is -105 dBc/Hz at an offset of 1 MHz. It consumes 17.4 mA from a 1.8 V supply.

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