A 3.1 to 5 GHz CMOS Transceiver for DS-UWB Systems

Bonghyuk Park, Kyung Ai Lee, Songcheol Hong, and Sangsung Choi

This paper presents a direct-conversion CMOS transceiver for fully digital DS-UWB systems. The transceiver includes all of the radio building blocks, such as a T/R switch, a low noise amplifier, an I/Q demodulator, a low pass filter, a variable gain amplifier as a receiver, the same receiver blocks as a transmitter including a phase-locked loop (PLL), and a voltage controlled oscillator (VCO). A single-ended-to-differential converter is implemented in the down-conversion mixer and a differential-to-single-ended converter is implemented in the driver amplifier stage. The chip is fabricated on a 9.0 mm^2 die using standard 0.18 μm CMOS technology and a 64-pin MicroLead Frame package. Experimental results show the total current consumption is 143 mA including the PLL and VCO. The chip has a 3.5 dB receiver gain flatness at the 660 MHz bandwidth. These results indicate that the architecture and circuits are adaptable to the implementation of a wideband, low-power, and high-speed wireless personal area network.

Keywords: DS-UWB, transceiver, LNA, mixer, VGA, LPF, PLL, CMOS.

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Bonghyuk Park (phone: + 82 42 860 1267, email: bhpark@etri.re.kr) and Sangsung Choi (email: sschoi@etri.re.kr) are with Digital Home Research Division, ETRI, Daejeon, S. Korea.

Kyung Ai Lee (email: kalee@eeinfo.kaist.ac.kr) and Songcheol Hong (email: schong@ee.kaist.ac.kr) are with the Department of Electrical Engineering, KAIST, Daejeon, S. Korea.

I. Introduction

High-data-rate wireless transceivers for wireless personal area networks (WPANs), such as ultra-wideband (UWB) have been developed [1]-[5], Recently, a number of them have become commercialized. Currently, there are two main approaches in IEEE 802.15.3a which support these features: direct-sequence code division multiple access (DS-CDMA) UWB and multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB. Both approaches use a lower frequency band of 3.1 to 5 GHz as a mandatory mode.

A 3.1 to 5 GHz CMOS UWB RF transceiver is presented in this paper. It is based on a DS-CDMA method as described in [6]. For the analog/digital system on a chip, the proposed RF transceiver is implemented using CMOS technology. It adopts direct-conversion architecture and includes all of the RF analog building blocks. Section II introduces the transceiver architecture in DS-UWB radio, and section III describes the design of the building blocks. Experimental results of the fabricated chip are reported in section IV, and the paper concludes in section V.

II. Transceiver Architecture

The overall block diagram of the DS-UWB RF transceiver, including an RF transmitter, a receiver, and a frequency synthesizer, is shown in Fig. 1. Direct-conversion is usually preferred due to its low cost and full integration, as it does not require any external filters. However, direct-conversion architecture suffers from inherent drawbacks, such as a DC-offset, I/Q mismatch, and so on [7]. A high-pass filter composed of 20 to 30 pF DC blocking capacitors is used in the receiver in order to overcome the DC-offset problems. On the

transmit side, a single path is implemented because the baseband modem uses binary phase-shift keying (BPSK) modulation, but the I and Q paths are used on the receiver side in order to compensate for the wireless channel phase difference. The UWB driver amplifier (DA) is merged with a differential-to-single-ended converter and a wideband output-matching network, which are included in the transmitter. A single-ended-to-differential converter is applied in the down-mixer block. A 4 GHz frequency synthesizer is implemented for local signal generation, and a 3-stage poly-phase filter is used for I/Q generation. In [6], for a packet error rate of less than 8%, the minimum receiver sensitivity number at a 220 Mbps rate is -76.5 dBm, the required E_b/N_o is 2.4 dB, and the channel bandwidth is 1.32 GHz. Therefore, the required receiver noise figure is 11.7 dB at 220 Mbps from (1) [1].

$$NF = Sensitivity - SNR + 174 \text{ dBm} - 10\log B, \qquad (1)$$

where *SNR* is the required SNR at the modem receiver, and *B* is the channel bandwidth.

The link margin is 6 dB including an implementation loss of 4 dB in a 4 m transmitter-receiver distance, and the maximum transmission power is -9.9 dBm without considering the I/Q gain, phase mismatch, and phase noise of the local signal.

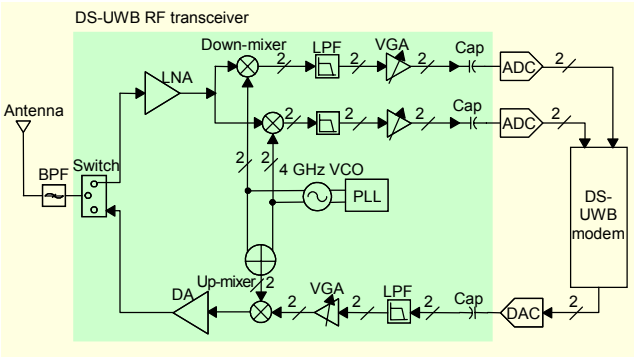

Fig. 1. RF transceiver chip block diagram.

III. Circuit Implementation

1. RF Front-End Receiver

The RF front-end receiver in the transceiver integrated circuit consists of a Tx/Rx selection switch, a low-noise amplifier (LNA), and a double-balanced mixer. Since the DS-UWB system communicates using a time division duplexing method, it needs the Tx/Rx selection switch for choosing the Tx and Rx modes. A Tx/Rx selection switch architecture is shown in Fig. 2. The switch has four transistors. A transmitter path works during the on state of series transistor M1 and a parallel transistor

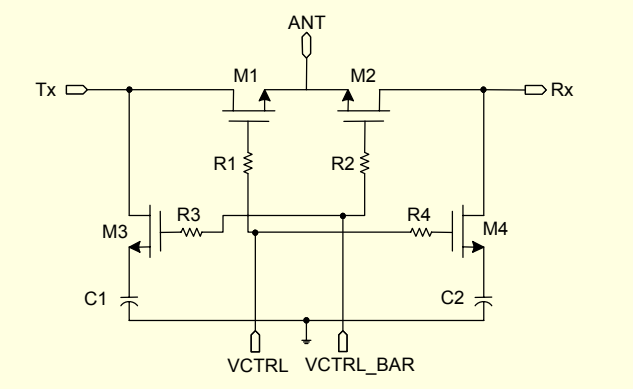

Fig. 2. Tx/Rx selection switch.

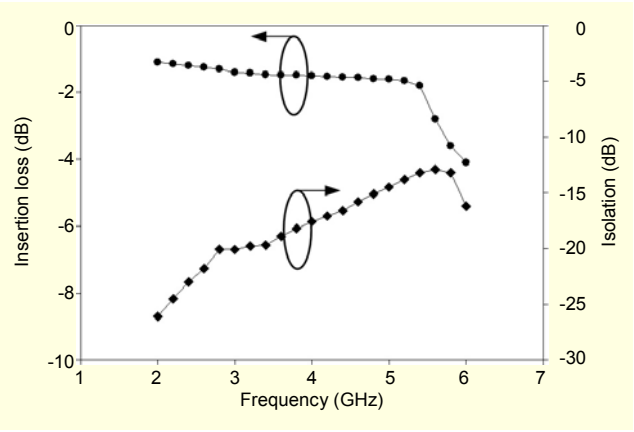

Fig. 3. Insertion loss and isolation characteristics of a switch.

M4. Series transistor M2 and shunt transistor M3 are in an off state at the same time [8]. The loss in the on transistor M1 mainly determines the insertion loss. Isolation is provided by the off series transistor M2. The on shunt transistor M4 helps in improving isolation by lowering the resistance seen at the source. The measurement results of a Tx/Rx selection switch are shown in Fig. 3.

For a low noise figure of an entire RF front-end receiver, sufficient gain of the LNA is required. By using a Darlington topology, a high gain can be achieved over the entire operating band. Recently reported CMOS LNAs [9], [10] have low gain due to the low transconductance of the CMOS and low cutoff frequency, f_T. The large parasitic capacitance, C_{gs}, C_{gd} of the CMOS reduces f_T. An insufficient f_T degrades the current gain at a high frequency. Therefore, it is important to increase f_T for a high gain at a high frequency. Reduction of parasitic capacitance is a way to increase f_T. This can be achieved by scaling down the CMOS gate length or by using a circuit topology. A UWB LNA using an f_T doubler, which is capable of reducing the parasitic capacitance of a MOS transistor, is proposed. Since the f_T doubler can be implemented by a

Darlington topology [11], a high current gain, $\beta(\omega)$, can also be attained at a high frequency. Figure 4 shows a designed two-stage CMOS LNA using a Darlington topology. The first stage is a cascode amplifier for the low noise figure and operates at a lower frequency than the second stage, and the second stage is a Darlington pair connection for high gain at high frequency.

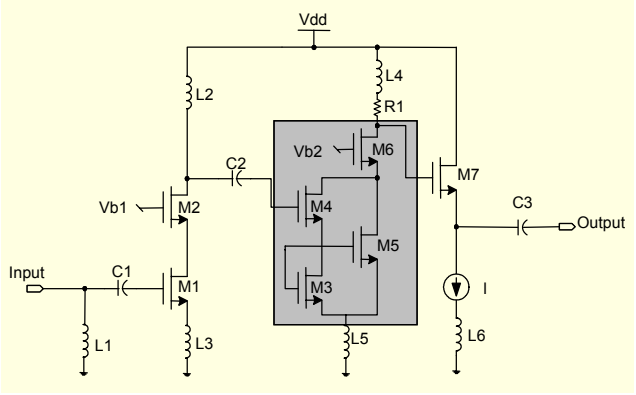

Fig. 4. Circuit of the wideband LNA.

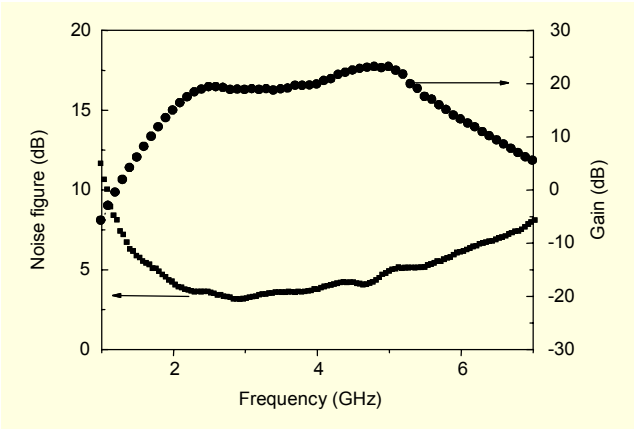

Fig. 5. Measured gain and noise figure of an LNA.

Figure 5 shows the measured gain and noise figure results. The measured gain is an average of 21 dB with ±2 dB flatness from 2.4 to 5.3 GHz. The noise figure is 3.15 dB to 4.8 dB from 3 to 5 GHz.

The double-balanced Gilbert-type mixer topology has been widely used due to its low local oscillator (LO) leakage and low even-order distortion products at the output. The trans-conductance function from the RF input to the differential IF output is given as in [12] as

$$\frac{I_{IF}}{V_{RF}}(j\omega) = g_{mRF}\, p_{11} \frac{1}{1+\dfrac{j\omega C_p}{g_{mLO}}}, \qquad (2)$$

where C_p is the parasitic capacitance at the common source node of the switching stage, g_{mLO} is the instantaneous transconductance of the switching pair, and p_{11} is the Fourier series coefficient of the fundamental frequency of the instantaneous current gain of each single-balanced cell with a sufficiently large LO signal [12]. To have a wide conversion gain, f_T of the transconductance stage transistor must be higher and C_p must be smaller. Therefore, the transconductance stage requires a large drive current and high-speed device. An extra inductor, L_p, at the common source node of the switching pair can reduce C_p. The inductor L_p is added in parallel with C_p, then making a resonance circuit at an LO frequency. With the current bleeding technique and an extra inductor, a high conversion gain can be obtained. Figure 6 shows a double-balanced down-conversion mixer. A single-ended-to-differential converter is merged at the mixer. For input impedance matching at 50 ohm, a series on-chip inductor is used.

The measured conversion gain of the LNA and down-mixer chain is shown in Fig. 7. The measured conversion gain shows an average power gain of 10 dB, and insertion loss is less than 20 dB from 3 GHz to 4.7 GHz.

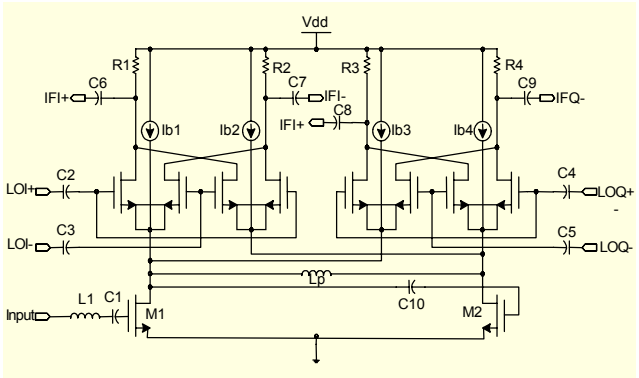

Fig. 6. Double-balanced down-conversion mixer.

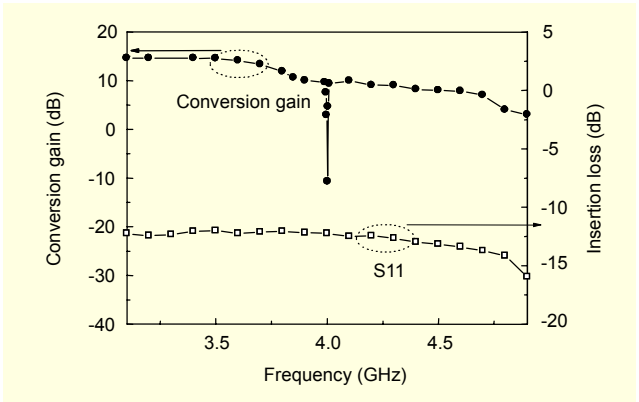

Fig. 7. Measured conversion gain and insertion loss of a down-converter.

2. Baseband Analog for DS-UWB Receiver

The baseband analog (BBA) for the DS-UWB receiver

consists of a variable gain amplifier (VGA) and low-pass filter (LPF). The core circuit of the Tx BBA is the same as the Rx BBA, but the number of stages is different.

Figure 8 shows the topology of the proposed VGA core and common mode feedback (CMFB). The VGA core utilizes a differential pair of cascode amplifiers. This suppresses even harmonics, rejects common-mode noises, and doubles the signal swing for a given supply voltage. It has the following additional features. First, the differential cascode configuration can extend the bandwidth and suppress signal distortion. Second, an active inductive load is used instead of a resistive load for wideband and low-voltage applications [13]. Third, a CMFB is achieved in a relatively simple way for a constant output DC level. Fourth, the current bleeding architecture in a load network increases the voltage gain [14]. Fifth, a constant current bias is used for good linearity and wideband performance regardless of the control voltages.

The input transistors M1 and M2 are made to operate in a triode region in order to use the exponential characteristic of g_{m1}. A variable gain can be achieved by controlling the gate voltage of transistors M3 and M4, Vctrl. A load network consists of active loads ((M7, M8, Is1, C1), (M10, M11, Is2, C2)), bleeding current sources (M9, M10), and DC level sensing transistors (M5, M6). The DC level sensing transistors monitor the DC level of output signals (Voutn, Voutp), and then a CMFB network (M13-M16) compares this DC level with a reference voltage (Vcm) and sets this DC level to Vcm by adjusting the bias currents of the bleeding current sources (M9, M10) automatically. With this bleeding technique, the current through the active load transistors (M8, M11) is reduced so that the output load resistance can be increased, leading to a higher gain [14]. The impedance of a single active load is given in [13] as

$$Z_0 \cong \frac{C_1}{g_{mM7} \cdot g_{mM8}} \left(s + \frac{g_{mM7}}{C_1} \right). \qquad (3)$$

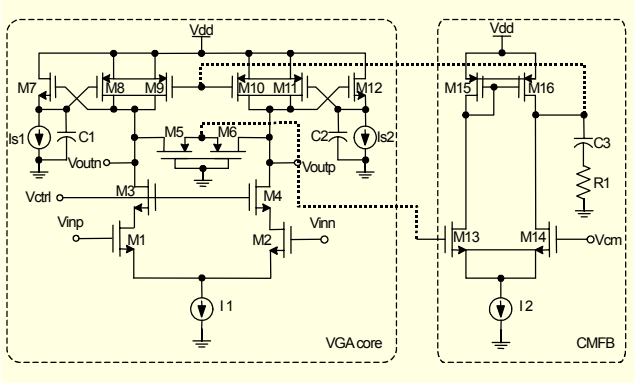

Fig. 8. Circuit of the VGA core and CMFB.

Equation (3) shows that this active load operates as an inductive load near the -3 dB frequency of the gain; therefore, the bandwidth of the VGA can be increased.

The receiver VGA is composed of a 3-stage VGA core and an output stage, and the transmitter VGA consists of a 1-stage VGA core and an output buffer as shown in Fig. 9.

Figure 10 shows the frequency response of the VGA at different control voltages. The control voltage, Vctrl, is varied from 0.8 to 1.6 V with increasing steps of 0.1 V. The measured bandwidth of the VGA is up to 970 MHz with a gain control

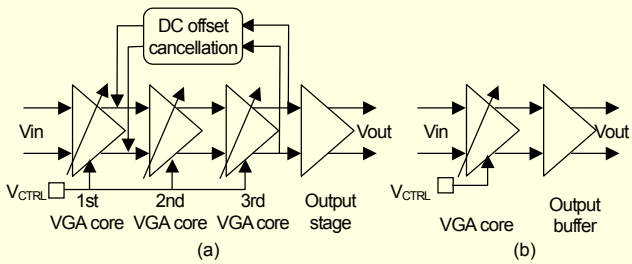

Fig. 9. Block diagrams of (a) Rx and (b) Tx VGAs.

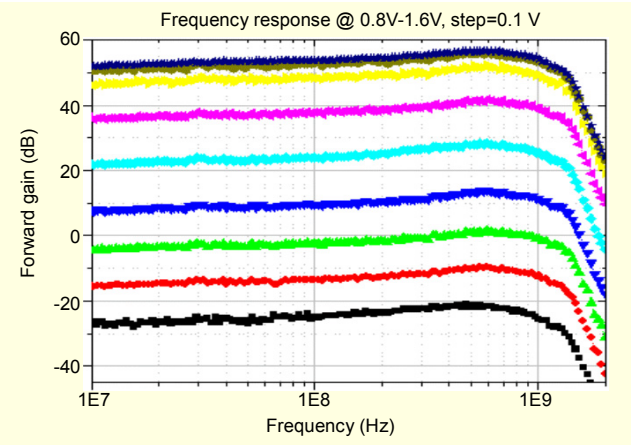

Fig. 10. Frequency response of an Rx VGA.

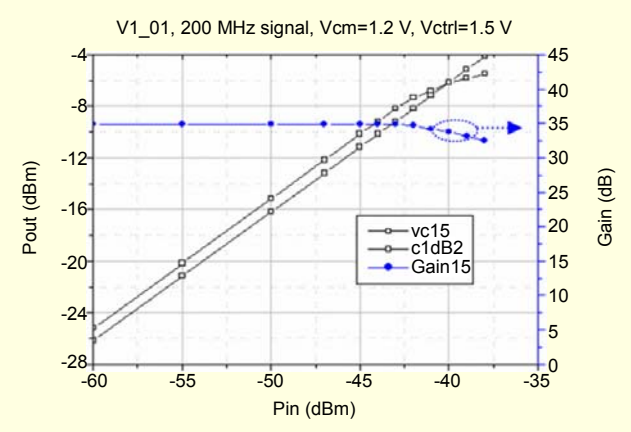

Fig. 11. Linearity characteristic of an Rx VGA.

range of 73 dB (-24.9 to 48.6 dB). The linearity characteristic of an Rx VGA at 200 MHz, 1.5 V control voltage is shown in Fig. 11.

The gyrator biquad architecture is implemented in an LPF. A general gyrator is composed of NMOS and PMOS, the drain of PMOS is connected to the gate of NMOS as shown in Fig 12. The parasitic capacitance of M1 works like an inductor at node X; therefore, the inductance can be expressed as

$$L = \frac{C_{1para}}{g_{m1} \cdot g_{m2}}. \quad (4)$$

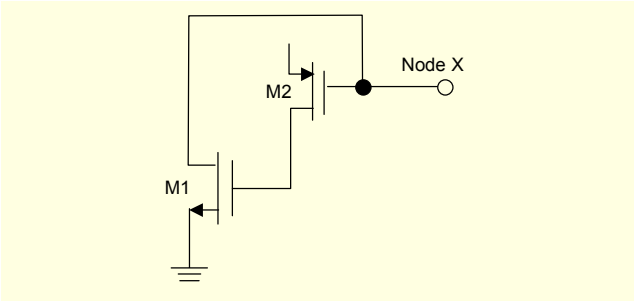

Fig. 12. General gyrator architecture.

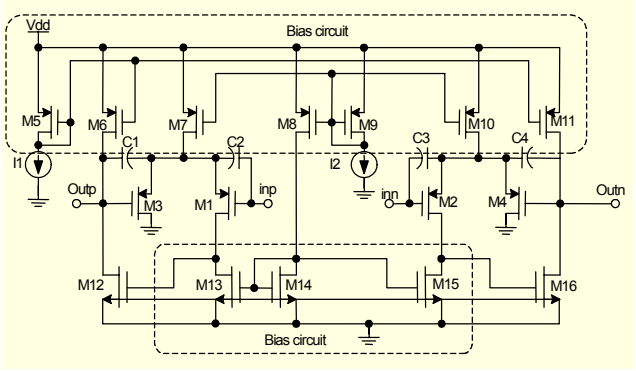

Fig. 13. Circuit of a gyrator biquad.

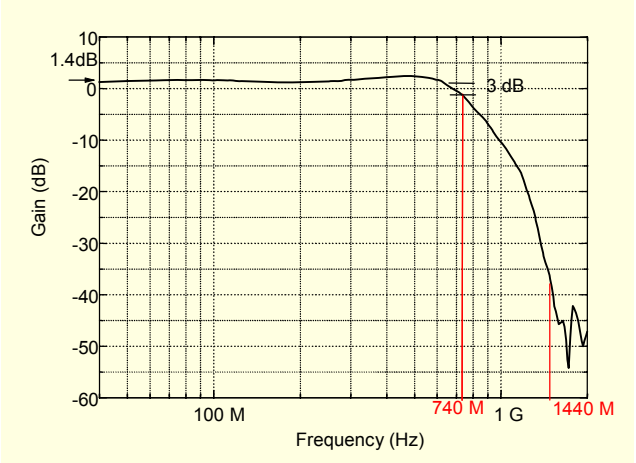

Fig. 14. Frequency response of an Rx LPF.

Figure 13 shows the gyrator biquad architecture. It is composed of the gyrator, bias circuit, and tuning capacitors, which control the ripple and frequency response. This architecture has two poles and zeros. The bandwidth is determined by varying the pole and zero values [15]. The receiver LPF is a fifth-order filter and consists of two-stage biquads and an output buffer.

The measurement results of an Rx LPF are shown in Fig. 14. The 3 dB cutoff bandwidth is 740 MHz, and the attenuation is more than 30 dB at 1440 MHz.

3. RF Front-End Transmitter

The RF front-end transmitter is composed of a DA, a differential-to-single-ended (D2S) converter, and an up-mixer. Figure 15 shows the block diagram of an RF transmitter, which consists of a double-balanced mixer with a linear transconductor, a DA merged with a D2S converter, and a wideband output matching network which is included in the DA block.

In this transmitter, the up-mixer adopts a conventional linear transconductor to improve the linearity. A double-balanced topology is used to suppress the strong LO power spectrum. Since the common-source transconductor exhibits smaller third-order nonlinearity than the differential pair at equal bias [16], this CMOS mixer utilizes the common-source transconductor as its input stage. The transconductor and double-balanced up-mixer are shown in Figs. 16 and 17, respectively.

With a constant current, I_3, I_4, through M1 and M2, V_{GS1} and V_{GS2} remain fixed so that variation of the input voltage is directly transferred to the resistor, R. Thus, the relationship between the current I_R through R and the input voltage, V_{IN}, is expressed as a linear equation under a linear resistor, R. By mirroring the current of M3 and M4, a linear trans-conductance stage is formed:

$$G_m = \frac{I_{out}}{V_{IN}} = \frac{W_5}{W_3} \cdot \frac{2}{R}. \quad (5)$$

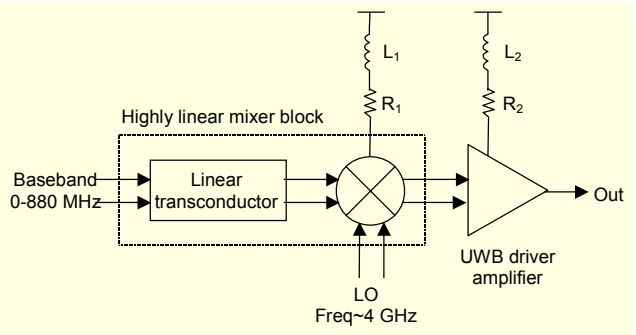

Fig. 15. Block diagram of the DS-UWB RF transmitter.

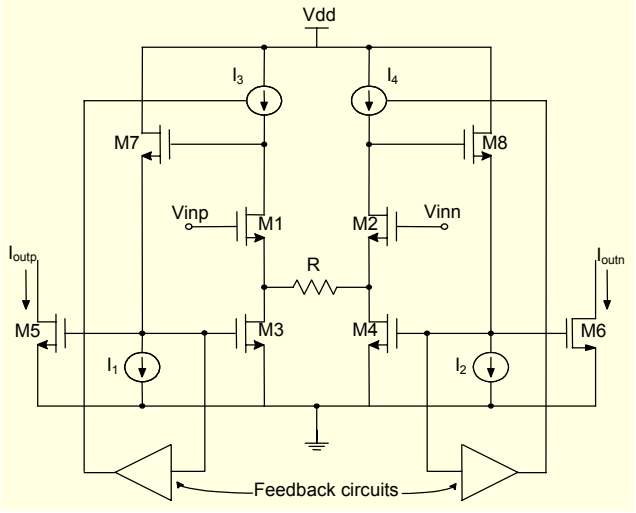

Fig. 16. Linear transconductor.

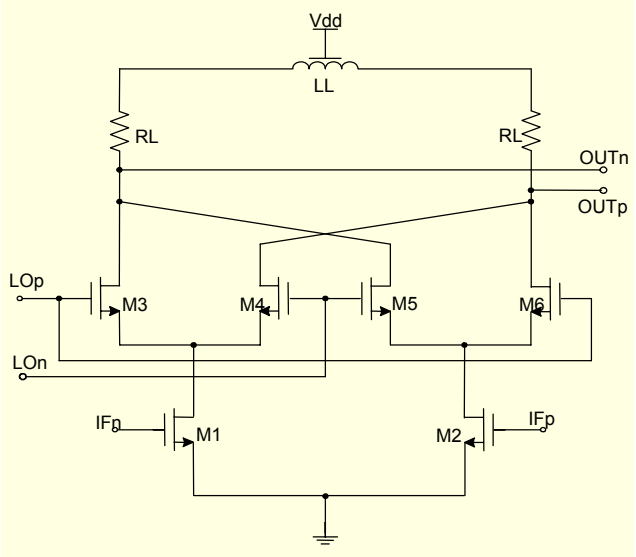

Fig. 17. Double-balanced up-mixer.

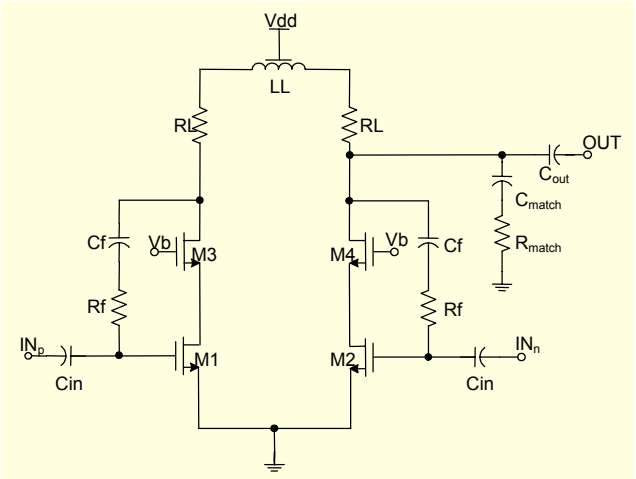

Fig. 18. DA with output matching circuit.

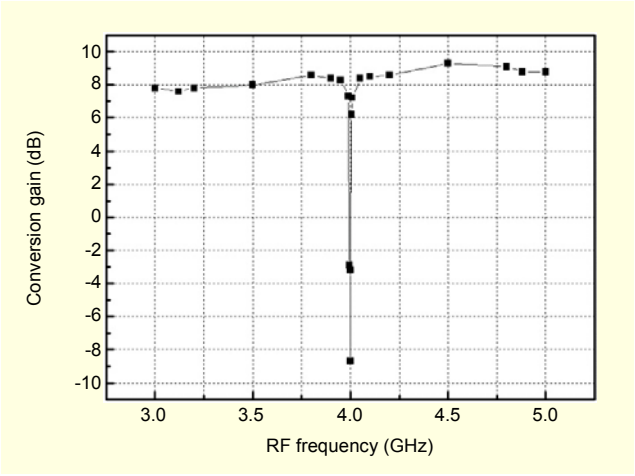

Fig. 19. Frequency response of an RF transmitter.

The DA is the differential structure, and while it has some advantages, we need a single-ended output stage because the transmitting antenna has a single input port. We can take the single-ended output only from the differential outputs of the DA, therefore the D2S converter is designed simply. The RC parallel filter structure is applied to the output stage of the DA. Figure 18 shows the DA with a wideband output matching circuit.

The measured frequency response of the RF transmitter is shown in Fig. 19. The gain flatness is 8.5 ± 0.8 dB.

4. Frequency Synthesizer

The frequency synthesizer generates the quadrature 4-GHz LO frequency needed for the mixers in the Rx and Tx chains. The synthesizer phase locks an on-chip voltage controlled oscillator (VCO) to a 1 MHz reference. The block diagram of the used integer-N frequency synthesizer is shown in Fig. 20. It consists of a phase frequency detector, a charge pump, an off chip loop filter, a VCO, a prescaler, a program and swallow counter, an R counter, and a lock detector. The quadrature 4-

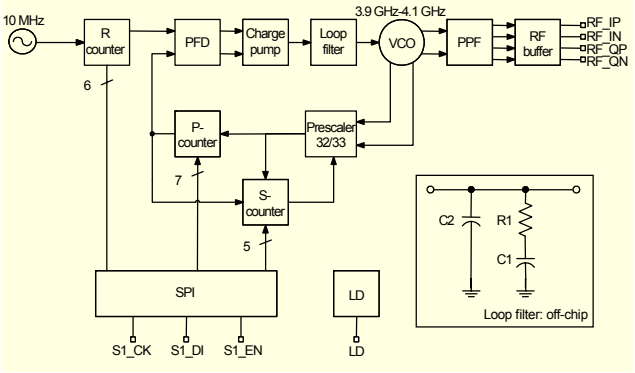

Fig. 20. Frequency synthesizer block diagram.

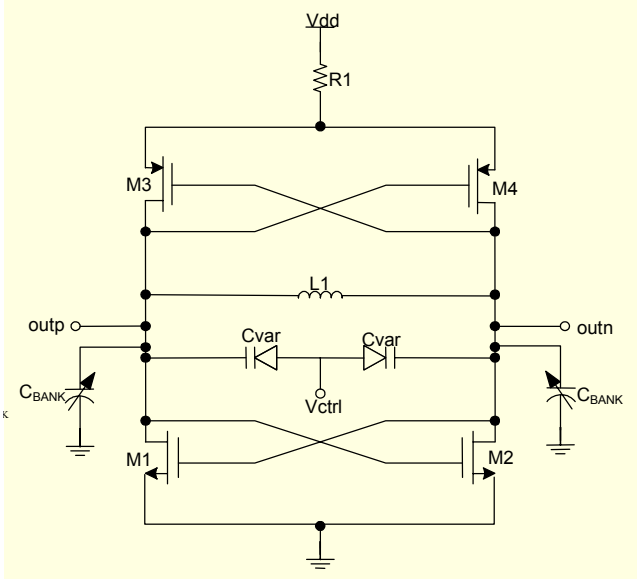

Fig. 21. Circuit schematic of a VCO.

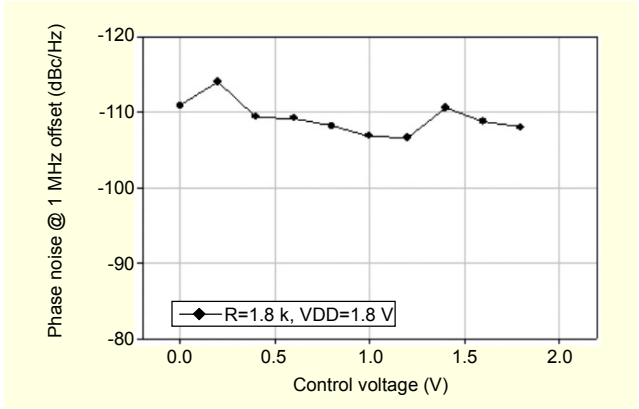

Fig. 22. Phase noise characteristic of a VCO.

GHz LOs are generated by passing the VCO waveform through an RC-CR poly-phase filter. Each frequency channel is selected by varying the serial-to-parallel interface block.

Figure 21 shows the schematic of the VCO. The complementary cross-coupled transistors M1, M2, M3, and M4 generate the negative impedance required to cancel the losses of the RLC tank circuit. Therefore, the negative impedance can be expressed as

$$R_{\text{negative}} = -\frac{2}{g_{mn} + g_{mp}}. \quad (6)$$

Because tank voltage amplitude has an important effect on the phase noise as in (7) and a better rise- and fall-time symmetry which results in a smaller $1/f^3$ noise corner [17], a PMOS, NMOS complementary LC oscillator is applied in our study.

$$L(\Delta\omega) = 10\log_{10}\left(\frac{i_n^2/\Delta f}{q_{\max}^2}\cdot\frac{\Gamma_{rms}^2}{2\Delta\omega^2}\right), \quad (7)$$

where q_{max} is the tank voltage amplitude. By choosing the values of Cvar and C_{BANK}, we can control the frequency range.

The measured phase noise of a VCO versus control voltage is shown in Fig. 22. The average phase noise is -110 dBc at a 1 MHz offset.

IV. Transceiver Experimental Results

This transceiver is fabricated in a 0.18 μm, single-poly six-metal CMOS technology. The die photograph is shown in Fig. 24. It occupies an area of 9.0 mm^2 including pads and is packaged in a 64-pin MicroLead Frame plastic package. Figure 23 shows a package model, including the wirebonding, used in the simulation of each individual block. The receiver chain dissipates 65 mA, the transmitter consumes 44 mA, and the synthesizer dissipates 34 mA from a 1.8 V power supply.

Figure 25 shows the digital-to-analog converter output spectrum of the direct-sequence spread spectrum, while Fig. 26 shows the RF transmission spectrum mask.

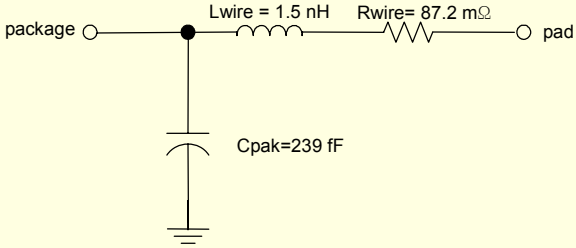

Fig. 23. Package and wirebonding model.

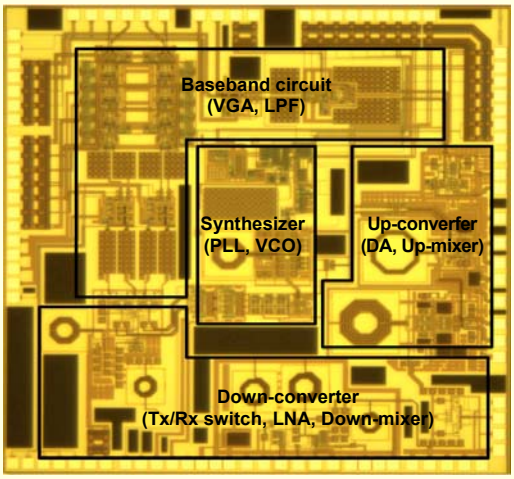

Fig. 24. Photo of a transceiver die (die size: 3000 × 3000 μm^2).

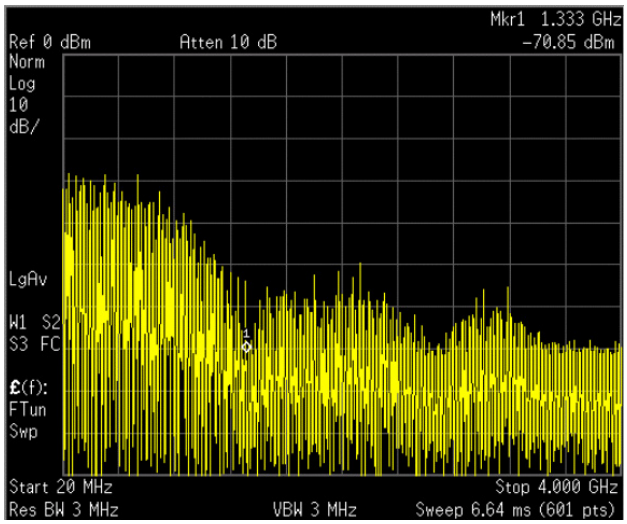

Fig. 25. Digital-to-analog converter output spectrum.

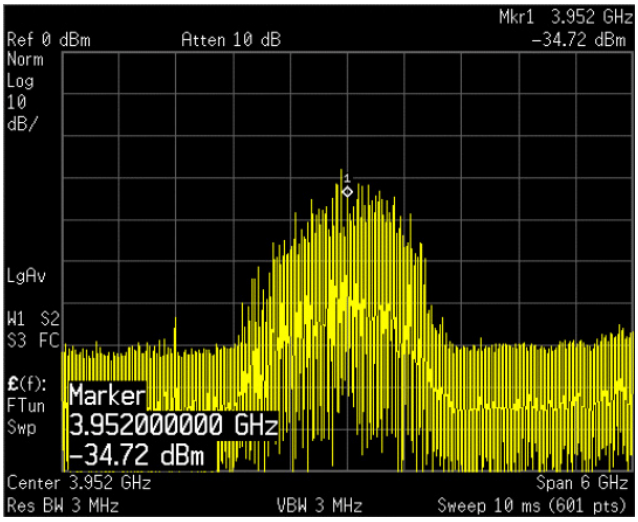

Fig. 26. RF transmission spectrum mask.

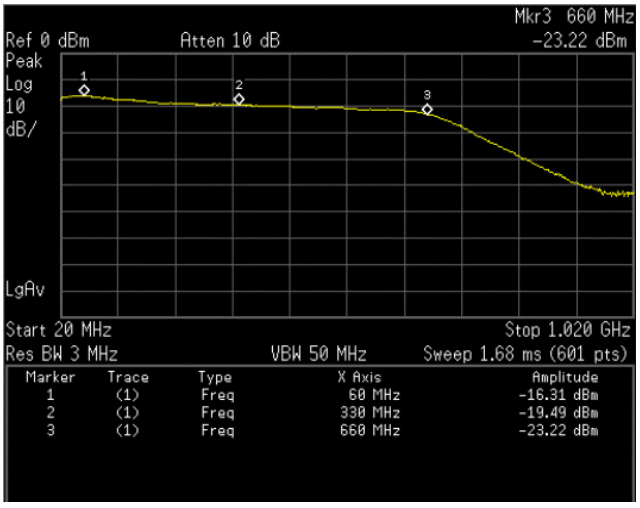

Fig. 27. Frequency response of a receiver.

Table 1. Comparison of DS-UWB transceiver performance.

Parameter	Sachio Iida et al. [2]	Our transceiver
Frequency band	3.1 to 5 GHz	3.1 to 5 GHz
LPF cutoff freq	500 MHz	660 MHz
Technology	0.18 μm CMOS	0.18 μm CMOS
Die area	9.3 mm^2	9 mm^2
Power consumption (Vdd=1.8 V)	105 mW for Tx mode	140 mW for Tx mode
	280 mW for Rx mode	178 mW for Rx mode

Table 2. Measured transceiver performance of the proposed transceiver.

Parameter	Measurement results
Frequency band	3.1 to 5 GHz
Voltage gain	72 dB
IIP3	- 27.1 dBm
I,Q gain mismatch	± 0.6 dB
Tx output P1 dB	- 1.8 dBm
Phase noise @ 1 MHz offset	- 110 dBc/Hz
Rx current consumption	65 mA
Tx current consumption	44 mA
Package	64-pin MicroLead Frame

Figure 26 shows the characteristics of a transmission mask at an antenna port. The average power is -8.3 dBm. The frequency response of the receiver is shown in Fig. 27. The flatness of the receiver is 3.5 dB in the 660 MHz bandwidth.
A performance comparison of the DS-UWB CMOS transceivers is summarized in Table 1. Table 2 summarizes the measured performance of the transceiver.

The experimental results of a transceiver include the external bandpass filter, cable loss, and PCB line loss.

V. Conclusion

A low-power, ultra-wideband direct-conversion CMOS RF transceiver has been presented in this paper. The 3.1 to 5 GHz transceiver fabricated in 0.18 μm CMOS technology meets the necessary transmission power, noise characteristics, and bandwidth requirement. Although direct-conversion is employed, the DC-offset is cancelled using the DC blocking capacitor. The transceiver including synthesizer consumes no more than 143 mA from a 1.8 V supply. Finally, to demonstrate the potential applications of the techniques, circuit prototypes and measurement results were presented for a down-converter, up-converter, baseband analog, and VCO.

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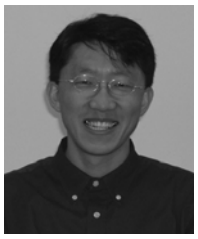
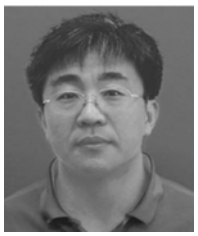


Bonghyuk Park received the BS degree in electrical engineering from Kyungpook National University, Korea, in 1996, and the MS degree in mechatronics from Gwangju Institute Science and Technology (GIST), Gwangju, Korea, in 1998, respectively. From 1998 to 1999, he worked as an RF Application Engineer at Ansoft. Since 1999, he has been with Electronics and Telecommunications Research Institute (ETRI), and he is also working toward the PhD degree from KAIST Daejeon, Korea. His main research interests include UWB RF transceiver front-end circuit design and system-level integration of transceivers.

Kyung Ai Lee received the BS degree in electrical engineering from Kyungpook National University, Daegu, Korea, in 2002, and the MS degree in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2004. She is currently working toward a PhD degree. Her research interests include analog, RF, and microwave IC design for wireless communications; CMOS, HBT, and HEMT technologies; and specifically, the analysis and design of power amplifiers for military and commercial applications.



Songcheol Hong received the BS and MS degrees in electronics from Seoul National University, Seoul, Republic of Korea, in 1982 and 1984, respectively. He received the PhD degree in electrical engineering from the University of Michigan, Ann Arbor, USA, in 1989. In May 1989, he joined the faculty of Dept. Electrical Engineering and Computer Science at Korea Advanced Institute of Science and Technology (KAIST). He held short visiting professorships at Stanford University, Palo Alto, and Samsung Microwave Semiconductor, USA, in 1997. His research interests are microwave integrated circuits and systems, including power amplifiers for mobile communications, miniaturized radar, millimeter-wave frequency synthesizers, as well as novel semiconductor devices.

Sangsung Choi received the BS degree in radio communication from Hanyang University, Korea, in 1977; the ME degree in communication from Korea University, Korea, in 1979; the MS degree in avionics from Ohio University, USA, in 1990; and the PhD degree in electrical engineering from University of Wyoming, USA, in 1999. He is currently the Team Leader of Digital Home Research Division in Electronics and Telecommunications Research Institute (ETRI), Daejeon, Korea. His main research interests are wireless home networking technologies including UWB technology.